SRAM

128K X 8 HIGH SPEED CMOS STATIC RAM

FEATURES

ßbFast Address Access Times : 10/12/15ns

ßbSingle 3.3V ±0.3V power supply

ßbCenter power/ground pin configuration

ßbLow Power Consumption : 110/105/100mA

ßbTTL I/O compatible

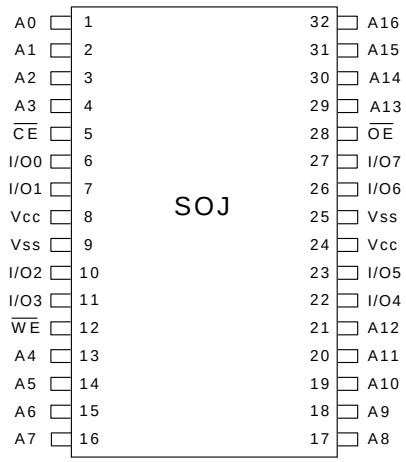
ßb2.0V data retention mode

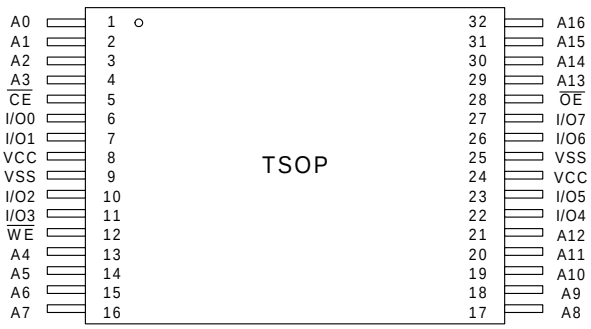
ßbAutomatic power-down when deselected

ßbAvailable packages :

- 32-pin 300 mil and 400 mil SOJ
- 32-pin TSOP 8x13.4mm and 8x20mm

PIN CONFIGURATION

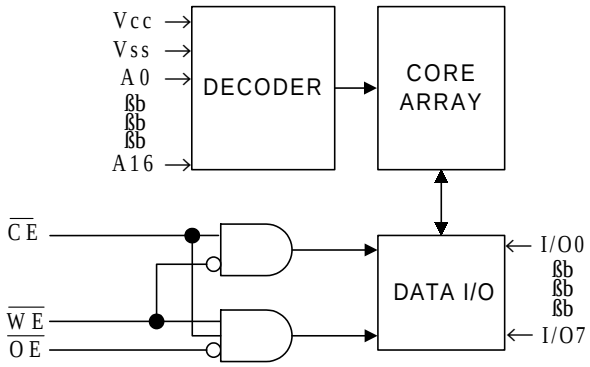




GENERAL DESCRIPTION

The T14L1024N is a one-megabit density, fast static random access memory organized as 131,072 words by 8 bits. It is designed for use in high performance memory applications such as main memory storage and high speed communication buffers. Fabricated using high performance CMOS technology, access times down to 10ns are achieved.

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
I/O0 - I/O7	Data Inputs/Outputs
$\overline{CE}$	Chip Select Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power Supply
Vss	Ground

PART NUMBER EXAMPLES

	PACKAGE	SPEED
T14L1024N-10J	SOJ 300mil	10ns
T14L1024N-10W	SOJ 400 mil	10ns
T14L1024N-10P	TSOP 8x13.4mm	10ns
T14L1024N-10H	TSOP 8x20mm	10ns

DC CHARACTERISTICS ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYM	RATING	UNIT
Power Supply Voltage	Vcc	-0.5 to 4.6	V
Input Voltage	V_{IN}	-0.5 to Vcc+0.5	V
Output Voltage	V_{OUT}	-0.5 to Vcc+0.5	V
Operating Temperatrue	T_{OPR}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OUT}	50	mA

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O0- I/O7	Vcc
H	X	X	Not Selected	High-Z	$I_{SB,}$ I_{SB1}
X	X	X	Not Selected	High-Z	$I_{SB,}$ I_{SB1}
L	H	H	Output Disable	High-Z	Icc
L	L	H	Read	Data Out	Icc
L	X	L	Write	Data In	Icc

OPERATING CHARACTERISTICS

(Vcc = 3.3V ±0.3V, Ta = 0 to 70°C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	MAX.	UNIT
Power Supply Voltage	Vcc			3.0	3.6	V
Input Low Voltage	V_{IL}			-0.5	0.8	V
Input High Voltage	V_{IH}			2.1	Vcc+0.3	V
Input Leakage Current	I_{LI}	V_{IN} =Vss to Vcc		-	5	µA
Output Leakage Current	I_{LO}	V_{IN}=Vss to Vcc , $\overline{CE}$ = V_{IH} $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		-	5	µA
Output Low Voltage	V_{OL}	I_{OL} = 4.0 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} =-2.0 mA		2.4	-	V
Operating Power Supply Current	Icc	$\overline{CE}$ = V_{IL}	10ns	-	110	mA
		f=max	12ns	-	105	mA
		IO = 0mA	15ns	-	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CE}$ = V_{IH}, IO = 0mA		-	25	mA
	I_{SB1}	Vcc = max; $\overline{CE}$ > Vcc-0.2V; f=0mhz; IO = 0mA		-	5	mA

Note: Typical characteristics are at Vcc = 3.3V, Ta = 25°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYM	MIN	TYP	MAX	UNIT
Supply Voltage	Vcc	Typ-0.3	3.3	Typ+0.3	V
Input Voltage, low	V_{IL}	-0.3	-	0.8	V
Input Voltage, high	V_{IH}	2.1	-	Vcc+0.3	V
Ambient Temperature	T_A	0	-	70	°C

CAPACITANCE

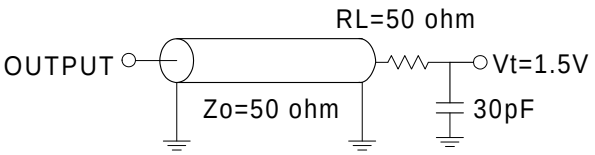
PARAMETER	SYMBOL	CONDITION	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/ Output Capacitance	$C_{I/O}$	V_{OUT}= 0V	8	pF

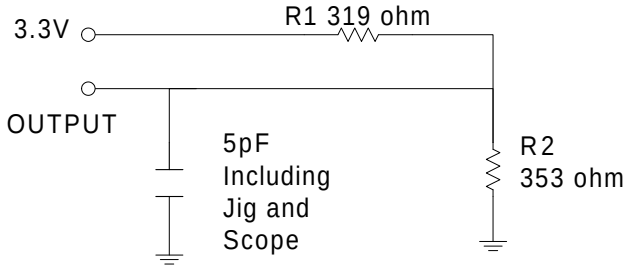
Note: These parameters are sampled but not 100% tested.

AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3.0 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L =30pF,I_{OH}/I_{OL}= -2mA/4mA

AC TEST LOADS AND WAVEFORM





(For TCLZ, TOLZ, TCHZ, TOHZ, TWHZ, TOW)

AC CHARACTERISTICS

(V_{CC}=3.3V ±0.3V, Vss = 0V, Ta = 0 to 70°C)

(1) READ CYCLE

PARAMETER	SYM.	T14L1024N-10		T14L1024N-12		T14L1024N-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	10	àµ	12	àµ	15	àµ	ns
Address Access Time	t_{AA}	àµ	10	àµ	12	àµ	15	ns
Chip Enable Access Time	t_{ACS}	àµ	10	àµ	12	àµ	15	ns
Output Enable to Output Valid	t_{AOE}	àµ	6	àµ	7	àµ	7	ns
Chip Enable to Output in Low Z	t_{CLZ*}	3	àµ	3	àµ	3	àµ	ns
Output Enable to Output in Low Z	t_{OLZ*}	0	àµ	0	àµ	0	àµ	ns
Chip Disable to Output in High Z	t_{CHZ*}	àµ	5	àµ	6	àµ	7	ns
Output Disable to Output in High Z	t_{OHZ*}	àµ	5	àµ	6	àµ	7	ns
Output Hold from Address Change	t_{OH}	3	àµ	3	àµ	3	àµ	ns

* These parameters are sampled but not 100% tested.

(2)WRITE CYCLE

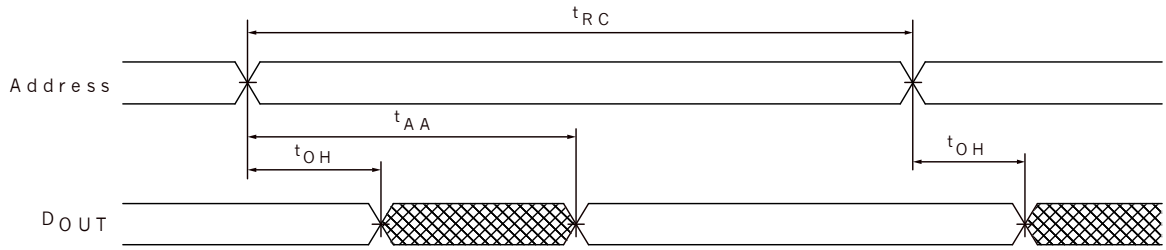
PARAMETER	SYM.	T14L1024N-10		T14L1024N-12		T14L1024N-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	10	àµ	12	àµ	15	àµ	ns
Chip Enable to End of Write	t_{CW}	8	àµ	10	àµ	11	àµ	ns
Address Valid to End of Write	t_{AW}	8	àµ	10	àµ	11	àµ	ns
Address Setup Time	t_{AS}	0	àµ	0	àµ	0	àµ	ns
Write Pulse Width	t_{WP}	8	àµ	10	àµ	11	àµ	ns
Write Recovery Time	t_{WR}	0	àµ	0	àµ	0	àµ	ns
Data Valid to End of Write	t_{DW}	6	àµ	8	àµ	8	àµ	ns
Data Hold from End of Write	t_{DH}	0	àµ	0	àµ	0	àµ	ns
Write to Output in High Z	t_{WHZ*}	àµ	5	àµ	6	àµ	6	ns
Output Disable to Output in High Z	t_{OHZ*}	àµ	5	àµ	6	àµ	7	ns
Output Active from End of Write	t_{OW}	0	àµ	0	àµ	0	àµ	ns

* These parameters are sampled but not 100% tested.

TIMING WAVEFORMS

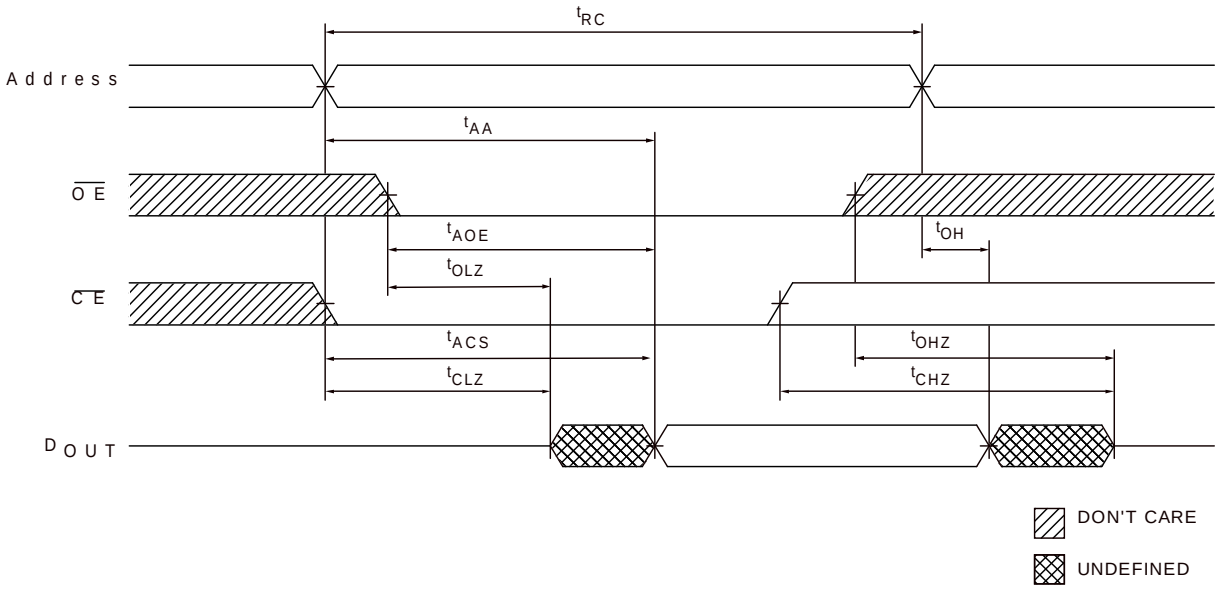
READ CYCLE 1

(Address Controlled)

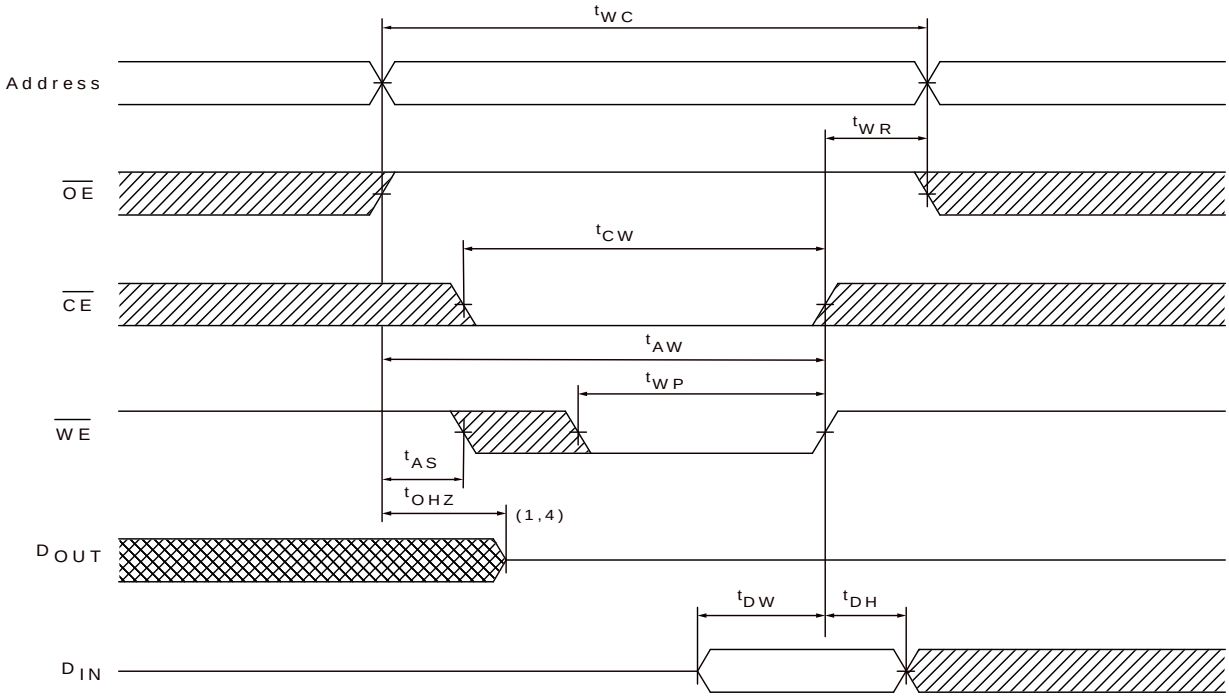


READ CYCLE 2

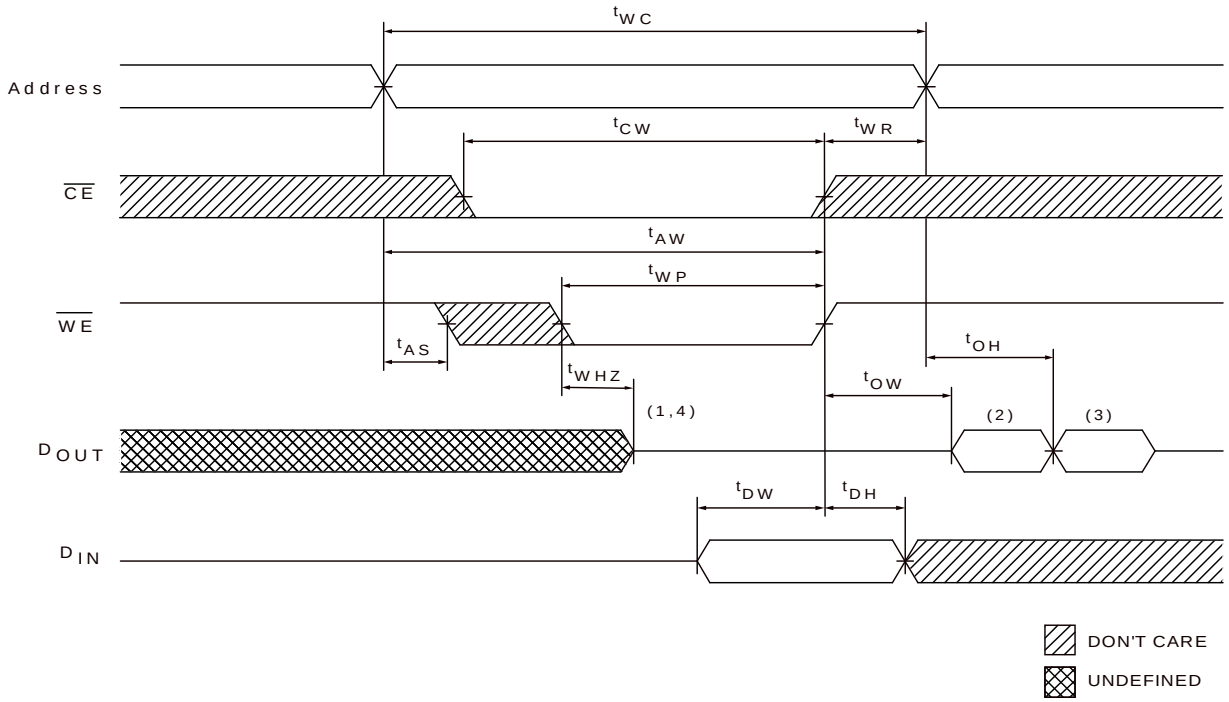
(Chip Enable Controlled)



WRITE CYCLE 1 ($\overline{OE}$ CLOCK)



WRITE CYCLE 2 ($\overline{OE}$ = V_{IL} Fixed)

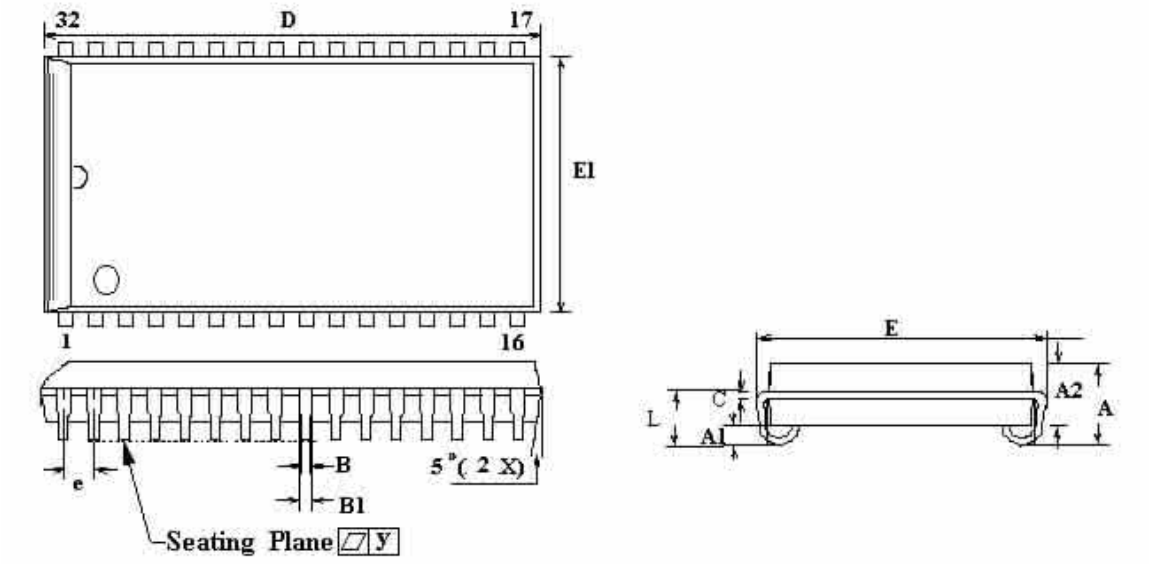


Notes: 1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.

2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with C_L = 5pF. This parameter is guaranteed but not 100% tested.
5. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

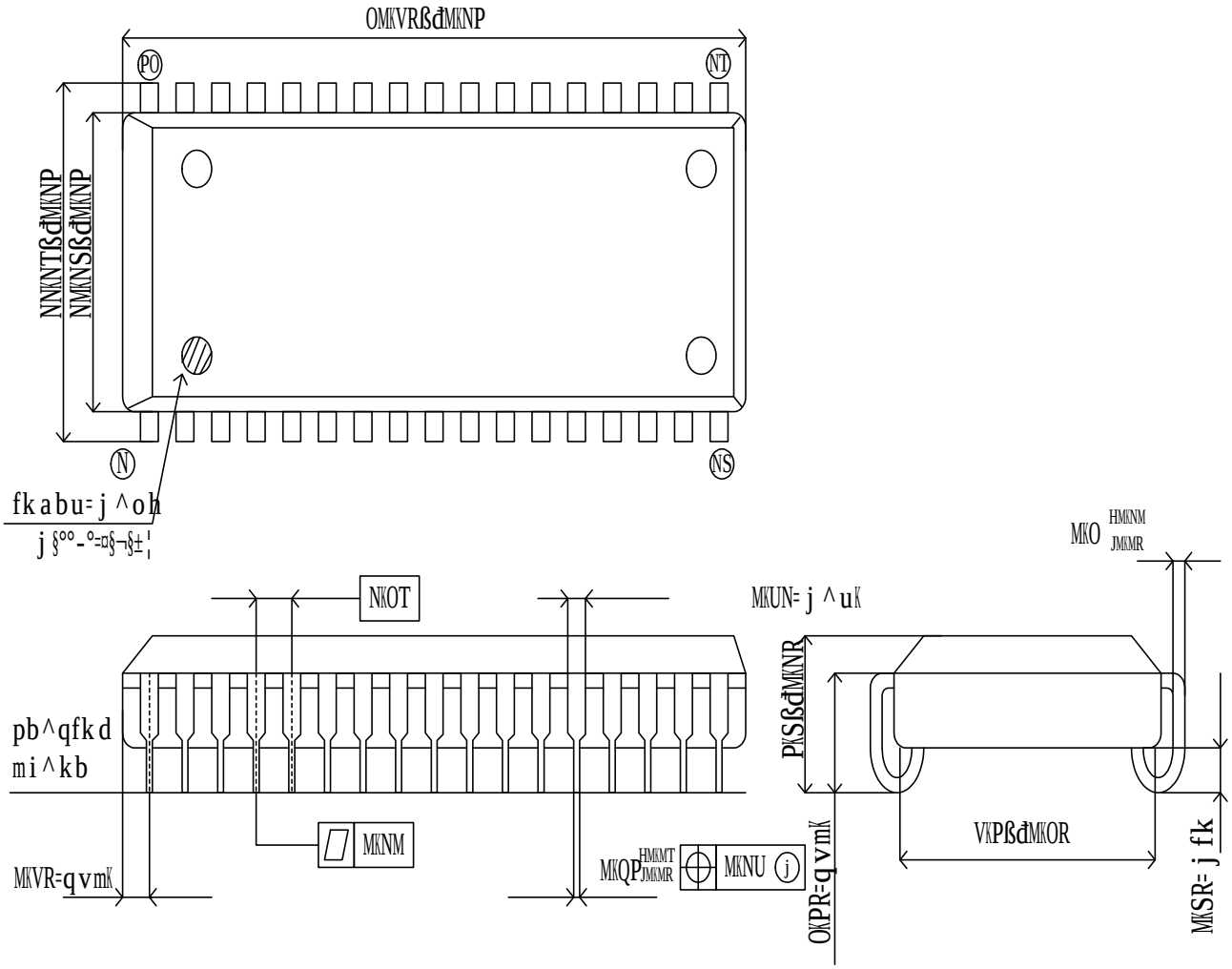
PACKAGE DIMENSIONS

32-LEAD SOJ (300 mil)

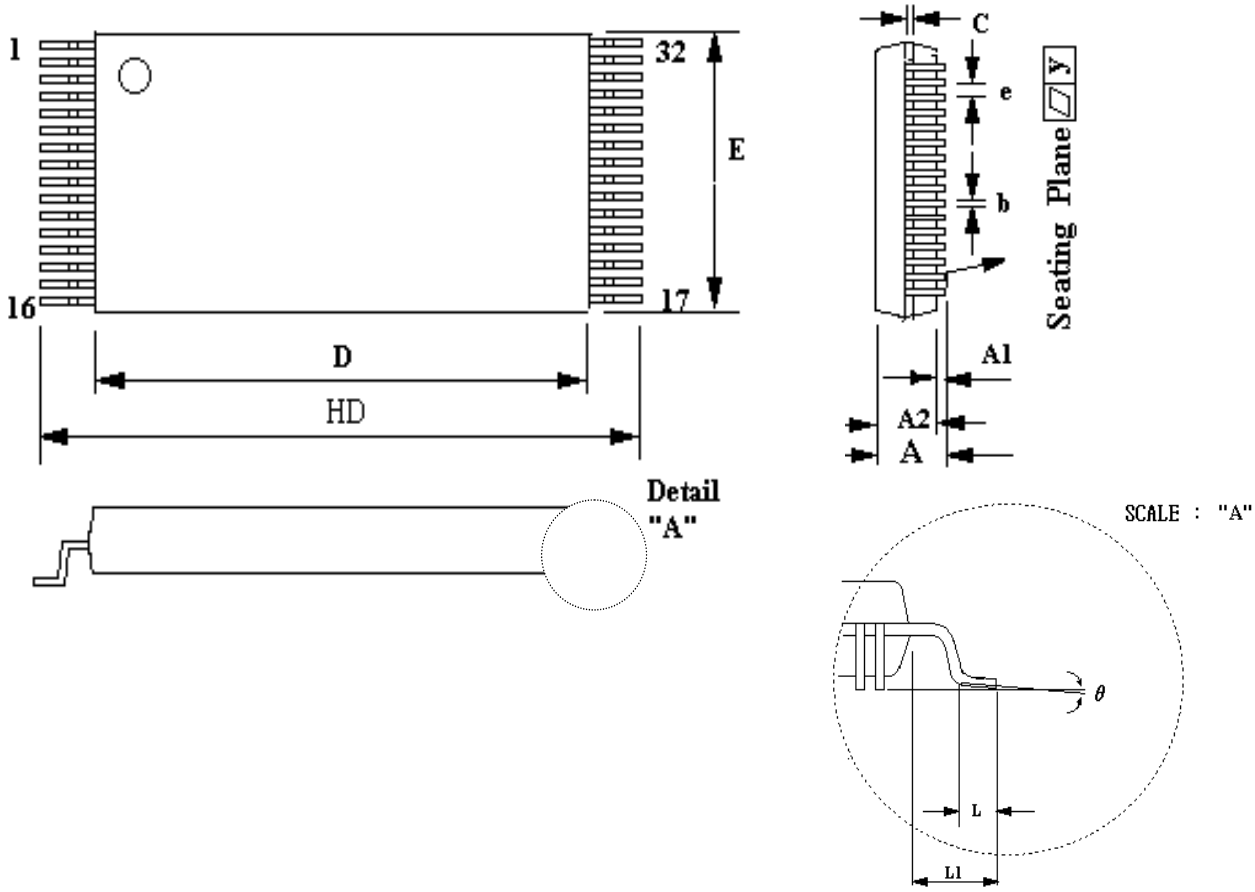


SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.140(MAX)	3.556(MAX)
A1	0.026(MIN)	0.660(MIN)
A2	0.100±0.005	2.540±0.127
B	0.018(TYP)	0.457(TYP)
B1	0.028(TYP)	0.711(TYP)
C	0.008(TYP)	0.203(TYP)
D	0.823±0.005	20.904±0.127
E	0.335±0.010	8.509±0.254
E1	0.300±0.005	7.620±0.127
e	0.050(TYP)	1.270(TYP)
L	0.086±0.010	2.184±0.254
y	0.003(MAX)	0.076(MAX)

PACKAGE DIMENSIONS
32-LEAD SOJ (400 mil)



PACKAGE DIMENSIONS
32-LEAD TSOP (8x13.4mm)



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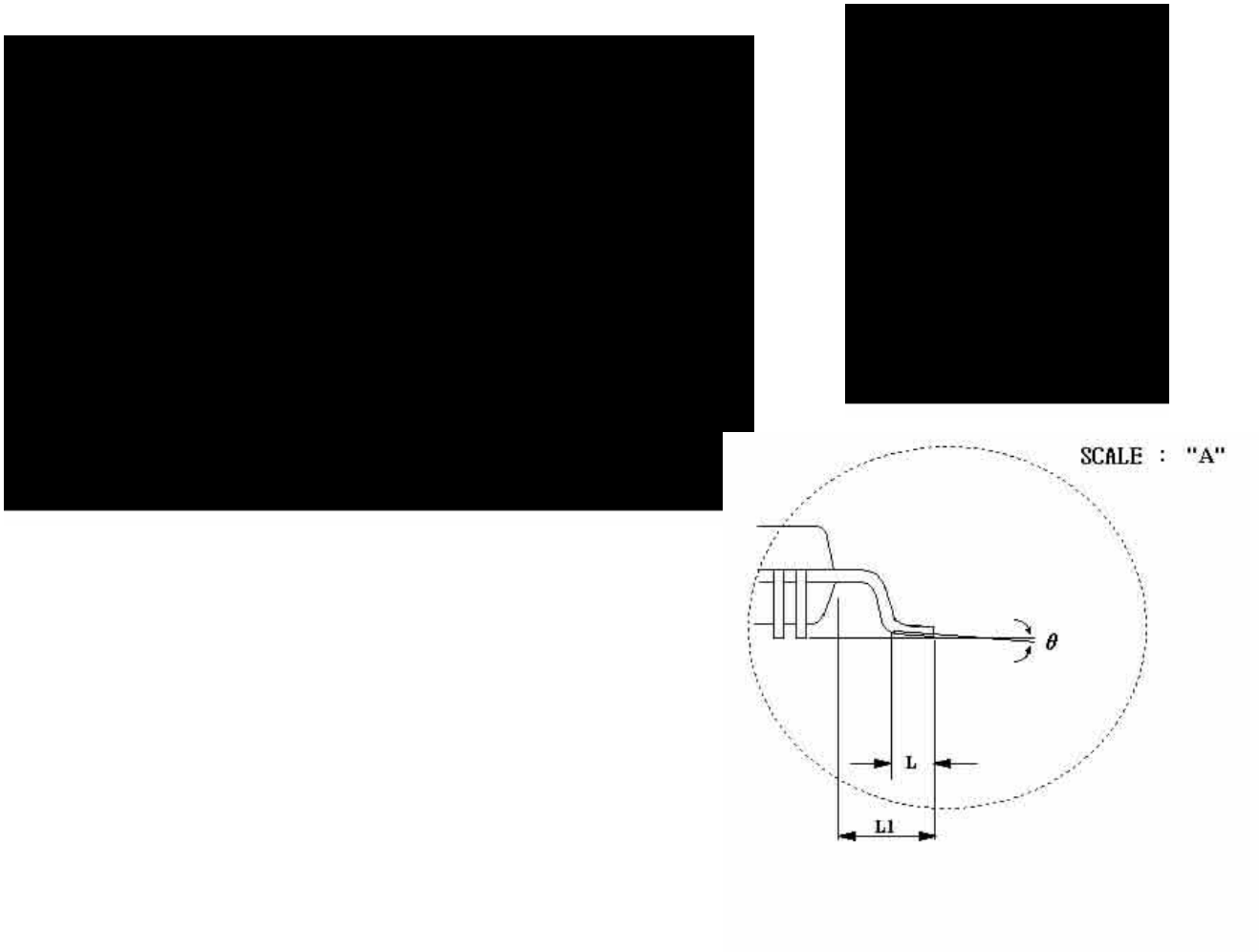
=	pvj_li ==a§«£¬±§-¬=§¬=§¬¡¦£±==	Dimension in mm
	^ MKMQQEj^uF	=1KNMEj^uF
	^N MKMMQ±MKMMO	=MKMR±MKMR
	^O MKMQNEj^uF	=NKMOEj^uF
	MKMMUßđMKMMQ	=MKOMßđMKNM
	C MKMMS±MKMMN	=MKNR±MKMO
	D MKQSR±MKMMU	=NNKU±MKO
	E MKPNR±MKMMQ	=UKM±MKN
	ea MKROU±MKMMU	=NPKQ±MKO
	e MKMOMEqvmKF	MKREqvmKF
	i MKMOM±MKMMQ	=MKR±MKN
	iN MKMPN±MKMMU	=MKU±MKO
	· MKMMOEj^uF	=MKMREj^uF
	á¡ ==Mß`¼Rß`	==Mß`¼Rß`

PACKAGE DIMENSIONS
32-LEAD TSOP (8x20mm)



SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.047(MAX)	1.19(MAX)
A1	0.012±0.002	0.30(MIN)
A2	0.035±0.002	0.889±0.051
b	0.009±0.002	0.229±0.051
C	0.006±0.001	0.152 ±0.026
D	0.787±0.008	19.99±0.203
Db	0.724±0.004	18.39±0.1
E	0.315±0.004	8.00±0.01
L	0.024±0.004	0.610±0.102
L1	0.032(TYP)	0.813(TYP)
á¡	0°~12°	0°~12°