

### Document Title

256Kx16 bit Dynamic RAM with EDO Page Mode

### Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0A	Initial Draft	August 9,2001	
0B	Revise for typo on page 20	December 18,2001	

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# IC41C16256 IC41LV16256



## 256K x 16 (4-MBIT) DYNAMIC RAM WITH EDO PAGE MODE

### FEATURES

- Extended Data-Out (EDO) Page Mode access cycle
- TTL compatible inputs and outputs; tristate I/O
- Refresh Interval: 512 cycles /8 ms
- Refresh Mode: RAS-Only, CAS-before-RAS (CBR), Hidden
- Single power supply:
  - 5V  $\pm$  10% (IC41C16256)
  - 3.3V  $\pm$  10% (IC41LV16256)
- Byte Write and Byte Read operation via two  $\overline{\text{CAS}}$
- Industrial Temperature Range -40°C to 85°C

### DESCRIPTION

The *ISI* IC41C16256 and IC41LV16256 is a 262,144 x 16-bit high-performance CMOS Dynamic Random Access Memories. The IC41C16256 offer an accelerated cycle access called EDO Page Mode. EDO Page Mode allows 512 random accesses within a single row with access cycle time as short as 10 ns per 16-bit word. The Byte Write control, of upper and lower byte, makes the IC41C16256 ideal for use in 16-, 32-bit wide data bus systems.

These features make the IC41C16256 and IC41LV16256 ideally suited for high-bandwidth graphics, digital signal processing, high-performance computing systems, and peripheral applications.

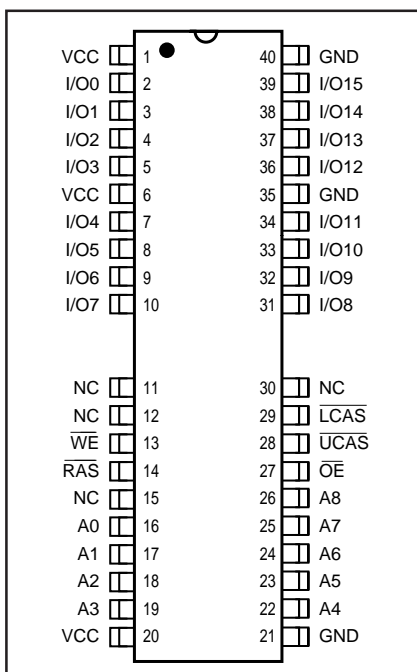
The IC41C16256 is packaged in a 40-pin 400mil SOJ and 400mil TSOP-2.

### KEY TIMING PARAMETERS

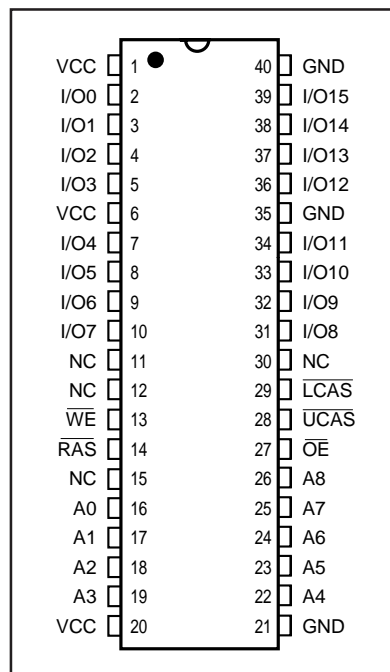
Parameter	-25(5V)	-35	-50	-60	Unit
Max. RAS Access Time ( $t_{\text{RAC}}$ )	25	35	50	60	ns
Max. CAS Access Time ( $t_{\text{CAC}}$ )	8	10	14	15	ns
Max. Column Address Access Time ( $t_{\text{AA}}$ )	12	18	25	30	ns
Min. EDO Page Mode Cycle Time ( $t_{\text{PC}}$ )	10	12	20	25	ns
Min. Read/Write Cycle Time ( $t_{\text{RC}}$ )	45	60	90	110	ns

### PIN CONFIGURATIONS

#### 40-Pin TSOP-2



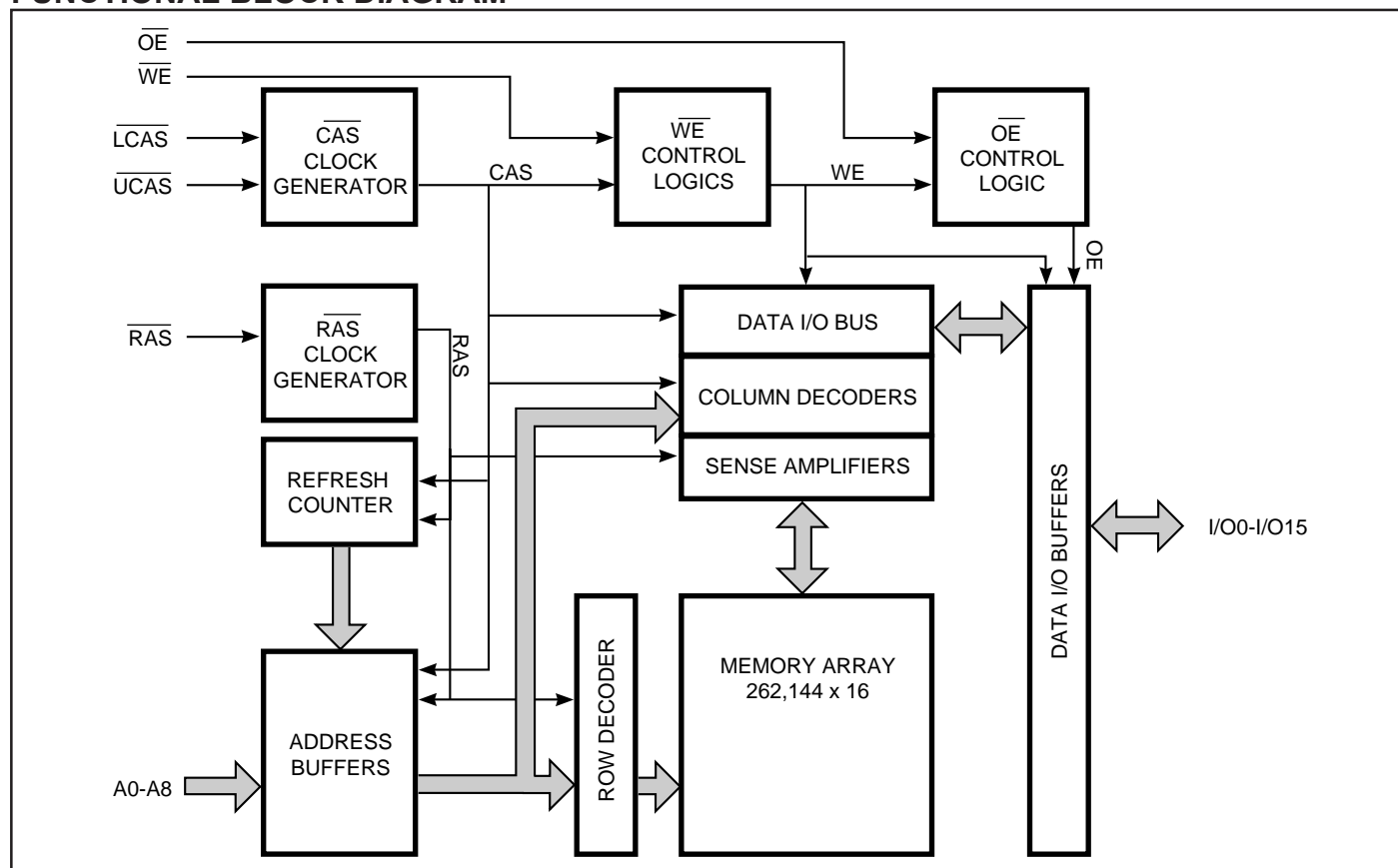
#### 40-Pin SOJ



### PIN DESCRIPTIONS

A0-A8	Address Inputs
I/O0-15	Data Inputs/Outputs
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{UCAS}}$	Upper Column Address Strobe
$\overline{\text{LCAS}}$	Lower Column Address Strobe
Vcc	Power
GND	Ground
NC	No Connection

## FUNCTIONAL BLOCK DIAGRAM



## TRUTH TABLE

Function		$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Address tr/tc	I/O
Standby		H	H	H	X	X	X	High-Z
Read: Word		L	L	L	H	L	ROW/COL	DOUT
Read: Lower Byte		L	L	H	H	L	ROW/COL	Lower Byte, DOUT Upper Byte, High-Z
Read: Upper Byte		L	H	L	H	L	ROW/COL	Lower Byte, High-Z Upper Byte, DOUT
Write: Word (Early Write)		L	L	L	L	X	ROW/COL	DIN
Write: Lower Byte (Early Write)		L	L	H	L	X	ROW/COL	Lower Byte, DIN Upper Byte, High-Z
Write: Upper Byte (Early Write)		L	H	L	L	X	ROW/COL	Lower Byte, High-Z Upper Byte, DIN
Read-Write <sup>(1,2)</sup>		L	L	L	H→L	L→H	ROW/COL	DOUT, DIN
EDO Page-Mode Read <sup>(2)</sup>	1st Cycle:	L	H→L	H→L	H	L	ROW/COL	DOUT
	2nd Cycle:	L	H→L	H→L	H	L	NA/COL	DOUT
	Any Cycle:	L	L→H	L→H	H	L	NA/NA	DOUT
EDO Page-Mode Write <sup>(1)</sup>	1st Cycle:	L	H→L	H→L	L	X	ROW/COL	DIN
	2nd Cycle:	L	H→L	H→L	L	X	NA/COL	DIN
EDO Page-Mode Read-Write <sup>(1,2)</sup>	1st Cycle:	L	H→L	H→L	H→L	L→H	ROW/COL	DOUT, DIN
	2nd Cycle:	L	H→L	H→L	H→L	L→H	NA/COL	DOUT, DIN
Hidden Refresh <sup>(2)</sup>	Read	L→H→L	L	L	H	L	ROW/COL	DOUT
	Write	L→H→L	L	L	L	X	ROW/COL	DOUT
RAS-Only Refresh		L	H	H	X	X	ROW/NA	High-Z
CBR Refresh <sup>(3)</sup>		H→L	L	L	X	X	X	High-Z

### Notes:

1. These WRITE cycles may also be BYTE WRITE cycles (either  $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$  active).
2. These READ cycles may also be BYTE READ cycles (either  $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$  active).
3. At least one of the two CAS signals must be active ( $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$ ).

## Functional Description

The IC41C16256 and IC41LV16256 is a CMOS DRAM optimized for high-speed bandwidth, low power applications. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits. These are entered 9 bits (A0-A8) at a time. The row address is latched by the Row Address Strobe ( $\overline{\text{RAS}}$ ). The column address is latched by the Column Address Strobe ( $\overline{\text{CAS}}$ ).

The IC41C16256 and IC41LV16256 has two  $\overline{\text{CAS}}$  controls,  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$ . The  $\overline{\text{LCAS}}$  and  $\overline{\text{UCAS}}$  inputs internally generates a CAS signal functioning in an identical manner to the single CAS input on the other 256K x 16 DRAMs. The key difference is that each CAS controls its corresponding I/O tristate logic (in conjunction with  $\overline{\text{OE}}$  and  $\overline{\text{WE}}$  and RAS).  $\overline{\text{LCAS}}$  controls I/O0 through I/O7 and  $\overline{\text{UCAS}}$  controls I/O8 through I/O15.

The IC41C16256 and IC41LV16256  $\overline{\text{CAS}}$  function is determined by the first  $\overline{\text{CAS}}$  ( $\overline{\text{LCAS}}$  or  $\overline{\text{UCAS}}$ ) transitioning LOW and the last transitioning back HIGH. The two CAS controls give the IC41C16256 both BYTE READ and BYTE WRITE cycle capabilities.

## Memory Cycle

A memory cycle is initiated by bring  $\overline{\text{RAS}}$  LOW and it is terminated by returning both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  HIGH. To ensure proper device operation and data integrity any memory cycle, once initiated, must not be ended or aborted before the minimum  $t_{\text{RAS}}$  time has expired. A new cycle must not be initiated until the minimum precharge time  $t_{\text{RP}}$ ,  $t_{\text{CP}}$  has elapsed.

## Read Cycle

A read cycle is initiated by the falling edge of  $\overline{\text{CAS}}$  or  $\overline{\text{OE}}$ , whichever occurs last, while holding  $\overline{\text{WE}}$  HIGH. The column address must be held for a minimum time specified by  $t_{\text{AR}}$ . Data Out becomes valid only when  $t_{\text{RAC}}$ ,  $t_{\text{AA}}$ ,  $t_{\text{CAC}}$  and  $t_{\text{OE}}$  are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters.

## Write Cycle

A write cycle is initiated by the falling edge of  $\overline{\text{CAS}}$  and  $\overline{\text{WE}}$ , whichever occurs last. The input data must be valid at or before the falling edge of  $\overline{\text{CAS}}$  or  $\overline{\text{WE}}$ , whichever occurs first.

## Refresh Cycle

To retain data, 512 refresh cycles are required in each 8 ms period. There are two ways to refresh the memory.

1. By clocking each of the 512 row addresses (A0 through A8) with  $\overline{\text{RAS}}$  at least once every 8 ms. Any read, write, read-modify-write or  $\overline{\text{RAS}}$ -only cycle refreshes the addressed row.
2. Using a  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle.  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh is activated by the falling edge of  $\overline{\text{RAS}}$ , while holding  $\overline{\text{CAS}}$  LOW. In  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle, an internal 9-bit counter provides the row addresses and the external address inputs are ignored.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  is a refresh-only mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle.

## Extended Data Out Page Mode

EDO page mode operation permits all 512 columns within a selected row to be randomly accessed at a high data rate.

In EDO page mode read cycle, the data-out is held to the next CAS cycle's falling edge, instead of the rising edge. For this reason, the valid data output time in EDO page mode is extended compared with the fast page mode. In the fast page mode, the valid data output time becomes shorter as the  $\overline{\text{CAS}}$  cycle time becomes shorter. Therefore, in EDO page mode, the timing margin in read cycle is larger than that of the fast page mode even if the CAS cycle time becomes shorter.

In EDO page mode, due to the extended data function, the CAS cycle time can be shorter than in the fast page mode if the timing margin is the same.

The EDO page mode allows both read and write operations during one  $\overline{\text{RAS}}$  cycle, but the performance is equivalent to that of the fast page mode in that case.

## Power-On

After application of the  $V_{\text{CC}}$  supply, an initial pause of 200  $\mu\text{s}$  is required followed by a minimum of eight initialization cycles (any combination of cycles containing a  $\overline{\text{RAS}}$  signal).

During power-on, it is recommended that  $\overline{\text{RAS}}$  track with  $V_{\text{CC}}$  or be held at a valid  $V_{\text{IH}}$  to avoid current surges.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameters		Rating	Unit
V <sub>T</sub>	Voltage on Any Pin Relative to GND	5V	–1.0 to +7.0	V
		3.3V	–0.5 to +4.6	
V <sub>CC</sub>	Supply Voltage	5V	–1.0 to +7.0	V
		3.3V	–0.5 to +4.6	
I <sub>OUT</sub>	Output Current		50	mA
P <sub>D</sub>	Power Dissipation		1	W
T <sub>A</sub>	Commercial Operation Temperature		0 to +70	°C
	Industrial Operating Temperature		–40 to +85	°C
T <sub>STG</sub>	Storage Temperature		–55 to +125	°C

### Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND.)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	5V	4.5	5.0	5.5	V
		3.3V	3.0	3.3	3.6	
V <sub>IH</sub>	Input High Voltage	5V	2.4	—	V <sub>CC</sub> + 1.0	V
		3.3V	2.0	—	V <sub>CC</sub> + 0.3	
V <sub>IL</sub>	Input Low Voltage	5V	–1.0	—	0.8	V
		3.3V	–0.3	—	0.8	
T <sub>A</sub>	Commercial Ambient Temperature		0	—	70	°C
	Industrial Ambient Temperature		–40	—	85	°C

## CAPACITANCE<sup>(1,2)</sup>

Symbol	Parameter	Max.	Unit
C <sub>IN1</sub>	Input Capacitance: A0-A8	5	pF
C <sub>IN2</sub>	Input Capacitance: RAS, UCAS, LCAS, WE, OE	7	pF
C <sub>IO</sub>	Data Input/Output Capacitance: I/O0-I/O15	7	pF

### Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz.

## ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed	Min.	Max.	Unit
I <sub>IL</sub>	Input Leakage Current	Any input 0V < V <sub>IN</sub> < V <sub>CC</sub> Other inputs not under test = 0V		-10	10	μA
I <sub>IO</sub>	Output Leakage Current	Output is disabled (Hi-Z) 0V < V <sub>OUT</sub> < V <sub>CC</sub>		-10	10	μA
V <sub>OH</sub>	Output High Voltage Level	I <sub>OH</sub> = -2.5 mA		2.4	—	V
V <sub>OL</sub>	Output Low Voltage Level	I <sub>OL</sub> = +2.1 mA		—	0.4	V
I <sub>CC1</sub>	Standby Current: TTL	$\overline{\text{RAS}}, \overline{\text{LCAS}}, \overline{\text{UCAS}} > V_{IH}$	Commerical 5V Industrial 5V Commerical 3.3V Industrial 3.3V	— — — —	2 3 1 2	mA
I <sub>CC2</sub>	Standby Current: CMOS	$\overline{\text{RAS}}, \overline{\text{LCAS}}, \overline{\text{UCAS}} > V_{CC} - 0.2V$	5V 3.3V	— —	1 0.5	mA
I <sub>CC3</sub>	Operating Current: Random Read/Write <sup>(2,3,4)</sup> Average Power Supply Current	$\overline{\text{RAS}}, \overline{\text{LCAS}}, \overline{\text{UCAS}}$ , Address Cycling, t <sub>RC</sub> = t <sub>RC</sub> (min.)	-25 -35 -50 -60	— — — —	260 230 180 170	mA
I <sub>CC4</sub>	Operating Current: EDO Page Mode <sup>(2,3,4)</sup> Average Power Supply Current	$\overline{\text{RAS}} = V_{IL}, \overline{\text{LCAS}}, \overline{\text{UCAS}}$ , Cycling t <sub>PC</sub> = t <sub>PC</sub> (min.)	-25 -35 -50 -60	— — — —	250 220 170 160	mA
I <sub>CC5</sub>	Refresh Current: $\overline{\text{RAS}}$ -Only <sup>(2,3)</sup> Average Power Supply Current	$\overline{\text{RAS}}$ Cycling, $\overline{\text{LCAS}}, \overline{\text{UCAS}} > V_{IH}$ t <sub>RC</sub> = t <sub>RC</sub> (min.)	-25 -35 -50 -60	— — — —	260 230 180 170	mA
I <sub>CC6</sub>	Refresh Current: CBR <sup>(2,3,5)</sup> Average Power Supply Current	$\overline{\text{RAS}}, \overline{\text{LCAS}}, \overline{\text{UCAS}}$ Cycling t <sub>RC</sub> = t <sub>RC</sub> (min.)	-25 -35 -50 -60	— — — —	260 230 180 170	mA

### Notes:

1. An initial pause of 200 μs is required after power-up followed by eight  $\overline{\text{RAS}}$  refresh cycles ( $\overline{\text{RAS}}$ -Only or CBR) before proper device operation is assured. The eight  $\overline{\text{RAS}}$  cycles wake-up should be repeated any time the t<sub>REF</sub> refresh requirement is exceeded.
2. Dependent on cycle rates.
3. Specified values are obtained with minimum cycle time and the output open.
4. Column-address is changed once each EDO page cycle.
5. Enables on-chip refresh and address counters.

## AC CHARACTERISTICS<sup>(1,2,3,4,5,6)</sup>

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-25		-35		-50		-60		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Random READ or WRITE Cycle Time	45	—	60	—	90	—	110	—	ns
t <sub>RAC</sub>	Access Time from $\overline{\text{RAS}}^{(6, 7)}$	—	25	—	35	—	50	—	60	ns
t <sub>CAC</sub>	Access Time from $\overline{\text{CAS}}^{(6, 8, 15)}$	—	8	—	10	—	14	—	15	ns
t <sub>AA</sub>	Access Time from Column-Address <sup>(6)</sup>	—	12	—	18	—	25	—	30	ns
t <sub>RAS</sub>	$\overline{\text{RAS}}$ Pulse Width	25	10K	35	10K	50	10K	60	10K	ns
t <sub>RP</sub>	$\overline{\text{RAS}}$ Precharge Time	15	—	20	—	30	—	40	—	ns
t <sub>CAS</sub>	$\overline{\text{CAS}}$ Pulse Width <sup>(26)</sup>	4	10K	6	10K	8	10K	10	10K	ns
t <sub>CP</sub>	$\overline{\text{CAS}}$ Precharge Time <sup>(9, 25)</sup>	4	—	5	—	8	—	10	—	ns
t <sub>CSH</sub>	$\overline{\text{CAS}}$ Hold Time <sup>(21)</sup>	25	—	35	—	50	—	60	—	ns
t <sub>RCD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time <sup>(10, 20)</sup>	10	17	11	28	19	36	20	45	ns
t <sub>ASR</sub>	Row-Address Setup Time	0	—	0	—	0	—	0	—	ns
t <sub>RAH</sub>	Row-Address Hold Time	6	—	6	—	8	—	10	—	ns
t <sub>ASC</sub>	Column-Address Setup Time <sup>(20)</sup>	0	—	0	—	0	—	0	—	ns
t <sub>CAH</sub>	Column-Address Hold Time <sup>(20)</sup>	5	—	6	—	8	—	10	—	ns
t <sub>AR</sub>	Column-Address Hold Time (referenced to $\overline{\text{RAS}}$ )	19	—	30	—	40	—	40	—	ns
t <sub>RAD</sub>	$\overline{\text{RAS}}$ to Column-Address Delay Time <sup>(11)</sup>	8	20	10	20	14	25	15	30	ns
t <sub>RAL</sub>	Column-Address to $\overline{\text{RAS}}$ Lead Time	12	—	18	—	25	—	30	—	ns
t <sub>RPC</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	0	—	0	—	0	—	0	—	ns
t <sub>RSH</sub>	$\overline{\text{RAS}}$ Hold Time <sup>(27)</sup>	7	—	8	—	14	—	15	—	ns
t <sub>CLZ</sub>	$\overline{\text{CAS}}$ to Output in Low-Z <sup>(15, 29)</sup>	3	—	3	—	3	—	3	—	ns
t <sub>CRP</sub>	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time <sup>(21)</sup>	5	—	5	—	5	—	5	—	ns
t <sub>OD</sub>	Output Disable Time <sup>(19, 28, 29)</sup>	2	12	3	12	3	12	3	12	ns
t <sub>OE</sub>	Output Enable Time <sup>(15, 16)</sup>	0	8	0	10	0	15	—	15	ns
t <sub>OEHC</sub>	$\overline{\text{OE}}$ HIGH Hold Time from $\overline{\text{CAS}}$ HIGH	10	—	10	—	10	—	10	—	ns
t <sub>OEP</sub>	$\overline{\text{OE}}$ HIGH Pulse Width	10	—	10	—	10	—	10	—	ns
t <sub>OES</sub>	$\overline{\text{OE}}$ LOW to $\overline{\text{CAS}}$ HIGH Setup Time	5	—	5	—	5	—	5	—	ns
t <sub>RCS</sub>	Read Command Setup Time <sup>(17, 20)</sup>	0	—	0	—	0	—	0	—	ns
t <sub>RRH</sub>	Read Command Hold Time (referenced to $\overline{\text{RAS}}$ ) <sup>(12)</sup>	0	—	0	—	0	—	0	—	ns
t <sub>RCH</sub>	Read Command Hold Time (referenced to $\overline{\text{CAS}}$ ) <sup>(12, 17, 21)</sup>	0	—	0	—	0	—	0	—	ns
t <sub>WCH</sub>	Write Command Hold Time <sup>(17, 27)</sup>	5	—	5	—	8	—	10	—	ns
t <sub>WCR</sub>	Write Command Hold Time (referenced to $\overline{\text{RAS}}$ ) <sup>(17)</sup>	19	—	30	—	40	—	50	—	ns
t <sub>WP</sub>	Write Command Pulse Width <sup>(17)</sup>	5	—	5	—	8	—	10	—	ns
t <sub>WPZ</sub>	$\overline{\text{WE}}$ Pulse Widths to Disable Outputs	10	—	10	—	10	—	10	—	ns
t <sub>RWL</sub>	Write Command to $\overline{\text{RAS}}$ Lead Time <sup>(17)</sup>	7	—	8	—	14	—	15	—	ns
t <sub>CWL</sub>	Write Command to $\overline{\text{CAS}}$ Lead Time <sup>(17, 21)</sup>	5	—	8	—	14	—	15	—	ns
t <sub>WCS</sub>	Write Command Setup Time <sup>(14, 17, 20)</sup>	0	—	0	—	0	—	0	—	ns
t <sub>DHR</sub>	Data-in Hold Time (referenced to $\overline{\text{RAS}}$ )	19	—	30	—	40	—	40	—	ns



## AC CHARACTERISTICS (Continued)<sup>(1,2,3,4,5,6)</sup>

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-25		-35		-50		-60		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>ACH</sub>	Column-Address Setup Time to $\overline{\text{CAS}}$ Precharge during WRITE Cycle	15	—	15	—	15	—	15	—	ns
t <sub>OE</sub>	OE Hold Time from $\overline{\text{WE}}$ during READ-MODIFY-WRITE cycle <sup>(18)</sup>	5	—	8	—	10	—	15	—	ns
t <sub>DS</sub>	Data-In Setup Time <sup>(15, 22)</sup>	0	—	0	—	0	—	0	—	ns
t <sub>DH</sub>	Data-In Hold Time <sup>(15, 22)</sup>	5	—	6	—	8	—	10	—	ns
t <sub>RWC</sub>	READ-MODIFY-WRITE Cycle Time	65	—	80	—	125	—	140	—	ns
t <sub>RWD</sub>	RAS to $\overline{\text{WE}}$ Delay Time during READ-MODIFY-WRITE Cycle <sup>(14)</sup>	35	—	45	—	70	—	80	—	ns
t <sub>CWD</sub>	CAS to $\overline{\text{WE}}$ Delay Time <sup>(14, 20)</sup>	17	—	25	—	34	—	36	—	ns
t <sub>AWD</sub>	Column-Address to $\overline{\text{WE}}$ Delay Time <sup>(14)</sup>	21	—	30	—	42	—	49	—	ns
t <sub>PC</sub>	EDO Page Mode READ or WRITE Cycle Time <sup>(24)</sup>	10	—	12	—	20	—	25	—	ns
t <sub>RASP</sub>	RAS Pulse Width in EDO Page Mode	25	100K	35	100K	50	100K	50	100K	ns
t <sub>CPA</sub>	Access Time from $\overline{\text{CAS}}$ Precharge <sup>(15)</sup>	—	14	—	21	—	27	—	34	ns
t <sub>PRWC</sub>	EDO Page Mode READ-WRITE Cycle Time <sup>(24)</sup>	32	—	40	—	47	—	56	—	ns
t <sub>COH</sub>	Data Output Hold after $\overline{\text{CAS}}$ LOW	5	—	5	—	5	—	5	—	ns
t <sub>OFF</sub>	Output Buffer Turn-Off Delay from $\overline{\text{CAS}}$ or RAS <sup>(13,15,19, 29)</sup>	3	15	3	15	3	15	3	15	ns
t <sub>WHZ</sub>	Output Disable Delay from $\overline{\text{WE}}$	3	15	3	15	3	15	3	15	ns
t <sub>CLCH</sub>	Last $\overline{\text{CAS}}$ going LOW to First $\overline{\text{CAS}}$ returning HIGH <sup>(23)</sup>	10	—	10	—	10	—	10	—	ns
t <sub>CSR</sub>	CAS Setup Time (CBR REFRESH) <sup>(30, 20)</sup>	5	—	8	—	10	—	10	—	ns
t <sub>CHR</sub>	CAS Hold Time (CBR REFRESH) <sup>(30, 21)</sup>	7	—	8	—	10	—	10	—	ns
t <sub>ORD</sub>	OE Setup Time prior to RAS during HIDDEN REFRESH Cycle	0	—	0	—	0	—	0	—	ns
t <sub>REF</sub>	Refresh Period (512 Cycles)	—	8	—	8	8	—	8	—	ms
t <sub>tr</sub>	Transition Time (Rise or Fall) <sup>(2, 3)</sup>	1	50	1	50	1	50	1	50	ns

## AC TEST CONDITIONS

Output load: Two TTL Loads and 50 pF ( $V_{CC} = 5.0V \pm 10\%$ )  
One TTL Load and 50 pF ( $V_{CC} = 3.3V \pm 10\%$ )

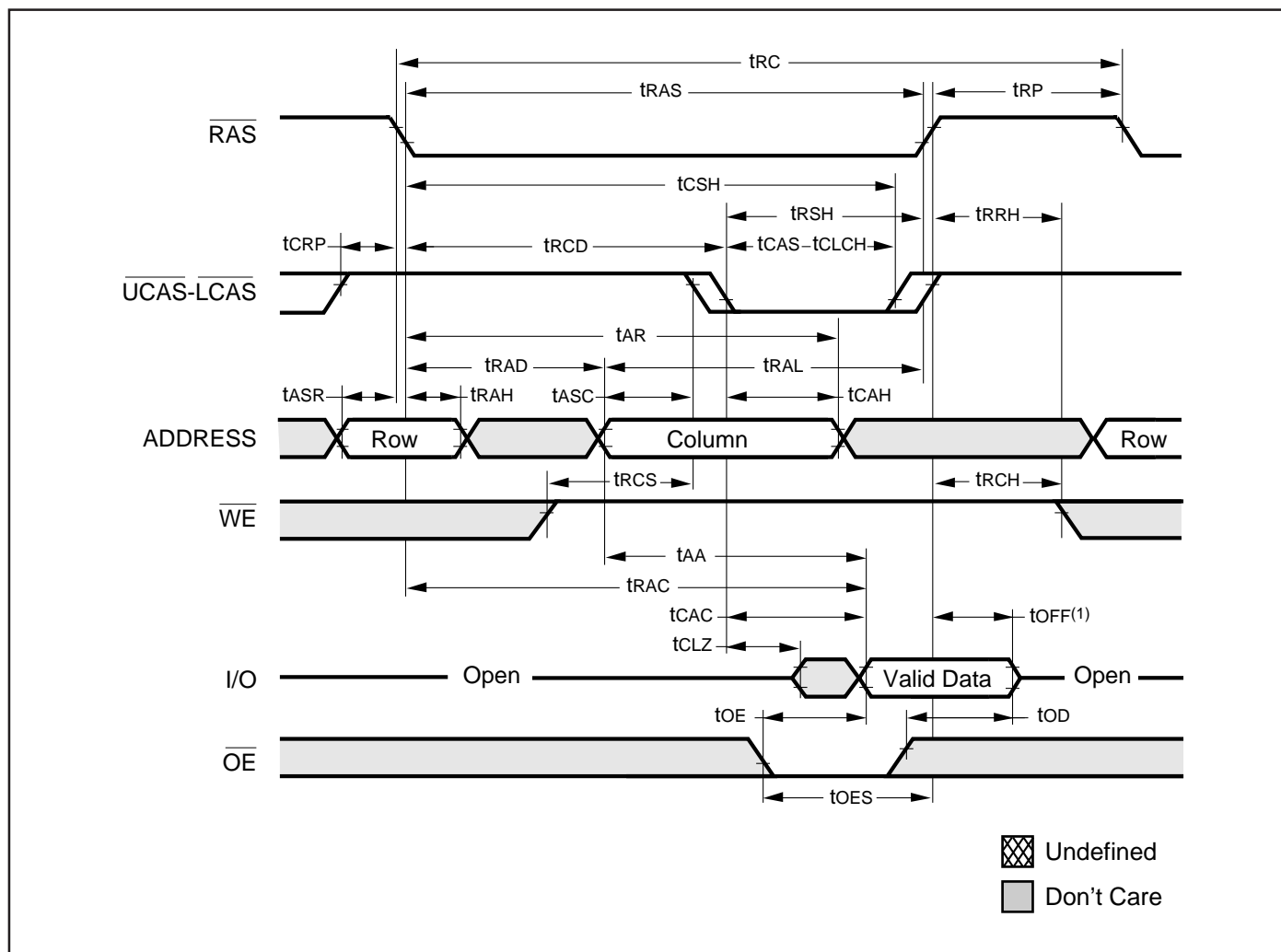
Input timing reference levels:  $V_{IH} = 2.4V$ ,  $V_{IL} = 0.8V$  ( $V_{CC} = 5.0V \pm 10\%$ );  
 $V_{IH} = 2.0V$ ,  $V_{IL} = 0.8V$  ( $V_{CC} = 3.3V \pm 10\%$ )

Output timing reference levels:  $V_{OH} = 2.0V$ ,  $V_{OL} = 0.8V$  ( $V_{CC} = 5V \pm 10\%$ ,  $3.3V \pm 10\%$ )

**Notes:**

1. An initial pause of 200  $\mu$ s is required after power-up followed by eight  $\overline{\text{RAS}}$  refresh cycle ( $\overline{\text{RAS}}$ -Only or CBR) before proper device operation is assured. The eight  $\overline{\text{RAS}}$  cycles wake-up should be repeated any time the  $t_{\text{REF}}$  refresh requirement is exceeded.
2.  $V_{\text{IH}}$  (MIN) and  $V_{\text{IL}}$  (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between  $V_{\text{IH}}$  and  $V_{\text{IL}}$  (or between  $V_{\text{IL}}$  and  $V_{\text{IH}}$ ) and assume to be 1 ns for all inputs.
3. In addition to meeting the transition rate specification, all input signals must transit between  $V_{\text{IH}}$  and  $V_{\text{IL}}$  (or between  $V_{\text{IL}}$  and  $V_{\text{IH}}$ ) in a monotonic manner.
4. If  $\text{CAS}$  and  $\overline{\text{RAS}} = V_{\text{IH}}$ , data output is High-Z.
5. If  $\text{CAS} = V_{\text{IL}}$ , data output may contain data from the last valid READ cycle.
6. Measured with a load equivalent to one TTL gate and 50 pF.
7. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{MAX})$ . If  $t_{\text{RCD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  will increase by the amount that  $t_{\text{RCD}}$  exceeds the value shown.
8. Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{MAX})$ .
9. If  $\text{CAS}$  is LOW at the falling edge of  $\overline{\text{RAS}}$ , data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer,  $\text{CAS}$  and  $\overline{\text{RAS}}$  must be pulsed for  $t_{\text{CP}}$ .
10. Operation with the  $t_{\text{RCD}} (\text{MAX})$  limit ensures that  $t_{\text{RAC}} (\text{MAX})$  can be met.  $t_{\text{RCD}} (\text{MAX})$  is specified as a reference point only; if  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}} (\text{MAX})$  limit, access time is controlled exclusively by  $t_{\text{CAC}}$ .
11. Operation within the  $t_{\text{RAD}} (\text{MAX})$  limit ensures that  $t_{\text{RCD}} (\text{MAX})$  can be met.  $t_{\text{RAD}} (\text{MAX})$  is specified as a reference point only; if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}} (\text{MAX})$  limit, access time is controlled exclusively by  $t_{\text{AA}}$ .
12. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a READ cycle.
13.  $t_{\text{OFF}} (\text{MAX})$  defines the time at which the output achieves the open circuit condition; it is not a reference to  $V_{\text{OH}}$  or  $V_{\text{OL}}$ .
14.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CWD}}$  are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If  $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{MIN})$ , the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If  $t_{\text{RWD}} \geq t_{\text{RWD}} (\text{MIN})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{MIN})$  and  $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{MIN})$ , the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until  $\text{CAS}$  and  $\overline{\text{RAS}}$  or  $\overline{\text{OE}}$  go back to  $V_{\text{IH}}$ ) is indeterminate.  $\overline{\text{OE}}$  held HIGH and  $\overline{\text{WE}}$  taken LOW after  $\overline{\text{CAS}}$  goes LOW result in a LATE WRITE ( $\overline{\text{OE}}$ -controlled) cycle.
15. Output parameter (I/O) is referenced to corresponding  $\text{CAS}$  input, I/O0-I/O7 by  $\overline{\text{LCAS}}$  and I/O8-I/O15 by  $\overline{\text{UCAS}}$ .
16. During a READ cycle, if  $\overline{\text{OE}}$  is LOW then taken HIGH before  $\overline{\text{CAS}}$  goes HIGH, I/O goes open. If  $\overline{\text{OE}}$  is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
17. Write command is defined as  $\overline{\text{WE}}$  going low.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both  $t_{\text{OD}}$  and  $t_{\text{OEH}}$  met ( $\overline{\text{OE}}$  HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if  $\overline{\text{CAS}}$  remains LOW and  $\overline{\text{OE}}$  is taken back to LOW after  $t_{\text{OEH}}$  is met.
19. The I/Os are in open during READ cycles once  $t_{\text{OD}}$  or  $t_{\text{OFF}}$  occur.
20. The first  $\chi\overline{\text{CAS}}$  edge to transition LOW.
21. The last  $\chi\overline{\text{CAS}}$  edge to transition HIGH.
22. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in EARLY WRITE cycles and  $\overline{\text{WE}}$  leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. Last falling  $\chi\overline{\text{CAS}}$  edge to first rising  $\chi\overline{\text{CAS}}$  edge.
24. Last rising  $\chi\overline{\text{CAS}}$  edge to next cycle's last rising  $\chi\overline{\text{CAS}}$  edge.
25. Last rising  $\chi\overline{\text{CAS}}$  edge to first falling  $\chi\overline{\text{CAS}}$  edge.
26. Each  $\chi\overline{\text{CAS}}$  must meet minimum pulse width.
27. Last  $\chi\overline{\text{CAS}}$  to go LOW.
28. I/Os controlled, regardless  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ .
29. The 3 ns minimum is a parameter guaranteed by design.
30. Enables on-chip refresh and address counters.

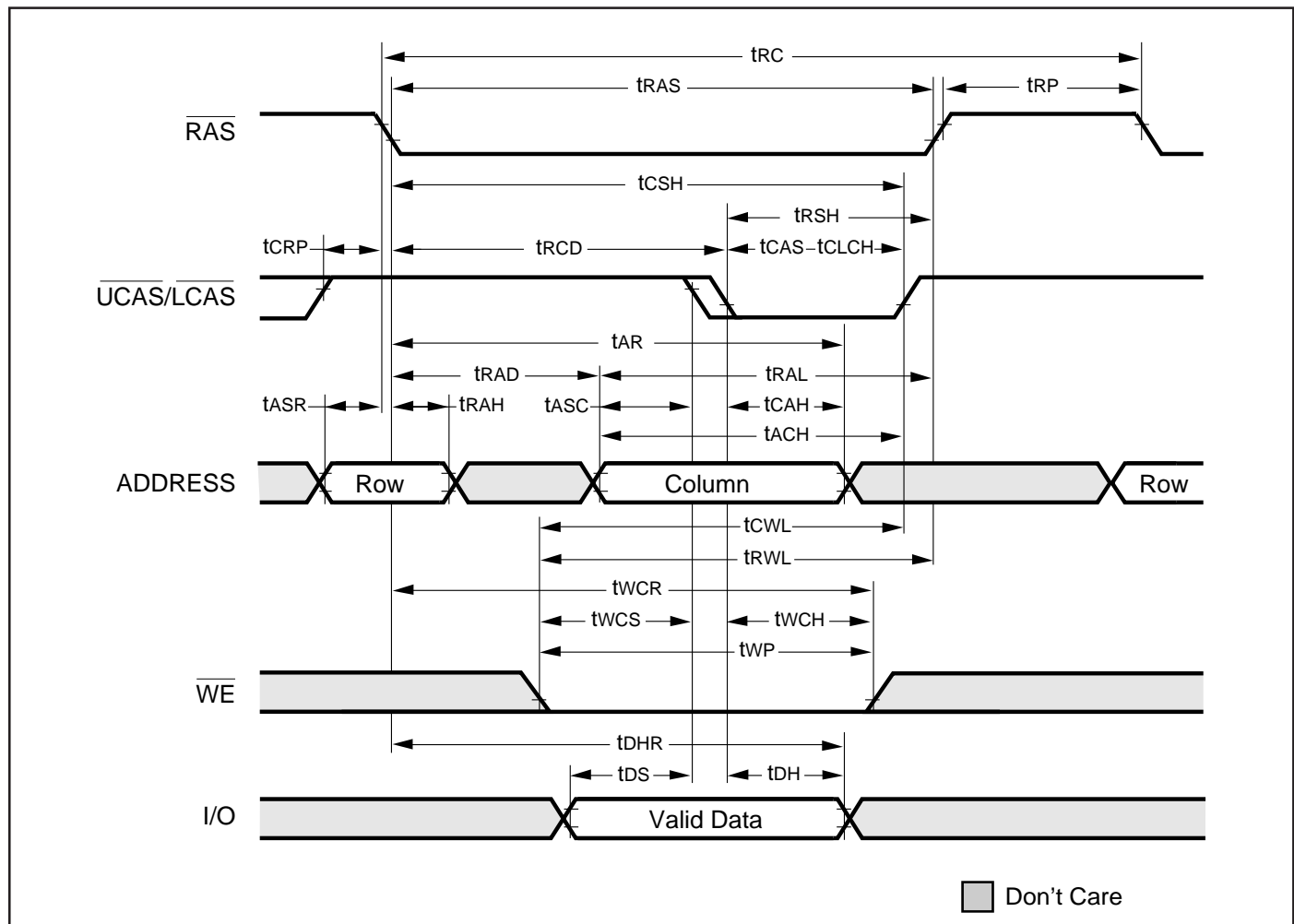
## READ CYCLE



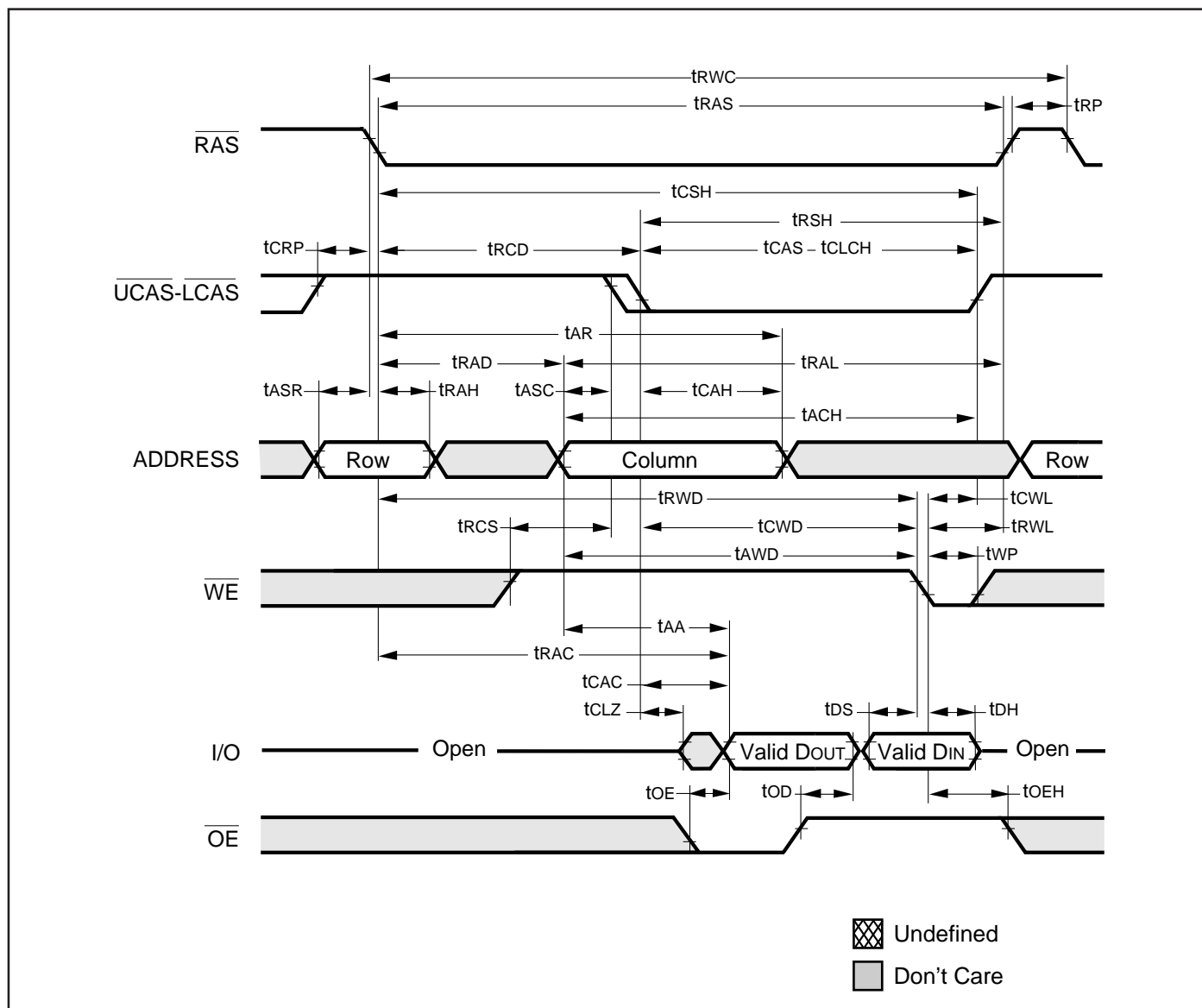
### Note:

1.  $t_{\text{OFF}}$  is referenced from rising edge of  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$ , whichever occurs last.

**EARLY WRITE CYCLE** ( $\overline{OE}$  = DON'T CARE)



# READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)



The diagram illustrates the timing relationships for a 2D DRAM array. The signals and their timing parameters are as follows:

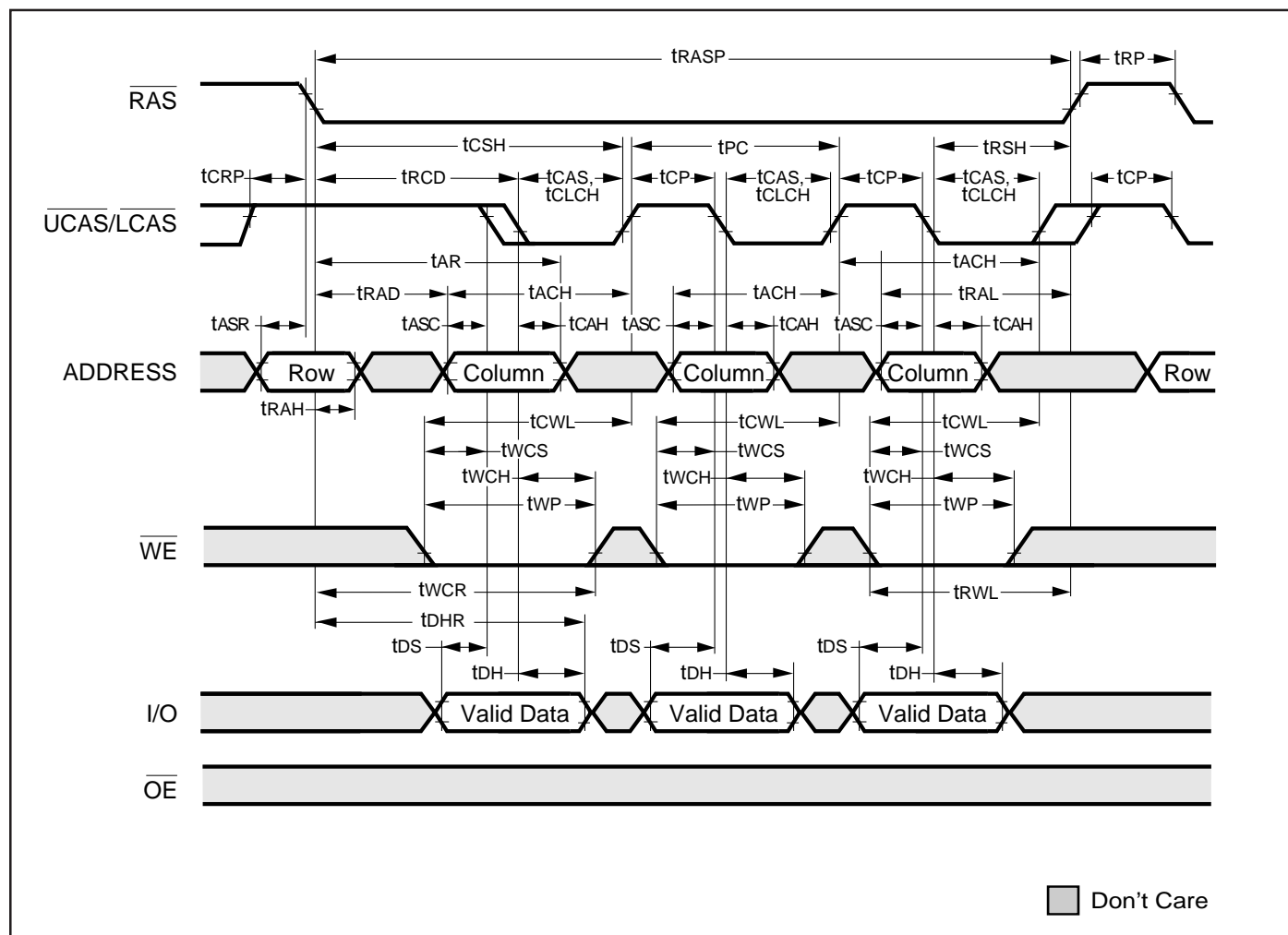
- RAS:**  $t_{RASP}$  (RAS pulse width),  $t_{TRP}$  (RAS precharge time).
- UCAS/LCAS:**  $t_{CRP}$  (UCAS/LCAS precharge time),  $t_{RCD}$  (RAS to UCAS/LCAS delay),  $t_{CAS}$ ,  $t_{CLCH}$  (CAS to UCAS/LCAS delay),  $t_{PC(1)}$  (UCAS/LCAS precharge time),  $t_{RSH}$  (UCAS/LCAS to RAS delay),  $t_{CP}$  (UCAS/LCAS to RAS delay).
- ADDRESS:**  $t_{AR}$  (ADDRESS precharge time),  $t_{RAD}$  (ADDRESS to RAS delay),  $t_{ASR}$  (ADDRESS to RAS delay),  $t_{ASC}$  (ADDRESS to RAS delay),  $t_{CAH}$  (ADDRESS to RAS delay),  $t_{ASC}$  (ADDRESS to RAS delay),  $t_{CAH}$  (ADDRESS to RAS delay),  $t_{ASC}$  (ADDRESS to RAS delay),  $t_{CAH}$  (ADDRESS to RAS delay),  $t_{RAH}$  (ADDRESS to RAS delay),  $t_{RCS}$  (ADDRESS to RAS delay),  $t_{RCH}$  (ADDRESS to RAS delay),  $t_{RRH}$  (ADDRESS to RAS delay).
- WE:**  $t_{AA}$  (WE to ADDRESS delay),  $t_{AC}$  (WE to ADDRESS delay),  $t_{CLZ}$  (WE to ADDRESS delay),  $t_{TOFF}$  (WE to ADDRESS delay).
- I/O:**  $t_{OE}$  (I/O to ADDRESS delay),  $t_{OES}$  (I/O to ADDRESS delay),  $t_{OD}$  (I/O to ADDRESS delay),  $t_{OEH}$  (I/O to ADDRESS delay),  $t_{OEP}$  (I/O to ADDRESS delay).
- OE:**  $t_{OE}$  (OE to ADDRESS delay),  $t_{OES}$  (OE to ADDRESS delay),  $t_{OD}$  (OE to ADDRESS delay),  $t_{OEH}$  (OE to ADDRESS delay),  $t_{OEP}$  (OE to ADDRESS delay).

Legend:

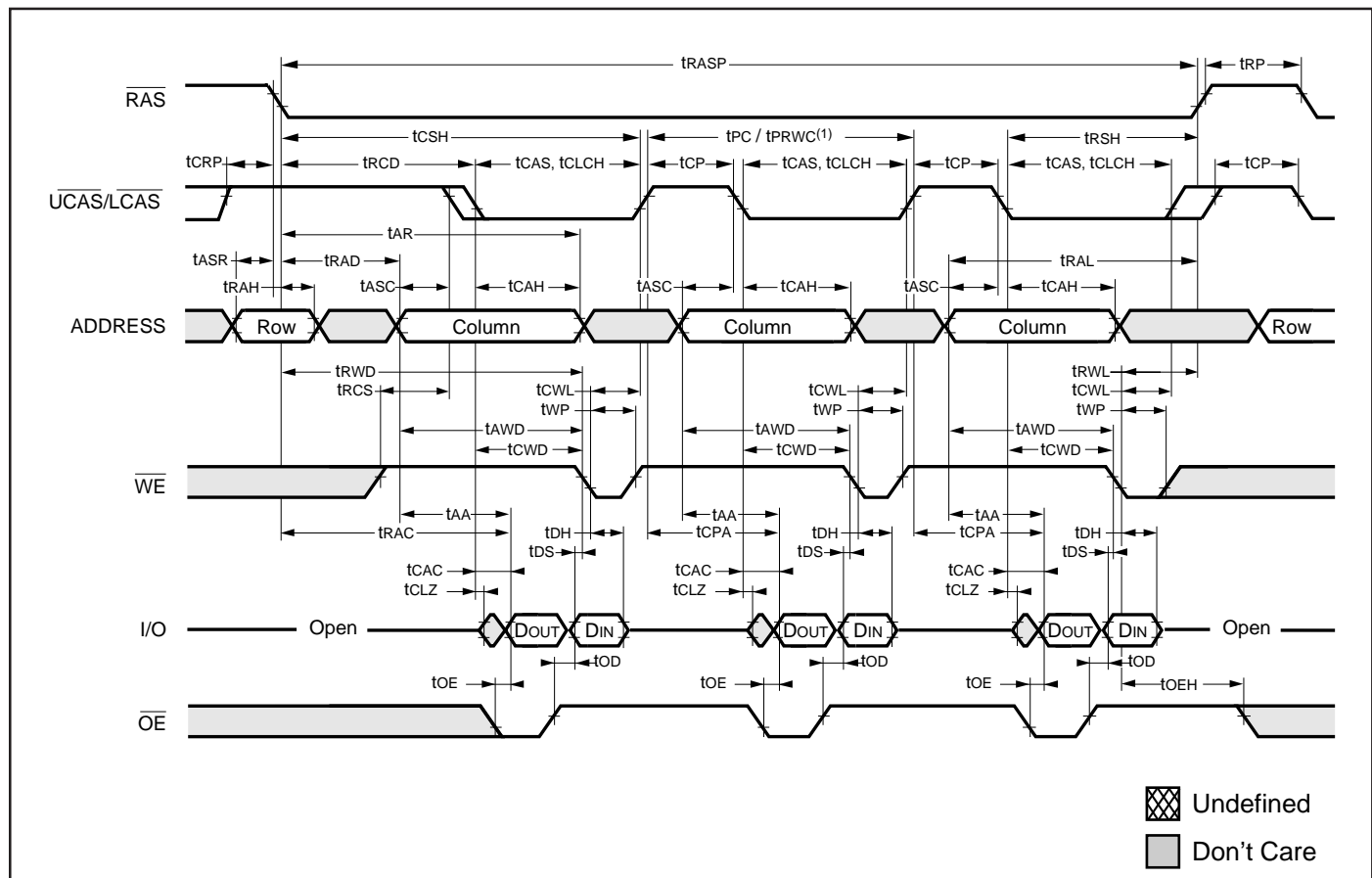
- Undefined (hatched box)
- Don't Care (gray box)

DR018-0B 12/18/2001

## EDO-PAGE-MODE EARLY-WRITE CYCLE



## EDO-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY WRITE Cycles)



### Note:

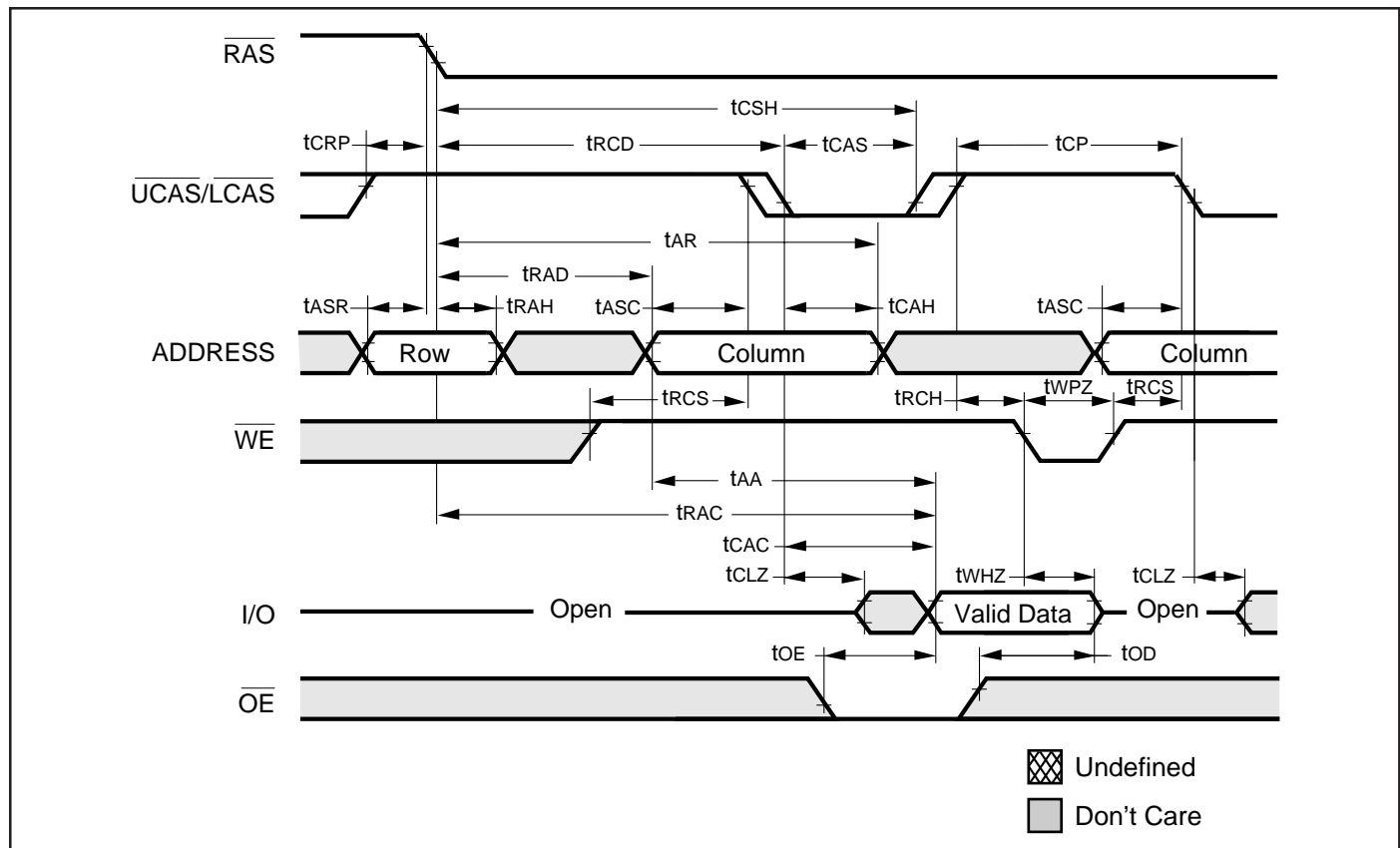
1.  $t_{PC}$  is for LATE write cycles only.  $t_{PC}$  can be measured from falling edge of  $\overline{CAS}$  to falling edge of  $\overline{CAS}$ , or from rising edge of  $\overline{CAS}$  to rising edge of  $\overline{CAS}$ . Both measurements must meet the  $t_{PC}$  specifications.



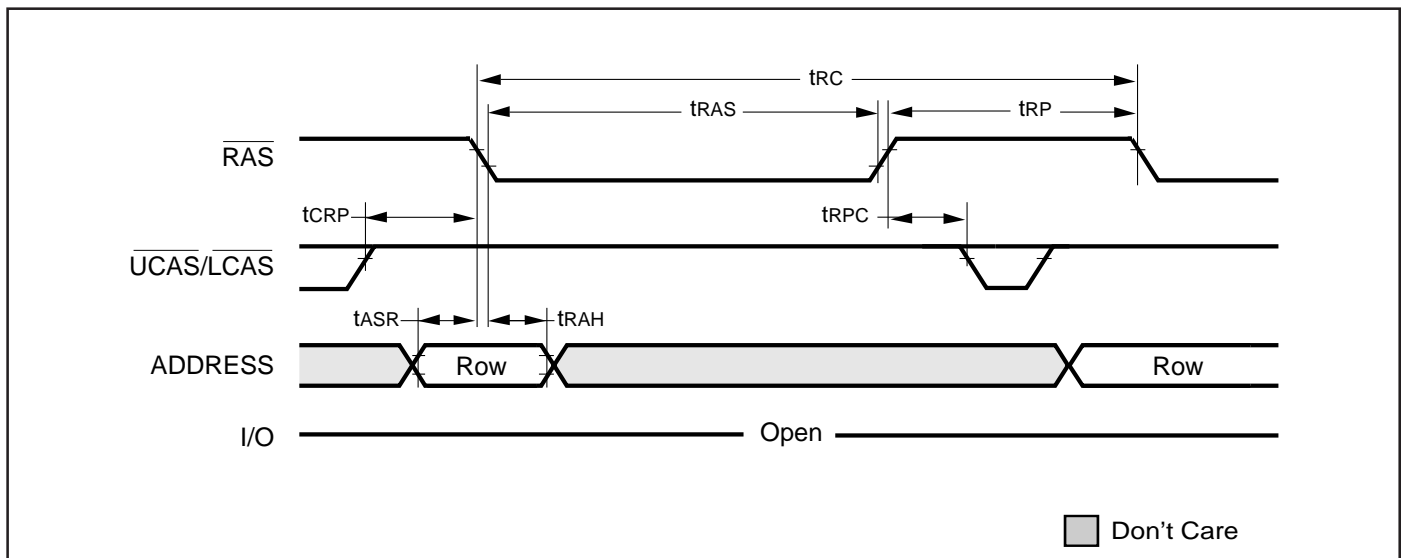
[illegible]

## AC WAVEFORMS

### READ CYCLE (With $\overline{WE}$ -Controlled Disable)



### RAS-ONLY REFRESH CYCLE ( $\overline{OE}$ , $\overline{WE}$ = DON'T CARE)



The diagram shows the timing relationships between three signals:  $\overline{\text{RAS}}$ ,  $\overline{\text{UCAS/LCAS}}$ , and I/O. The I/O signal is a single horizontal line labeled "Open". The  $\overline{\text{RAS}}$  signal is a square wave that transitions from high to low and back to high. The  $\overline{\text{UCAS/LCAS}}$  signal is a square wave that transitions from low to high and back to low. The timing parameters are defined as follows:

- $t_{RP}$ : RAS pulse width (time from  $\overline{\text{RAS}}$  falling edge to rising edge).
- $t_{RAS}$ : RAS access time (time from  $\overline{\text{RAS}}$  falling edge to data valid).
- $t_{RPC}$ : RAS to column address setup time (time from  $\overline{\text{RAS}}$  falling edge to  $\overline{\text{UCAS/LCAS}}$  falling edge).
- $t_{CP}$ : Column address pulse width (time from  $\overline{\text{UCAS/LCAS}}$  falling edge to rising edge).
- $t_{CHR}$ : RAS to column address hold time (time from  $\overline{\text{UCAS/LCAS}}$  rising edge to  $\overline{\text{RAS}}$  rising edge).
- $t_{CSR}$ : RAS to column address setup time (time from  $\overline{\text{RAS}}$  falling edge to  $\overline{\text{UCAS/LCAS}}$  falling edge).

Timing diagram for a 16M16000 1T1R DRAM. The diagram illustrates the relationship between RAS, UCAS/LCAS, ADDRESS, I/O, and OE signals over time. Key timing parameters are labeled:  $t_{RAS}$ ,  $t_{RP}$ ,  $t_{RC}$ ,  $t_{RCD}$ ,  $t_{RSH}$ ,  $t_{CHR}$ ,  $t_{AR}$ ,  $t_{RAD}$ ,  $t_{RAH}$ ,  $t_{ASC}$ ,  $t_{AL}$ ,  $t_{CAH}$ ,  $t_{AA}$ ,  $t_{AC}$ ,  $t_{CAC}$ ,  $t_{CLZ}$ ,  $t_{OE}$ ,  $t_{ORD}$ ,  $t_{OD}$ , and  $t_{OFF(2)}$ . The ADDRESS bus shows Row and Column phases. The I/O bus shows Open and Valid Data states. The OE signal is active-low. A legend indicates that cross-hatched areas are 'Undefined' and grey areas are 'Don't Care'.

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**ORDERING INFORMATION**

**IC41C16256**

**Commercial Range: 0°C to 70°C**

Speed (ns)	Order Part No.	Package
25	IC41C16256-25K	400mil SOJ
	IC41C16256-25T	400mil TSOP-2
35	IC41C16256-35K	400mil SOJ
	IC41C16256-35T	400mil TSOP-2
50	IC41C16256-50K	400mil SOJ
	IC41C16256-50T	400mil TSOP-2
60	IC41C16256-60K	400mil SOJ
	IC41C16256-60T	400mil TSOP-2

**Industrial Range: -40°C to 85°C**

Speed (ns)	Order Part No.	Package
25	IC41C16256-25KI	400mil SOJ
	IC41C16256-25TI	400mil TSOP-2
35	IC41C16256-35KI	400mil SOJ
	IC41C16256-35TI	400mil TSOP-2
50	IC41C16256-50KI	400mil SOJ
	IC41C16256-50TI	400mil TSOP-2
60	IC41C16256-60KI	400mil SOJ
	IC41C16256-60TI	400mil TSOP-2

**ORDERING INFORMATION:**

**IC41LV16256**

**Commercial Range: 0°C to 70°C**

Speed (ns)	Order Part No.	Package
35	IC41LV16256-35K	400mil SOJ
	IC41LV16256-35T	400mil TSOP-2
50	IC41LV16256-50K	400mil SOJ
	IC41LV16256-50T	400mil TSOP-2
60	IC41LV16256-60K	400mil SOJ
	IC41LV16256-60T	400mil TSOP-2

**Industrial Range: -40°C to 85°C**

Speed (ns)	Order Part No.	Package
35	IC41LV16256-35K	400mil SOJ
	IC41LV16256-35T	400mil TSOP-2
50	IC41LV16256-50KI	400mil SOJ
	IC41LV16256-50TI	400mil TSOP-2
60	IC41LV16256-60KI	400mil SOJ
	IC41LV16256-60TI	400mil TSOP-2



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