

RMPA61810

Single Channel 6-18 GHz 1 Watt Power Amplifier MMIC

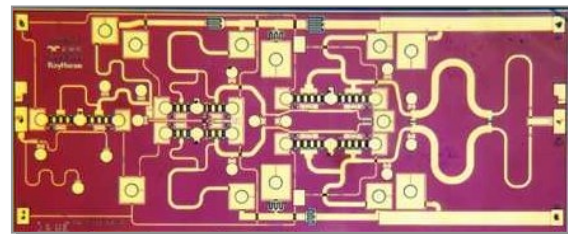
PRELIMINARY INFORMATION

Description

The Raytheon RMPA61810 is a fully monolithic power amplifier operating over the 6.0 to 18.0 GHz frequency band. The amplifier uses a .25 micron Pseudomorphic High Electron Mobility Transistor (PHEMT) process to maximize efficiency and output power. The chip configuration incorporates two stages of reactively combined amplifiers at the output preceded by an input amplifier stage. This single channel amplifier provides typically, 22 dB small signal gain and 31 dBm output power at 1 dB gain compression.

Features

- ◆ 21.0 dB Typical Small Signal Gain
- ◆ 2.0:1 Typical Input SWR, 2.5:1 Typical Output SWR
- ◆ 31 dBm Output Power at 1 dB Gain Compression
- ◆ 32 dBm Output Power at 3 dB Gain Compression
- ◆ 22% Typical Power Added Efficiency at 1 dB Gain Compression
- ◆ Chip size: 6.55 mm x 2.67 mm x 0.1 mm



Absolute Maximum Ratings (Single Channel)

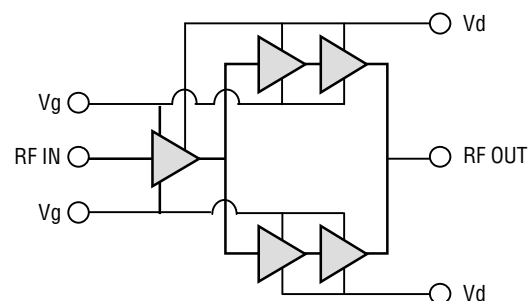
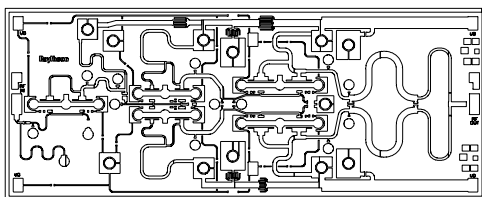
Parameter	Symbol	Value	Unit
Positive Drain DC Voltage	V _d	8.5	V
RF CW Input Power	P _{in}	27	dBm
Drain Current	I _d	1.2	A
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{storage}	-40 to 110	°C

Performance Characteristics

Parameter	Min	Typ	Max	Unit
Frequency Range	6.0		18.0	GHz
Small Signal Gain	15	21		dB
P1dB Compression.	28	31		dBm
P3dB Compression	30	32		dBm
PAE at 1 dB Gain Comp.	12	22		%
Input Return Loss		9.5		dB
Output Return Loss		7.4		dB

Parameter	Min	Typ	Max	Unit
Gate Voltage (V _G)		-0.4		V
Gain vs. Temp. 0~85°C		-0.025		dB/°C
Thermal Resistance @ T _{bc} =80°C (T _{bc} =Temp. @ back of chip)		12.0		°C/W
Maximum Safe Operating Channel Temp.		150		°C

Layout and Schematic



Characteristic performance data and specifications are subject to change without notice.

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Application Note

Scope:

This application note briefly describes the procedure for evaluating the Raytheon RMPA-61810, high efficiency .25um PHEMT Single-Channel Amplifier. The chip configuration incorporates two stages of reactively combined amplifiers at the output preceded by an input amplifier stage.

Carrier Assembly:

The attached drawing shows a recommended off chip bias scheme for the RMPA-61810. The MMIC is mounted on a Cu shim or ridge, which in turn blazed to Cu-Mo-Cu, or Cu-W, or Mo carrier with alumina 50-ohm microstrip lines for in/out RF connections and off-chip DC bias components. The drawing shows the placement of components and bond wire connections. The following should be noted:

- (1) 1 mil gold bond wires are used on the carrier assembly.
- (2) Use 3-1 mil gold wires about 25 mils in length for optimum RF performance.
- (3) VG: Gate Voltage (negative) input terminal for amplifier stages. For best results, the gate supply should have a source resistance less than 100 ohms.
- (4) VD: Drain Voltage (positive) input terminal for amplifier stages.
- (5) VG and VD on both sides of the MMIC must be biased to insure proper operation.
- (6) Bias decoupling capacitors of 0.01 uF (multilayer) and 100 pF (single layer) are used on the carrier.
- (7) Close placement of external components is essential to stability.
- (8) The test fixture should incorporate a pair of 25 uF capacitor on the drain and gate(optional) bias terminals to prevent oscillations caused by the test fixture.
- (9) For Laboratory testing uses good power supplies, set current limits on supplies to RF drive-up current level, keep supply wire/leads as short as possible and if required use additional bypass capacitors at the fixture terminals.

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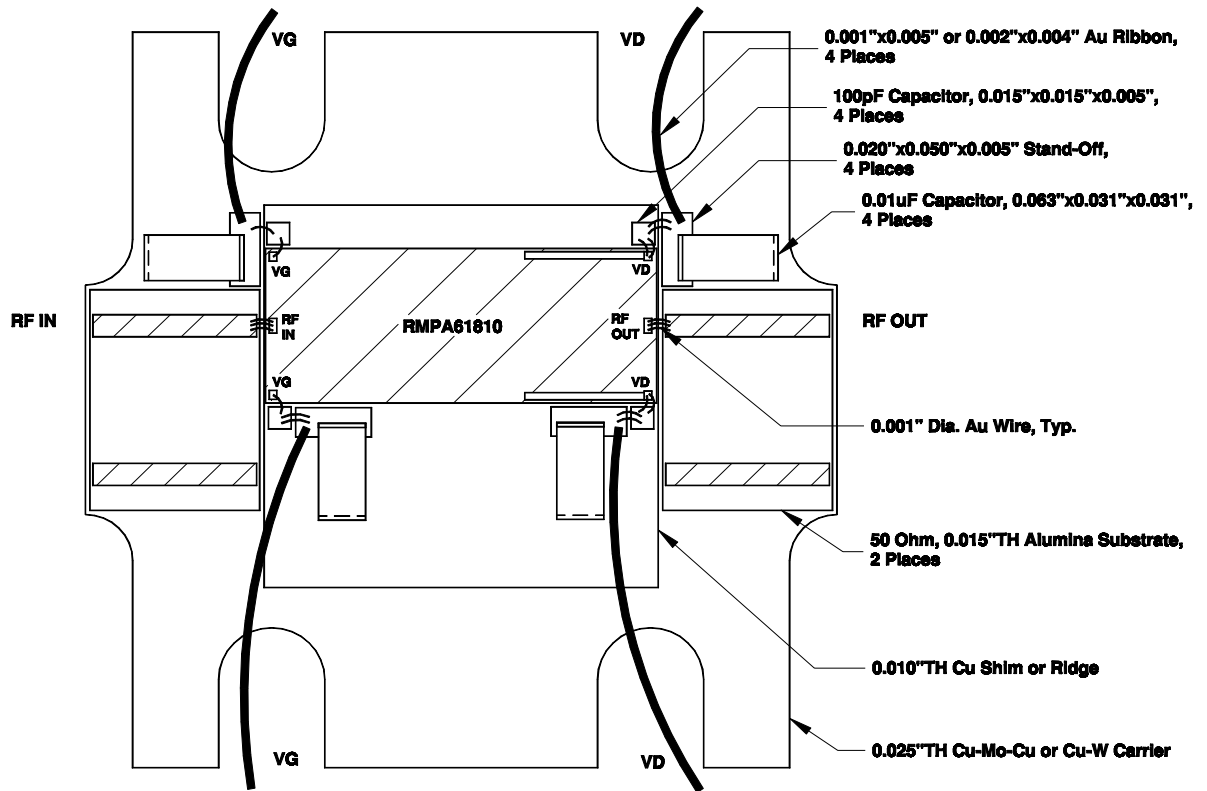
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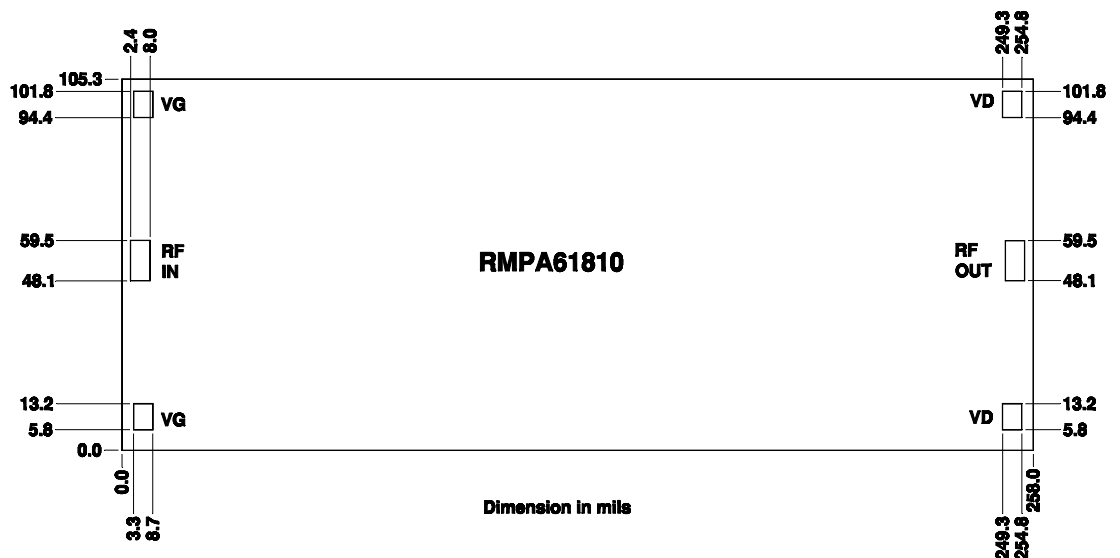
PRELIMINARY INFORMATION

Application Note

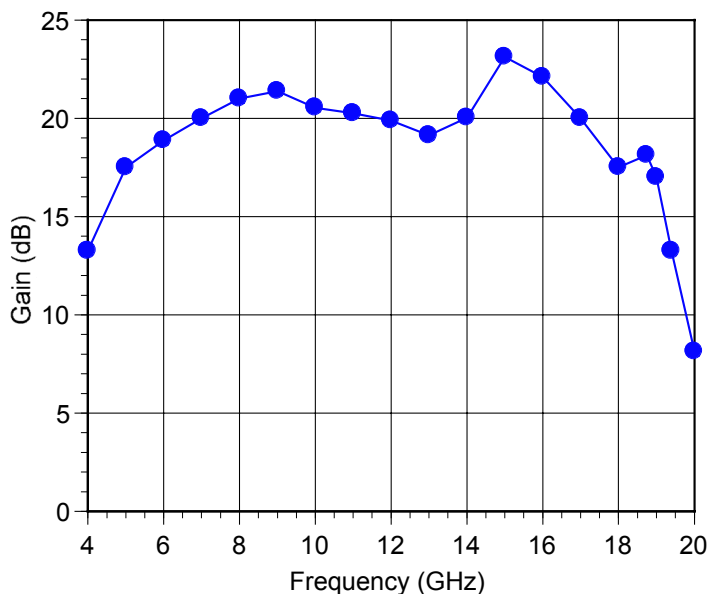
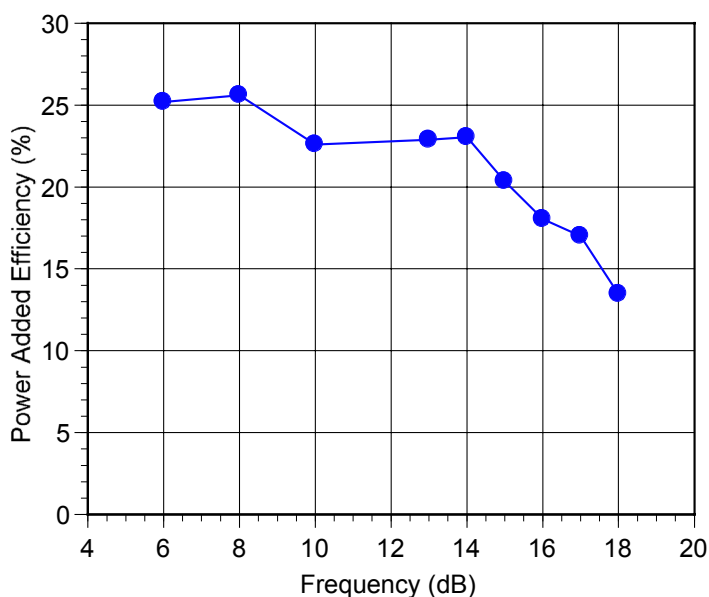
Example of
Assembled Module



Bonding Pads



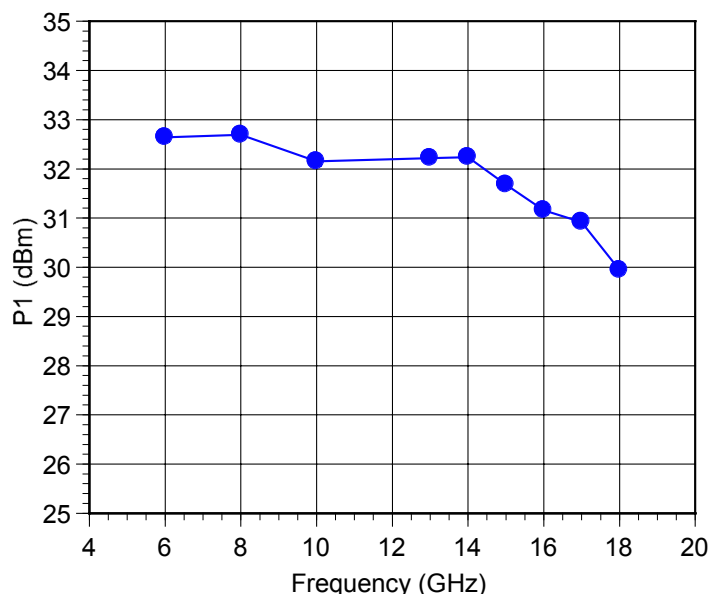
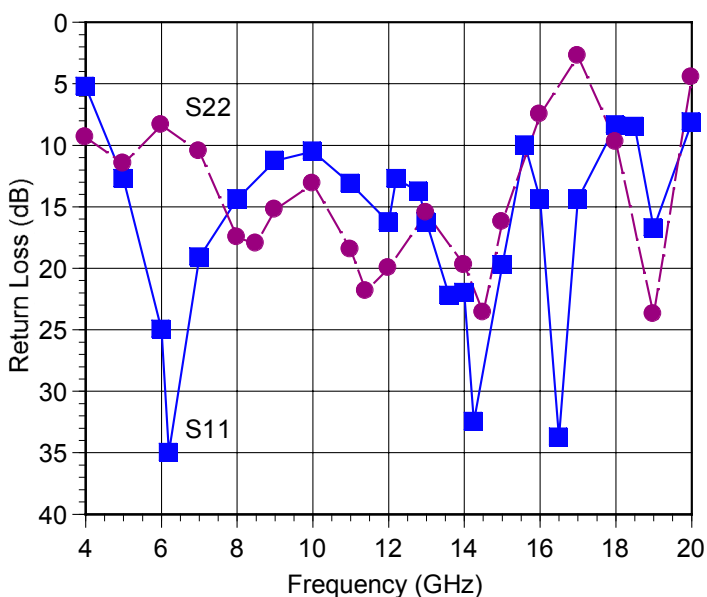
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**Typical
Characteristics****Small Signal Gain**
V_d=8.0V, I_{dq}=600mA**Power Added Efficiency @ P1**
V_d=8.0V, I_{dq}=600 mA

The above data is derived from fixtured measurements which includes 3 parallel, 1 mil diameter, 15 mil long, gold bond wires connected to the RF input and output.

The I_d @ 1 dB compression increases to 1 A or thereabouts. The dc supply should be able to support the required current to achieve the above performance.

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**Typical
Characteristics****Output Power @ 1 dB Compression**
Vd=8.0V, Idq=600mA**Input & Output Return Loss**
Vd=8.0V, Idq= 600mA

The above data is derived from fixtured measurements which includes 3 parallel, 1 mil diameter, 15 mil long, gold bond wires connected to the RF input and output.

The Id @ 1 dB compression increases to 1 A or thereabouts. The dc supply should be able to support the required current to achieve the above performance.

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Test Procedure

CAUTION: LOSS OF GATE VOLTAGE (VG) WHILE DRAIN VOLTAGE (VD) IS PRESENT MAY DAMAGE THE AMPLIFIER. THIS AMPLIFIER IS AN ESD SENSITIVE DEVICE.

The following procedure must be followed to properly test the amplifier:

Step 1: Slowly apply Gate Voltage (typical Vpinch-off= -1.5V) to terminal VG.

Step 2: Slowly apply Drain Voltage at VD (<+5 volts) and monitor drain current Ids. Adjust negative voltage VG to set the drain current (Ids) to approximately 600 mA. Adjust the drain voltage VD to nominal +8 volts (adjust Gate Voltage VG, if needed, to maintain the drain current at Ids).

Step 3: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band.

Step 4: Follow Turn-off sequence:

- (i) RF input power=off,
- (ii) VD=off,
- (iii) VG=off.

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Worldwide Sales Representatives

North America

D&L Technical Sales
6139 S. Rural Road, #102
Tempe, AZ 85283
480-730-9553
fax: 480-730-9647
Nicholas Delvecchio, Jr.
dlarizona@aol.com

Hi-Peak Technical Sales
P.O. Box 6067
Amherst, NH 03031
866-230-5453
fax: 603-672-9228
sales@hi-peak.com

Spartech South
2115 Palm Bay Road, NE,
Suite 4
Palm Bay, FL 32904
321-727-8045
fax: 321-727-8086
Jim Morris
jim@spartech-south.com

TEQ Sales, Inc.
920 Davis Road, Suite 304
Elgin, IL 60123
847-742-3767
fax: 847-742-3947
Dennis Culpepper
dculpepper@teqsales.com

Cantec Representatives
8 Strathearn Ave, No. 18
Brampton, Ontario
Canada L6T 4L9
905-791-5922
fax: 905-791-7940
Dave Batten
cantec-ott@cantec-o.net

Steward Technology
6990 Village Pkwy #206
Dublin, CA 94568
925-833-7978
fax: 925-560-6522
John Steward
johnsteward1@msn.com

Europe

Sangus OY
Lunkintie 21,
90460 Oulunsalo
Finland
358-8-8251-100
fax: 358-8-8251-110
Juha Virtala
juha.virtala@sangus.fi

Sangus AB
Berghamnvgen 68
Box 5004
S-165 10 Hasselby
Sweden
Ronny Gustafson
468-0-380210
fax: 468-0-3720954

Globes Elektronik & Co.
Klarastrabe 12
74072 Heilbronn
Germany
49-7131-7810-0
fax: 49-7131-7810-20
Ulrich Blievernicht
hfwelt@globes.de

MTI Engineering Ltd.
Afek Industrial Park
Hamelacha 11
New Industrial Area
Rosh Hayin 48091
Israel
972-3-902-5555
fax: 972-3-902-5556
Adi Peleg
adi_p@mti-group.co.il

Sirces srl
Via C. Boncompagni, 3B
20139 Milano
Italy
3902-57404785
fax: 3902-57409243
Nicola Iacovino
nicola.iacovino@sirces.it

Asia

ITX Corporation
2-5, Kasumigaseki
3-Chome
Chiyoda-Ku
Tokyo 100-6014 Japan
81-3-4288-7073
fax: 81-3-4288-7243
Maekawa Ryosuke
maekawa.ryosuke@
itx-corp.co.jp

Sea Union
9F-1, Building A, No 19-3
San-Chung Road
Nankang Software Park
Taiwan, ROC
Taipei 115
02-2655-3989
fax: 02-2655-3918
Murphy Su
murphy@seaunionweb.com.tw

Worldwide Distribution

Headquarters
6321 San Ignacio Drive
San Jose, CA 95119
408-360-4073
fax: 408-281-8802
Art Herbig
art.herbig@avnet.com

Belgium and Luxembourg
Cipalstraat
2440 GEEL
Belgium
32 14 570670
fax: 32 14 570679
sales.be@bfiophtilas.avnet.com

United Kingdom
Burnt Ash Road
Aylesford, Kent
England
ME207XB
44 1622882467
fax: 44 1622882469
rfsales.uk@
bfiophtilas.avnet.com

France
4 Allee du Cantal
Evry, Cedex
France
33 16079 5900
fax: 33 16079 8903
sales.fr@
bfiophtilas.avnet.com

Holland
Chr. Huygensweg 17
2400 AJ ALPHEN AAN DEN
RIJN
The Netherlands
31 172 446060
fax: 33 172 443414
sales.nl@
bfiophtilas.avnet.com

Spain
C/Isobel Colbrand, 6 - 4a
28050 Madrid
Spain
34 913588611
fax: 34 913589271
sales.es@
bfiophtilas.avnet.com

Sales Office Headquarters

**United States
(East Coast)**
Raytheon
362 Lowell Street
Andover, MA 01810
978-684-8628
fax: 978-684-8646
Walter Shelmet
wshelmet@
rrfc.raytheon.com

**United States
(West Coast)**
Raytheon
362 Lowell Street
Andover, MA 01810
978-684-8919
fax: 978-684-8646
Rob Sinclair
robert_w_sinclair@
rrfc.raytheon.com

Europe
Raytheon
AM Teckenberg 53
40883 Ratingen
Germany
49-2102-706-155
fax: 49-2102-706-156
Peter Hales
peter_j_hales@
raytheon.com

Asia
Raytheon
Room 601, Gook Je Ctr. Bldg
191 Hangang Ro 2-GA
Yongsan-Gu, Seoul,
Korea 140-702
82-2-796-5797
fax: 82-2-796-5790
T.G. Lee
tg_lee@
rrfc.raytheon.com

Customer Support

978-684-8900

fax: 978-684-5452

customer_support@rrfc.raytheon.com