UG2 Series

0.5µm ULC Series

Description

The UG2 series of ULCs is well suited for conversion of medium- to-large sized CPLDs and FPGAs. Devices are implemented in high-performance CMOS technology with 0.5-µm (drawn) channel lengths, and are capable of supporting flip-flop toggle rates of 625 MHz at 5V and 360 MHz at 3.3V, operating clock frequencies up to 150 MHz and input to output delays as fast as 5 ns, 200 ps at 5V.

The architecture of the UG2 series allows for efficient conversion of many PLD architecture and FPGA device types with higher IO count. A compact RAM cell, along with the large number of available gates allows the implementation of RAM in FPGA architectures that support this feature, as well as JTAG boundary-scan and scan-path testing.

Conversion to the UG2 series of ULC can provide a significant reduction in operating power when compared to the original PLD or FPGA. This is especially true when compared to many PLD and CPLD architecture devices, which typically consume 100 mA or more even when not being clocked. The UG2 series has a very low standby consumption of 0.4 nA/gate typically commercial temp, which would yield a standby current of 0.4 nA/gate, 4 mA on a 10,000 gate design. Operating consumption is a strict function of clock frequency, which typically results in a power reduction of 50% to 90% depending on the device being compared.

The UG2 series provides several options for output buffers, including a variety of drive levels up to 24 mA. Schmitt trigger inputs are also an option. A number of techniques are used for improved noise immunity and reduced EMC emissions, including: several independent power supply busses and internal decoupling for isolation; slew rate limited outputs are also available as required.

The UG2 series is designed to allow conversions of high performance 3-V devices as well as 5-V devices. Support of mixed supply conversions is also possible, allowing optimal trade-offs between speed and power consumption.

Features

- High performance ULC family suitable for medium- to large-sized CPLDs and FPGAs
- Conversions to over 700,000 FPGA gates
- Pin counts to over 582 pins
- Any pin-out matched due to limited number of dedicated pads
- Full range of packages: DIP, SOIC, LCC/PLCC, PQFP/TQFP, PGA/PPGA, PBGA/CABGA
- 3.3V and/or 5.0V operation.
- Low quiescent current: 0.04 nA/gate
- Available in commercial, industrial, automotive, military and space grades.
- 0.5 µm Drawn CMOS, 3 Metal Layers
- Library Optimised for Synthesis, Floor Plan & Automatic Test Generation (ATG)
- High Speed Performances:
  - 200 ps Typical Gate Delay @5 V
  - Typical 625 MHz Toggle Frequency @5V and 360 MHz @3.3 V
- High System Frequency Skew Control:
  - Clock Tree Synthesis Software
- 3 & 5 Volts Operation; Single or Dual Supply Modes
- Low Power Consumption:
  - 0.6 µW/Gate/MHz @3 V
  - 2.2 µW/Gate/MHz @5 V
- Power on Reset
- Standard 3, 6, 12 and 24mA I/Os
- CMOS/TTL/PCI Interface
- ESD (2 kV) and Latch–up Protected I/O
- High Noise & EMC Immunity:
  - I/O with Slew Rate Control
  - Internal Decoupling
  - Signal Filtering between Periphery & Core
  - Application Dependent Supply Routing & Several

Product Outline

Part Number*	Full programmable Pads	Equivalent FPGA Gates
UG2005	45	4900
UP2104	100	12500
UG215	111	24300
UG222	127	34800
UG244	171	58600
UG291	235	108500
UG2140	285	156800
UG2194	331	206300
UG2265	384	318000
UG2360	435	432000

** Check with factory for availability of product type.*

Architecture

The basic element of the UG2 family is called a cell. One cell can typically implement between two to three FPGA gates. Cells are located contiguously through out the core of the device, with routing resources provided in two or three metal layers above the cells. Some cell blockage does occur due to routing, and utilization will be significantly greater with three metal routing than two. The sizes listed in the Product Outline are estimated usable amounts using three metal layers. I/O cells are provided at each pad, and may be configured as inputs, outputs, I/Os, V_{DD} or V_{SS} as required to match any FPGA or PLD pinout. Special function cells and pins are located in the corners which typically are unused.

In order to improve noise immunity within the device, separate V_{DD} and V_{SS} busses are provided for the internal cells and the I/O cells.

I/O buffer interfacing

I/O Fexibility

All I/O buffers may be configured as input, output, bi–directional, oscillator or supply. A level translator could be located close to each buffer.

Outputs

Low noise buffers with 12 mA drive at 5 V.

I/O Options

Inputs

Each input can be programmed as TTL, CMOS, or Schmitt Trigger, with or without a pull up or pull down resistor.

Fast Output Buffer

Fast output buffers are able to source or sink 3 to 12 mA at 5 V according to the chosen option. 24mA achievable, using 2 pads.

Slew Rate Controlled Output Buffer

In this mode, the p- and n-output transistor commands are delayed, so that they are never set “ON” simultaneously, resulting in a low switching current and low noise. These buffer are dedicated to very high load drive.

3.3-V Compatibility

The UG2 series of ULCs is fully capable of supporting high-performance operation at 3.3 V or 5 V. The performance specifications of any given ULC design however, must be explicitly specified as 3.3 V, 5 V or both.

Power Supply and Noise Protection

The speed and density of the UG2 technology cause large switching current spikes for example either when:

16 high current output buffers switch simultaneously,

or

10% of the 700 000 gates are switching within a window of 1ns.

Sharp edges and high currents cause some parasitic elements in the packaging to become significant. In this frequency range, the package inductance and series resistance should be taken into account. It is known that an inductor slows down the setting time of the current and causes voltage drops on the power supply lines. These drops can affect the behaviour of the circuit itself or disturb the external application (ground bounce).

In order to improve the noise immunity of the UG2 core matrix, several mechanisms have been implemented inside the UG2 arrays. Two kinds of protection have been added: one to limit the I/O buffer switching noise and the other to protect the I/O buffers against the switching noise coming from the matrix.

I/O buffers switching protection

Three features are implemented to limit the noise generated by the switching current:

- The power supplies of the input and output buffers are separated.
- The rise and fall times of the output buffers can be controlled by an internal regulator.
- A design rule concerning the number of buffers connected on the same power supply line has been imposed.

Matrix switching current protection

This noise disturbance is caused by a large number of gates switching simultaneously. To allow this without impacting the functionality of the circuit, three new features have been added:

- Decoupling capacitors are integrated directly on the silicon to reduce the power supply drop.
- A power supply network has been implemented in the matrix. This solution reduces the number of parasitic elements such as inductance and resistance and constitutes an artificial VDD and Ground plane. One mesh of the network supplies approximately 150 cells.
- A low pass filter has been added between the matrix and the input to the output buffer. This limits the transmission of the noise coming from the ground or the VDD supply of the matrix to the external world via the output buffers.

Absolute Maximum Ratings

Supply Voltage (V_{DD}) . . . . . –0.5 V to 7.0 V
Input Voltage (V_{IN}) . . . . . –0.5 V to V_{DD} + 7.0 V
Storage Temperature . . . . . –65 to 150°C

Recommended Operating Range

V_{DD} . . . . . 2.7 to 5.5 V

Operating Temperature
Commercial . . . . . 0 to 70°C
Industrial . . . . . –40 to 85°C
Military . . . . . –55 to 125°C

DC Characteristics

Specified at VDD = +5 V ± 10 %

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIL	Input low voltage CMOS input TTL input	 0 0		 0.3 VDD 0.8	 V	
VIH	Input high voltage CMOS input TTL input	 0.7 VDD 2.2		 VDD VDD	 V	
VOL	Output low voltage TTL input			 0.4	 V	IOL = –12, 6, 3 mA*
VOH	Output high voltage CMOS input TTL input	 3.9 2.4			 V	IOH = +12, 6, 3 mA*
VT+	Scmitt trigger positive threshold CMOS input TTL input			 2.8 1.5	 V	
VT–	Scmitt trigger negative threshold CMOS input TTL input	 1.2 1.0			 V	
IL	Input leakage No pull up/down Pull up Pull down	–5 –120 79		+5 –55 330	µA	
IOZ	3–State Output Leakage current	–5		+5	µA	
IOS	Output Short circuit current IOSN IOSP			 48 36	 mA mA	Bout12 VOUT = 4.5 V VOUT = VSS
ICCSB	Leakage current per cell			5	nA	commercial
				7	nA	industrial
				10	nA	military
ICCOP	Operating current per cell			0.6	µA/MHz	

** According buffer: Bout12, Bout6, Bout3, VDD = 4,5 V*

DC Characteristics

Specified at VDD = +3 V ± 10 % or 3.3 ± 10 %

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIL	Input low voltage LVCMOS input LVTTL input	 0 0		 0.3 VDD 0.8	 V	
VIH	Input high voltage LVCMOS input LVTTL input	 0.7 VDD 2.0		 VDD VDD	 V	
VOL	Output low voltage TTL input			 0.4	 V	IOL = –6, 3, 1.5 mA*
VOH	Output high voltage TTL input	 2.4			 V	IOH = +4, 2, 1 mA*
VT+	Scmitt trigger positive threshold LVCMOS input LVTTL input			 1.1 1.5	 V	
VT–	Scmitt trigger negative threshold CMOS input TTL input	 1.0 0.9			 V	
IL	Input leakage No pull up/down Pull up Pull down	–5 –100 50		+5 –30 200	µA µA µA	
IOZ	3–State Output Leakage current	–5		+5	µA	
IOS	Output Short circuit current IOSN IOSP			 24 12	 mA mA	Bout12 VOUT = VDD VOUT = VSS
ICCSB	Leakage current per cell			3	nA	commercial
				5	nA	industrial
				7	nA	military
ICCOP	Operating current per cell			0.3	µA/MHz	

** According buffer: Bout12, Bout6, Bout3*

AC Characteristics

TJ = 25°C, Process typical (all values in ns)

Buffer	Description	Load	Transition	VDD	
				5V	3V
BOUT12	Output buffer with 12 mA drive	60pf	Tplh	3.18	4.67
			Tphl	2.35	3.33

Cell	Description	Load	Transition	VDD	
				5V	3V
BINCMOS	CMOS input buffer	15 fan	Tplh	0.75	1.12
			Tphl	0.7	0.98
BINTTL	TTL input buffer	16 fan	Tplh	0.88	1.29
			Tphl	0.65	1.03
INV	Inverter	12 fan	Tplh	0.54	0.85
			Tphl	0.39	0.49
NAND2	2 – input NAND	12 fan	Tplh	0.57	0.89
			Tphl	0.49	0.67
FDFF	D flip–flop, Clk to Q	8 fan	Tplh	0.86	1.30
			Tphl	0.73	1.08
			Ts	0.44	1.06
			Th	0.00	0.00

Power Consumption

Static Power Consumption for UG2 Series ULCs

There are three main factors to consider:

- Leakage in the core:
  - $P_{LC} = V_{DD} * I_{CCSB}$ * number of used gates
- Leakage in inputs and tri-stated outputs:
  - $P_{LIO} = V_{DD} * (I_{IX} * N + I_{OZ} * M)$
  - where: N = number of inputs
  - M = number of tri-stated outputs
  - Care must be taken to include the appropriate figure for pins with pull-ups or pull-downs. In practice, the static consumption calculation is typically done to determine the standby current of a device; in this case only those pins sourcing current should be included, i.e. where V_{IN} or $V_{OUT} = V_{DD}$.
- Dc power dissipation in driving I/O buffers due to resistive loads:
  - In practice, the static consumption calculation is typically done to determine the standby current of a device, and under circumstances where all of the outputs are tri-stated or in input mode. So this term is zero.
  - Global formula for static consumption:
  - $P_{SB} = P_{LC} + P_{LIO}$

Dynamic Power Consumption for UG2 Series ULCs

There are four main factors to consider:

- Static power dissipation is negligible compared to dynamic and can be ignored.
- Dc power dissipation in I/O buffers due to resistive loads:
  - $P_1 (mW) = V_{OL} * \Sigma_n (D_{Ln} * I_{OLn}) + (V_{DD} - V_{OH}) * \Sigma_n (D_{Hn} * I_{OHn})$
  - where: Σ_n is a summation over all of the outputs and I/Os.
  - I_{OLn} and I_{OHn} are the appropriate values for driver n
  - D_{Ln} = percentage of time n is being driven to V_{OL}
  - D_{Hn} = percentage of time n is being driven to V_{OH}

- It is difficult to obtain an exact value for this factor, since it is determined primarily by external system parameters. However, in practice this can be simplified to one of two cases where the device is either driving CMOS loads or driving TTL loads. CMOS loads can be approximated as purely capacitive loads, allowing this term to be treated as zero. TTL loads source significant current in the low state, but not the high state, allowing the second summation to be ignored. If a 50% duty cycle is assumed for dynamic outputs driving TTL loads, this can be approximated as:
- P_1 (mW) = V_{OL} * (Σ_n * I_{OLn}/2 + Σ_m * I_{OLm}) (TTL loads)
- where n are dynamic outputs and m are static low outputs.

– Dynamic power dissipation for the internal gates:
  - P_2 (mW) = V_{DD} * I_{DDOP} * Σ_g (N_f * f_g)/1000
  - where: N_f = number of gates toggling at frequency f_g
  - f_g = clock frequency of internal logic in MHz
  - Note: If the actual toggle rates are not known, a rule of thumb is to assume that the average used gate is toggling at one half of the input clock frequency.

– Dynamic power dissipation in the outputs:
  - P_3 (mW) = V_{DD}^2 * Σ_n f_n * (C_{OUT} + C_n)/1000
  - where: f_n = clocking frequency in MHz of output n
  - C_n = output load capacitance in pF of output n
  - C_{OUT} = output capacitance from DC Characteristics
  - Global formula for dynamic consumption:
  - $P = P_1 + P_2 + P_3$

Example:

Static calculation

- A 100-pin ULC with 3000 used gates, 10 inputs, 20 I/Os in input mode, 40 outputs all tri-stated. No pull-ups or pull-downs. Half of the pins are at V_{DD}, half at V_{SS}. Input clock is not toggling. For this example only the current calculation is desired, so the V_{DD} term in the equations is dropped.
- P_{LC} = 1 * 3000 = 3 mA
- P_{LIO} = ((10 + 20) * 5 + 40 * 5)/2 = 105 mA
- P_{SB} = 3 + 105 = 108 mA

Dynamic Calculation

- We take a 16-bit resettable ripple counter which is approximately 100 gates, operating at a clock frequency of 33 MHz, which gives an average clock frequency of 33 MHz/16 for each bit and each output. There are no static outputs on this device. Operation is at 5 V, and 6-mA outputs are used and loaded at 25 pF. The output buffers are driving CMOS loads.
- P_1 = 0
- P_2 = 5 * 0.5 * 100 * 33/16/1000 = 0.5 mW
- P_3 = 5^2 * 16 * 33/16 * (25 + 2)/1000 = 22 mW
- P = 0 + 0.5 + 22 = 22.5 mW

Typical ULC Test Conditions

For AC specification purposes, an improved output loading scheme has been defined for Atmel Wireless & Microcontrollers high-drive (24 mA), high-speed ULC devices. The schematic below (Figure 1) describes the typical conditions for testing these ULC devices, using the standard loading scheme commonly available on high-end ATE.

Compared to a no-load condition, this provides the following advantages:

- Output load is more representative of “real life” conditions during transitions.
- Transient energy is absorbed at the end of the line to prevent reflections which would lead to inaccurate ATE measurements.

Figure 1