VxxxPBC Rev. B2

LOCAL BUS TO PCI BRIDGE CONTROLLERS

Data Sheet Addendum

- Large, 576-byte FIFOs using V3's unique *DYNAMIC BANDWIDTH ALLOCATION™* architecture
- 33MHz and 40MHz local bus versions available with independent PCI operation up to 33MHz
- Both target and master (primary or secondary) modes supported on the PCI and local buses
- Dual bi-directional address space remapping
- On-the-fly byte order (endian) conversion including automatic endian detection
- I_2O^{TM} ready hardware messaging unit
- 2 channel DMA controller
- Bi-directional mailboxes w/doorbell interrupts
- Flexible PCI and local interrupt management
- Serial EEPROM configuration interface
- Fully compliant with PCI 2.1 specification
- Low cost 160-pin EIAJ PQFP package

This addendum is a companion to the V960PBC, V961PBC, V962PBC, V292PBC data sheets revision 2.3, which updates product codes and local bus timing parameters for revision B2 devices.

The pinouts, package mechanical information, DC characteristics, and PCI bus AC characteristics for any of the VxxxPBC devices can be found in corresponding B1 data sheets. Detailed functional information is contained in the PBC family User's Manual. The B2 Enhancement document, which is describing the added I_2O features, can be ordered by contacting V3 Semiconductor Sales office.

V3 Semiconductor retains the rights to change documentation, specifications, or device functionality at any time without notice. Please verify that you have the latest copy of all documents before finalizing a design.

1.0 Product Codes

Table 1: Product Codes

Product Code	Processor	Bus Type	Package	Frequency
V962PBC-33 REV B2	i960Cx/Hx	32-bit demultiplexed	160-pin EIAJ PQFP	33MHz
V962PBC-40 REV B2	i960Cx/Hx	32-bit demultiplexed	160-pin EIAJ PQFP	40MHz
V961PBC-33 REV B2	i960JA/JD/JF PPC401GF	32-bit multiplexed	160-pin EIAJ PQFP	33MHz
V961PBC-40 REV B2	i960JA/JD/JF PPC401GF	32-bit multiplexed	160-pin EIAJ PQFP	40MHz
V960PBC-33 REV B2	i960SA/SB	16-bit multiplexed	160-pin EIAJ PQFP	33MHz
V292PBC-33 REV B2	Am29030/35/40	32-bit demultiplexed	160-pin EIAJ PQFP	33MHz
V292PBC-40 REV B2	Am29030/35/40	32-bit demultiplexed	160-pin EIAJ PQFP	40MHz

2.0 Local Bus Timings

Table 2: Local Bus AC Test Conditions

Symbol	Parameter	Limits	Units
V_{CC}	Supply voltage	4.75 to 5.25	V
V_{IN}	Input low and high voltages	0.4 and 2.0	V
C_{OUT}	Capacitive load on output and I/O pins	50	pF

Table 3: Capacitive Derating for Output and I/O Pins

Output Drive Limit	Derating
4mA	0.096 ns/pF for loads > 50pF

Figure 1: Clock and Synchronous Signals

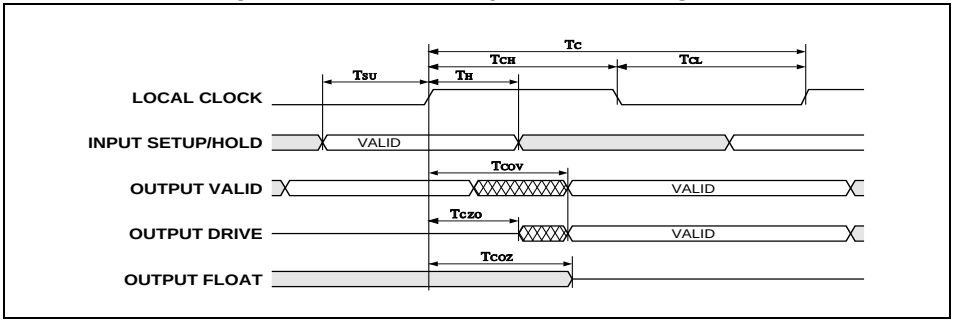

Table 4: V962PBC Local Bus Timing Parameters for Vcc = 5 Volts +/- 5%

				33MHz		40MHz		
#	**Symbol**	**Description**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Units**
1	T_C	LCLK period		30		25		ns
2	T_{CH}	LCLK high time	1	12		11		ns
3	T_{CL}	LCLK low time	1	12		11		ns
4	T_{SU}	Synchronous input setup	2	7		6		ns
4a	T_{SU}	Synchronous input setup ($\overline{BLAST}$)		8		7		ns
4b	T_{SU}	Synchronous input setup (W/$\overline{R}$, $\overline{BTERM}$)		4		4		ns
4c	T_{SU}	Synchronous input setup ($\overline{ADS}$)		6		5		ns
4d	T_{SU}	Synchronous input setup (address, data, byte enables)		9		8		ns
4e	T_{SU}	Synchronous input setup for read data when in local bus master mode		5		5		ns
5	T_H	Synchronous input hold			1		1	ns
6	T_{COV}	LCLK to output valid delay	3	3	14	3	12	ns
6a	T_{COV}	LCLK to output valid delay (address, data, byte enable, parity)		3	15	3	14	ns
7	T_{CZO}	LCLK to output driving delay		3	15	3	14	ns
8	T_{COZ}	LCLK to high impedance delay	4	3	15	3	14	ns
9	T_{RST}	Reset period when LRST used as input		$16 \cdot T_C$		$16 \cdot T_C$		ns

Notes:
1. Measured at 1.5V.
2. All local bus signals except those in 4a, 4b, 4c, 4d and 4e.
3. All local bus signals except those in 6a.
4. $\overline{READY}$, $\overline{BLAST}$, $\overline{ADS}$ are driven to high impedance at the falling edge of LCLK.

Table 5: V961PBC Local Bus Timing Parameters for Vcc = 5 Volts +/- 5%

				33MHz		40MHz		
#	**Symbol**	**Description**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Units**
1	T_C	LCLK period		30		25		ns
2	T_{CH}	LCLK high time	1	12		11		ns
3	T_{CL}	LCLK low time	1	12		11		ns
4	T_{SU}	Synchronous input setup	2	7		6		ns
4a	T_{SU}	Synchronous input setup ($\overline{BLAST}$)		8		7		ns
4b	T_{SU}	Synchronous input setup (W/$\overline{R}$, $\overline{BTERM}$)		4		4		ns
4c	T_{SU}	Synchronous input setup ($\overline{ADS}$)		6		5		ns
4d	T_{SU}	Synchronous input setup (address, data, byte enables)		9		8		ns
4e	T_{SU}	Synchronous input setup for read data when in local bus master mode		5		5		ns
5	T_H	Synchronous input hold			1		1	ns
6	T_{COV}	LCLK to output valid delay	3	3	14	3	12	ns
6a	T_{COV}	LCLK to output valid delay (address, data, byte enable, parity)		3	15	3	14	ns
7	T_{CZO}	LCLK to output driving delay		3	15	3	14	ns
8	T_{COZ}	LCLK to high impedance delay	4	3	15	3	14	ns
9	T_{RST}	Reset period when LRST used as input		$16 \cdot T_C$		$16 \cdot T_C$		ns

Notes:
1. Measured at 1.5V.
2. All local bus signals except those in 4a, 4b, 4c, 4d and 4e.
3. All local bus signals except those in 6a.
4. $\overline{RDYRCV}$, $\overline{BLAST}$, $\overline{ADS}$ are driven to high impedance at the falling edge of LCLK.

Table 6: V960PBC Local Bus Timing Parameters for Vcc = 5 Volts +/- 5%

				33MHz		
#	**Symbol**	**Description**	**Notes**	**Min**	**Max**	**Units**
1	T_C	LCLK period		30		ns
2	T_{CH}	LCLK high time	1	12		ns
3	T_{CL}	LCLK low time	1	12		ns
4	T_{SU}	Synchronous input setup	2	7		ns
4a	T_{SU}	Synchronous input setup ($\overline{BLAST}$)		8		ns
4b	T_{SU}	Synchronous input setup (W/$\overline{R}$)		4		
4c	T_{SU}	Synchronous input setup ($\overline{AS}$)		6		
4d	T_{SU}	Synchronous input setup (address, data, byte enables)		9		
4e	T_{SU}	Synchronous input setup for read data when in local bus master mode		5		
5	T_H	Synchronous input hold			2	ns
6	T_{COV}	LCLK to output valid delay	3	3	14	ns
6a	T_{COV}	LCLK to output valid delay (address, data, byte enable, parity)		3	15	ns
7	T_{CZO}	LCLK to output driving delay		3	15	ns
8	T_{COZ}	LCLK to high impedance delay	4	3	15	ns
9	T_{RST}	Reset period when LRST used as input		$16 \cdot T_C$		ns

Notes:
1. Measured at 1.5V.
2. All local bus signals except those in 4a, 4b, 4c, 4d and 4e.
3. All local bus signals except those in 6a.
4. $\overline{READY}$, $\overline{BLAST}$, $\overline{AS}$ are driven to high impedance at the falling edge of LCLK.

Table 7: V292PBC Local Bus Timing Parameters for Vcc = 5 Volts +/- 5%

				33MHz		40MHz		
#	**Symbol**	**Description**	**Notes**	**Min**	**Max**	**Min**	**Max**	**Units**
1	T_C	LCLK period		30		25		ns
2	T_{CH}	LCLK high time	1	12		11		ns
3	T_{CL}	LCLK low time	1	12		11		ns
4	T_{SU}	Synchronous input setup	2	7		6		ns
4a	T_{SU}	Synchronous input setup ($\overline{BURST}$)		8		7		ns
4b	T_{SU}	Synchronous input setup (R/$\overline{W}$, $\overline{ERR}$)		4		4		ns
4c	T_{SU}	Synchronous input setup ($\overline{LREQ}$)		6		5		ns
4d	T_{SU}	Synchronous input setup (address, data, byte enables)		9		8		ns
4e	T_{SU}	Synchronous input setup for read data when in local bus master mode		5		5		ns
5	T_H	Synchronous input hold			1		1	ns
6	T_{COV}	LCLK to output valid delay	3	3	14	3	12	ns
6a	T_{COV}	LCLK to output valid delay (address, data, byte enable, parity)		3	15	3	14	ns
7	T_{CZO}	LCLK to output driving delay		3	15	3	14	ns
8	T_{COZ}	LCLK to high impedance delay	4	3	15	3	14	ns
9	T_{RST}	Reset period when LRST used as input		$16 \cdot T_C$		$16 \cdot T_C$		ns

Notes:
1. Measured at 1.5V.
2. All local bus signals except those in 4a, 4b, 4c, 4d and 4e.
3. All local bus signals except those in 6a.
4. $\overline{RDY}$, $\overline{BURST}$, $\overline{LREQ}$ are driven to high impedance at the falling edge of LCLK.

The timing parameters of the ALE signal in V960PBC and V961PBC Rev B2 devices are the same as revision B1 of the silicon.

3.0 Revision History

Table 8: Revision History

Revision Number	Date	Comments and Changes
1.0	2/97	First revision of the VxxxPBC data sheet addendum.

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