Preliminary Information

4K/8K X84047/X84087 MPS™ E²PROM

Micro Port Saver E²PROM with ID Lock™

FEATURES

- **Direct Interface to Micros**
  - **—Eliminates I/O port requirements**
  - **—No interface glue logic required**
  - **—Eliminates need for parallel to serial converters**
- **IDLock**
- **Up to 5Mbps data transfer rate**
- **1048 x 8 Bits**
  - **—16 Byte Page Write Mode**
- **ID Lock Protection**
  - **—Block Lock Protect any 1/4, 1st 1/2, First or Last Page or None of the array**
- **Low Power CMOS**
  - **—<1μA Standby Current**
  - **—<3mA Active Current during Program**
  - **—<400μA Active Current during Read**
- **Minimum 25ns Read Access Time**
- **Single Byte Write Capability**
- **Typical Nonvolatile Write Cycle Time: 5ms**
- **High Reliability**
  - **—100,000 Endurance Cycles**
  - **—Guaranteed Data Retention: 100 Years**
- **Small Package Options**
  - **—8-Lead SOIC Package**
  - **—8-Lead TSSOP Package**

DESCRIPTION

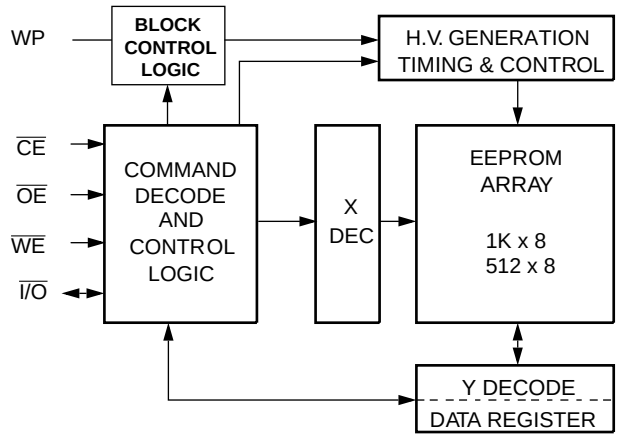
The X84047/X84087 Micro Port Saver device is an 8K-bit CMOS E²PROM designed for direct interface to port limited microcontroller or I/O limited microprocessor designs. This device provides all of the benefits of serial memories, such as low cost, low power, low voltage operation, and small package size, while featuring high data transfer rates and reduced interface code requirements—without the need for a dedicated serial bus. The X84047/X84087 is organized as a byte wide memory, but it is also suitable in 16-bit, 32-bit or 64-bit environments, due to the bit serial nature of the interface.

The X84047/X84087 device directly connects to the processor bus and communicates over a single data line using a sequence of standard bus read and write operations. This eliminates the need for dedicated port pins, parallel to serial converters, complicated ASIC implementations, or other glue logic, lowering system cost.

An ID Lock feature prevents writes to as little as 16 bytes or as much as half the array. A Write Protect ($\overline{WP}$) pin prevents inadvertent writes to the entire memory.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

BLOCK DIAGRAM



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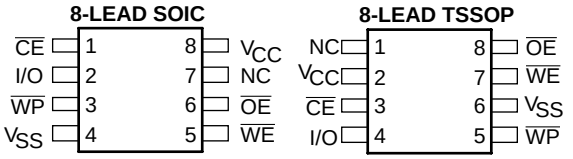
PIN CONFIGURATIONS



PIN NAMES

I/O	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{WP}$	Write Protect Input
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	No Connect

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PIN DESCRIPTIONS

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, the chip is deselected, the I/O pin is in the high impedance state, and unless a nonvolatile write operation is underway, the device is in the standby power mode.

Output Enable ($\overline{OE}$)

The Output Enable input must be LOW to enable the output buffer and to read data from the device on the I/O line.

Write Enable ($\overline{WE}$)

The Write Enable input must be LOW to write either data or command sequences to the device.

Data In/Data Out (I/O)

Data and command sequences are serially written to or serially read from the device through the I/O pin.

Write Protect ($\overline{WP}$)

When the Write Protect input is LOW, nonvolatile writes to the device are disabled. When $\overline{WP}$ is HIGH, all functions, including nonvolatile writes, operate normally. If a nonvolatile write cycle is in progress, $\overline{WP}$ going LOW will have no effect on the cycle already underway, but will inhibit any additional nonvolatile write cycles.

DEVICE OPERATION

The X84047/X84087 is a serial E^2PROM designed to interface directly with most microprocessor buses. Standard $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ signals control the read and write operations, and a single I/O line is used to send and receive data and commands serially.

Data Timing

Data input on the I/O line is latched on the rising edge of either $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Data output on the I/O line is active whenever both $\overline{OE}$ and $\overline{CE}$ are LOW. Care should be taken to ensure that $\overline{WE}$ and $\overline{OE}$ are never both LOW while $\overline{CE}$ is LOW.

Read Sequence

A read sequence consists of sending a 16-bit address followed by the reading of data serially. The address is written by issuing 16 separate write cycles ($\overline{WE}$ and $\overline{CE}$ LOW, $\overline{OE}$ HIGH) to the part without a read cycle between the write cycles. The address is sent serially, most significant bit first, over the I/O line. Note that this sequence is fully static, with no special timing restrictions, and the processor is free to perform other tasks on the bus whenever the device $\overline{CE}$ pin is HIGH. Once the 16 address bits are sent, a byte of data can be read on the I/O line by issuing 8 separate read cycles ($\overline{OE}$ and $\overline{CE}$ LOW, $\overline{WE}$ HIGH). At this point, writing a ‘1’ will terminate the read sequence and enter the low power standby state, otherwise the device will await further reads in the sequential read mode.

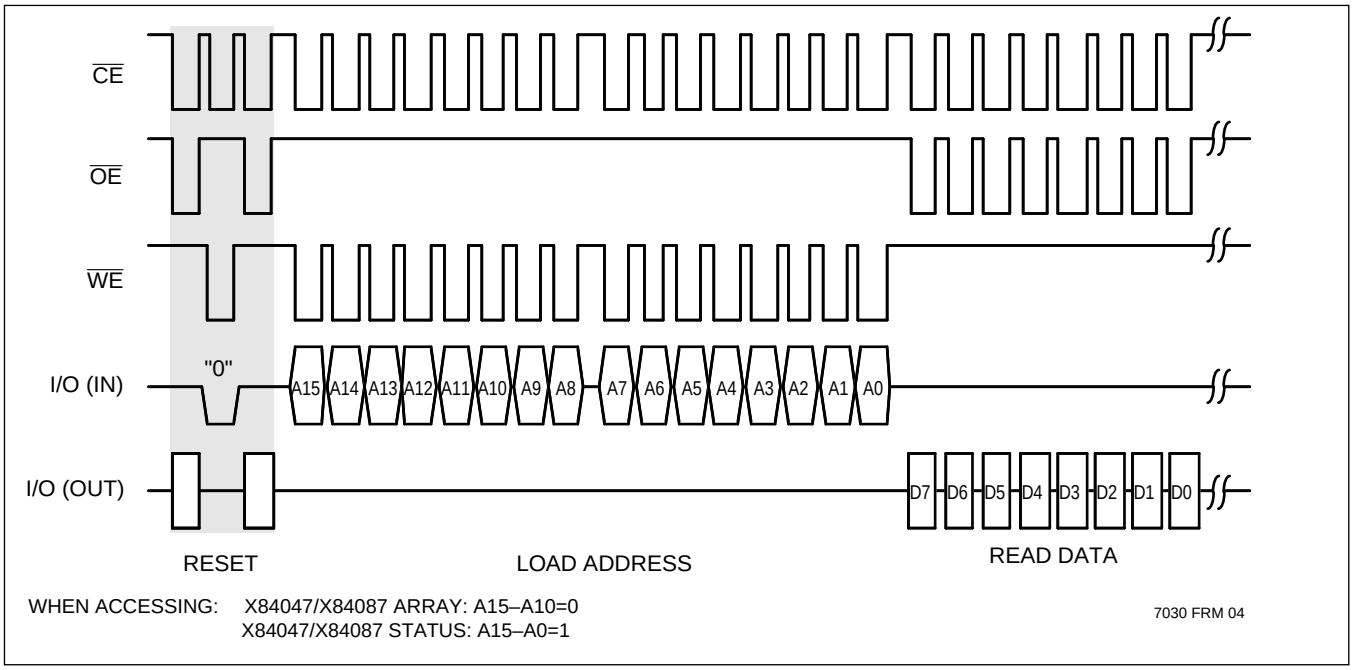
Sequential Read

The byte address is automatically incremented to the next higher address after each byte of data is read. The data stored in the memory at the next address can be read sequentially by continuing to issue read cycles. When the highest address in the array is reached, the address counter rolls over to address $000 and reading may be continued indefinitely.

Reset Sequence

The reset sequence resets the device and sets an internal write enable latch. A reset sequence can be sent at any time by performing a read/write “0”/read operation (see Figs. 1 and 2). This breaks the multiple read or write cycle sequences that are normally used to read from or write to the part. The reset sequence can be used at any time to interrupt or end a sequential read or page load. As soon as the write “0” cycle is complete, the part is reset (unless a nonvolatile write cycle is in progress). The second read cycle in this sequence, and any further read cycles, will read a HIGH on the I/O pin until a valid read sequence (which includes the address) is issued. The reset sequence must be issued at the beginning of both read and write sequences to be sure the device initiates these operations properly.

Figure 1. Read Sequence



Write Sequence

A nonvolatile write sequence consists of sending a reset sequence, a 16-bit address, up to 16 bytes of data, and then a special “start nonvolatile write cycle” command sequence. The reset sequence is issued first (as described in the Reset Sequence section) to set an internal write enable latch. The address is written serially by issuing 16 separate write cycles ($\overline{WE}$ and $\overline{CE}$ LOW, $\overline{OE}$ HIGH) to the part without any read cycles between the writes. The address is sent serially, most significant bit first, on the I/O pin.

Up to 16 bytes of data are written by issuing a byte multiple of write cycles. Again, no read cycles are allowed between writes. The nonvolatile write cycle is initiated by issuing a special read/write “1”/read sequence. The first read cycle ends the page load, then the write “1” followed by a read starts the nonvolatile write cycle.

The device recognizes 16-byte pages beginning at addresses XXXXX0000. When sending data to the part, attempts to exceed the upper address of the page will result in the address counter “wrapping-around” to the first address on the page, where data loading can continue. For this reason, sending more than 128 consecutive data bits to a page will result in overwriting previous data just sent to the same page. A nonvolatile write cycle will not start if a partial or incomplete write sequence is issued. The internal write enable latch is reset when the nonvolatile write cycle is completed to prevent inadvertent writes. Note that this sequence is fully static, with no special timing restrictions. The processor is free to perform other tasks on the bus whenever the chip enable pin ($\overline{CE}$) is HIGH.

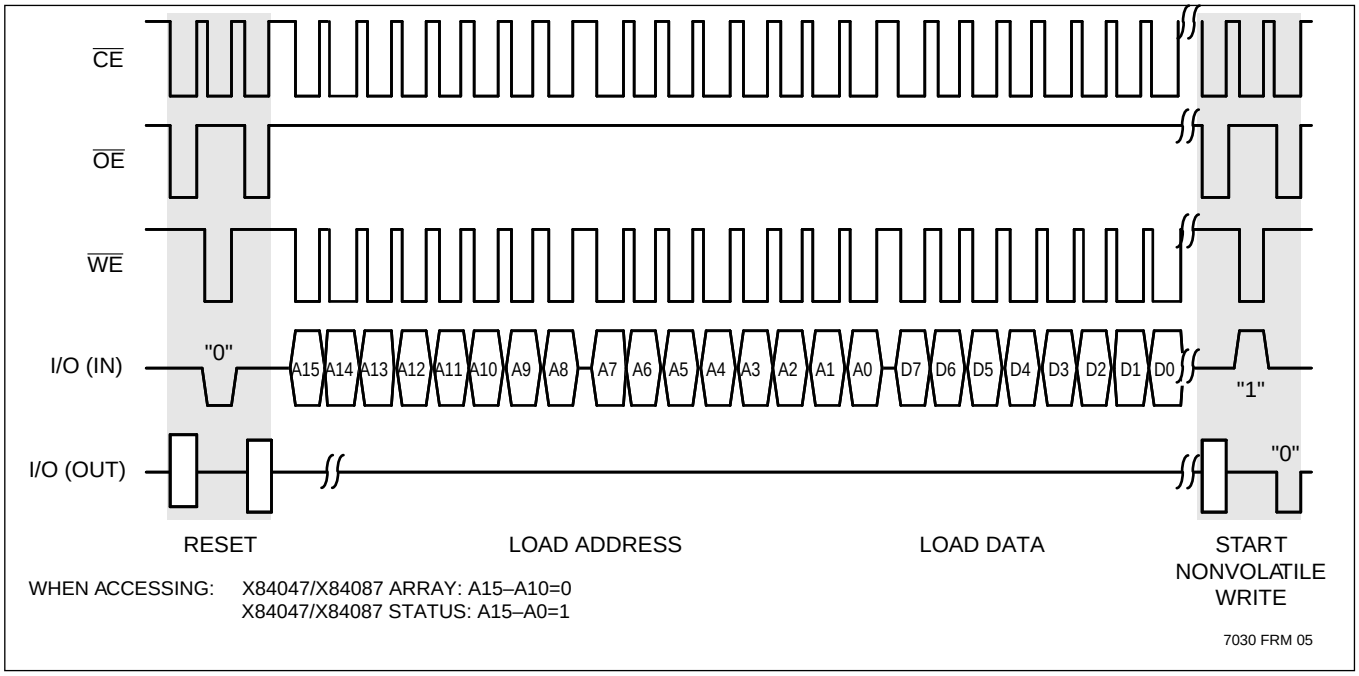
Nonvolatile Write Status

The status of a nonvolatile write cycle can be determined at any time by simply reading the state of the I/O pin on the device. This pin is read when $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH. A read during a nonvolatile write cycle returns the I/O state as LOW. When the nonvolatile write cycle is complete, reading the I/O pin returns a HIGH. A reset sequence can also be issued during a nonvolatile write cycle with the same result: I/O is LOW as long as a nonvolatile write cycle is in progress, and I/O is HIGH when the nonvolatile write cycle is done.

ID Lock Operation

Standard reads and writes to address FFFFh gain access to the Status Register of the X84047/X84087. The status register contains three bits to control the ID lock functions. ID Lock provides the designer a mechanism of preventing writes to one of seven segments of memory. These segments range in size from 16 bytes to 512 bytes. Table 1 shows the location of the control bits in the status register. Table 2 shows the ID lock that results from the selected BL bits. To protect the entire array from write operations, tie the $\overline{WP}$ pin LOW. With WP LOW, no writes are allowed to any array location,

Figure 2: Write Sequence



regardless of the setting of the ID Lock bits. It is possible to read and write only a single byte at a time from/to the status register. Writing more than one byte to the status register will abort the operation. Reading bytes after the first byte will return '0'.

Table 1. Status Register/ID Lock Protection Byte

7	6	5	4	3	2	1	0
0	0	0	0	0	BL2	BL1	BL0

Note: Bits [7:3] specified to be "0's"

.

Table 2. Block Protect Bits

BL2	BL1	BL0	Array Locked	X84047 Address	X84087 Address
0	0	0	None	N/A	N/A
0	0	1	Lowest 1/4 (Q1)	00H-7FH	00H-FFH
0	1	0	Second 1/4 (Q2)	80H-FFH	100H-1FFH
0	1	1	Third 1/4 (Q3)	100H-17FH	200H-2FFH
1	0	0	Highest 1/4 (Q4)	180H-1FFH	300H-3FFH
1	0	1	Lowest 1/2 (H1)	00H-FFH	00H-1FFH
1	1	0	Lower Page (P0)	0H-FH	00H-0FH
1	1	1	Upper Page (Pn)	1F0H-1FFH	3F0H-3FFH

Low Power Operation

The device enters an idle state, which draws minimal current when:

—an illegal sequence is entered. The following are the more common illegal sequences:

- Read/Write/Write—any time
- Read/Write '1'—When writing the address or writing data.
- Write '1'—when reading data
- Read/Read/Write '1'—after data is written to device, but before entering the NV write sequence.

—the device powers-up;

—a nonvolatile write operation completes.

While a sequential read is in progress, the device remains in an active state. This state draws more current than the idle state, but not as much as during a read itself. To go back to the lowest power condition, an invalid condition is created by writing a '1' after the last bit of a read operation.

Write Protection

The following circuitry has been included to prevent inadvertent nonvolatile writes:

—The internal Write Enable latch is reset upon power-up.

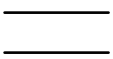
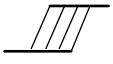
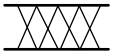
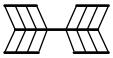
—A reset sequence must be issued to set the internal write enable latch before starting a write sequence.

—A special “start nonvolatile write” command sequence is required to start a nonvolatile write cycle.

—The internal Write Enable latch is reset automatically at the end of a nonvolatile write cycle.

—The internal Write Enable latch is reset and remains reset as long as the $\overline{WP}$ pin is LOW, which blocks all nonvolatile write cycles.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don’t Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Terminal Voltage with
Respect to V_{SS} .....–1V to +7V
DC Output Current..... 5mA
Lead Temperature (Soldering, 10 seconds).....300°C

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Extended	–20°C	+85°C
Industrial	–40°C	+85°C

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Supply Voltage	Limits
X84047/X84087	5V ±10%
X84047/X84087 – 2.7†	2.7V to 5.5V

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† Contact factory for availability.

D.C. OPERATING CHARACTERISTICS (V_{CC} = 5V ±10%)

(Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, I/O = Open, $\overline{CE}$ clocking @ 4MHz
I_{CC2}	V_{CC} Supply Current (Write)		2	mA	I_{CC} During Nonvolatile Write Cycle All Inputs at CMOS Levels
I_{SB1}	V_{CC} Standby Current		1	µA	$\overline{CE}$ = V_{CC}, Other Inputs = V_{CC} or V_{SS}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL} (1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH} (1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA, V_{CC} = 5V ±10%
V_{OH}	Output HIGH Voltage	V_{CC} – 0.8		V	I_{OH} = –1mA, V_{CC} = 5V ±10%

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Notes: (1) V_{IL} Min. and V_{IH} Max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

D.C. OPERATING CHARACTERISTICS (V_{CC} = 3V ±10%)

(Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		500	µA	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, I/O = Open, $\overline{CE}$ clocking @ 1MHz
I_{CC2}	V_{CC} Supply Current (Write)		2	mA	I_{CC} During Nonvolatile Write Cycle All Inputs at CMOS Levels
I_{SB1}	V_{CC} Standby Current		1	µA	$\overline{CE}$ = V_{CC}, Other Inputs = V_{CC} or V_{SS}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 1mA, V_{CC}=3V
V_{OH}	Output HIGH Voltage	V_{CC} – 0.4		V	I_{OH} = –400µA, V_{CC}=3V

7030 FRM T05.1

Notes: (1) V_{IL} Min. and V_{IH} Max. are for reference only and are not tested.

D.C. OPERATING CHARACTERISTICS (V_{CC} = 1.8V-3.6V)

(Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		300	µA	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, I/O = Open, $\overline{CE}$ clocking @ 1MHz
I_{CC2}	V_{CC} Supply Current (Write)		1	mA	I_{CC} During Nonvolatile Write Cycle All Inputs at CMOS Levels
I_{SB1}	V_{CC} Standby Current		1	µA	$\overline{CE}$ = V_{CC}, Other Inputs = V_{CC} or V_{SS}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–1	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 0.5mA, V_{CC}=2V
V_{OH}	Output HIGH Voltage	V_{CC} – 0.2		V	I_{OH} = –250µA, V_{CC}=2V

7030 FRM T05.1

Notes: (1) V_{IL} Min. and V_{IH} Max. are for reference only and are not tested.

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

7030 FRM T06

Notes: (2) Periodically sampled, but not 100% tested.

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(3)	Power-up to Read Operation	1	ms
t_{PUW}(3)	Power-up to Write Operation	1	ms

7030 FRM T07

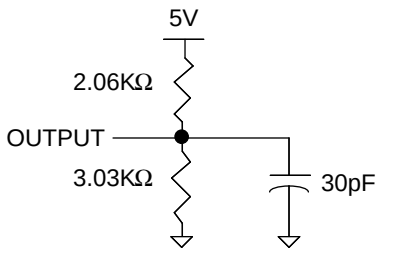
Notes: (3) Time delays required from the time the V_{CC} is stable until the specific operation can be initiated. Periodically sampled, but not 100% tested.

A.C. CONDITIONS OF TEST

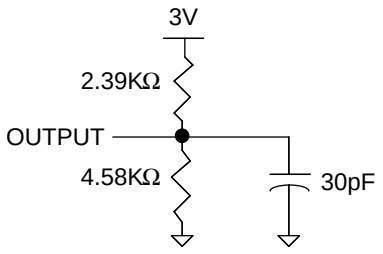
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	5ns
Input and Output Timing Levels	V_{CC} x 0.5

7030 FRM T08

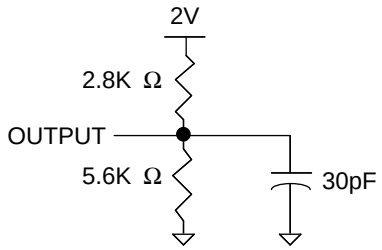
EQUIVALENT A.C. LOAD CIRCUITS



7030 FRM F06



7030 FRM F07



7030 FRM F07

A.C. CHARACTERISTICS

(Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits – X84047/X84087

Symbol	Parameter	V_{CC} = 4.5V-5.5V		V_{CC} = 2.5V-5.5V		V_{CC} = 1.8-3.6V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	50		100		200		ns
t_{CE}	$\overline{CE}$ Access Time		10		25		50	ns
t_{OE}	$\overline{OE}$ Access Time		10		25		50	ns
t_{OEL}	$\overline{OZ}$ Pulse Width	25		30		50		ns
t_{OEH}	$\overline{OZ}$ HIGH Recovery Time	25		30		50		ns
t_{LOW}	$\overline{CE}$ LOW Time	20		30		65		ns
t_{HIGH}	$\overline{CE}$ HIGH Time	30		30		30		ns
t_{LZ}(4)	$\overline{CE}$ LOW to Output In Low Z	0		0		0		ns
t_{HZ}(4)	$\overline{CE}$ HIGH to Output In High Z	0	15	0	30	0	95	ns
t_{OLZ}(4)	$\overline{OE}$ LOW to Output In Low Z	0		0		0		ns
t_{OHZ}(4)	$\overline{OE}$ HIGH to Output In High Z	0	15	0	50	0	110	ns
t_{OH}	Output Hold from $\overline{CE}$ or $\overline{OE}$ HIGH	0		0		0		ns
t_{WES}	$\overline{WE}$ HIGH Setup Time	10		10		10		ns
t_{WEH}	$\overline{WE}$ HIGH Hold Time	10		10		10		ns

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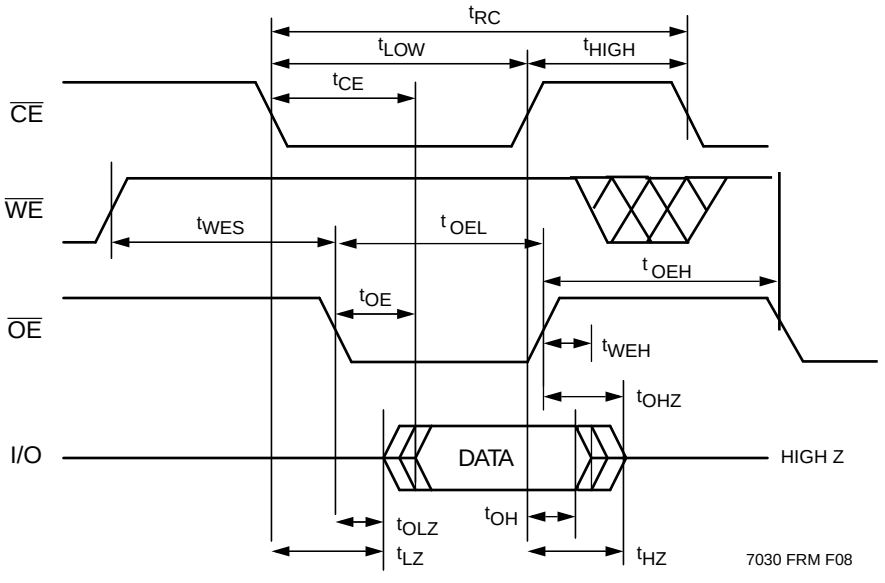
Notes: (4) Periodically sampled, but not 100% tested. t_{HZ} and t_{OHZ} are measured from the point where $\overline{CE}$ or $\overline{OE}$ goes HIGH (whichever occurs first) to the time when I/O is no longer being driven into a 5pF load.

Read Cycle



Write Cycle Limits – X84047/X84087

Symbol	Parameter	V_{CC} = 4.5V-5.5V		V_{CC} = 2.5V-5.5V		V_{CC} = 1.8-3.6V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{NVWC}(5)	Nonvolatile Write Cycle Time		3		5		5	ms
t_{WC}	Write Cycle Time	50		95		156		ns
t_{WP}	$\overline{WE}$ Pulse Width	20		35		70		ns
t_{WPH}	$\overline{WE}$ HIGH Recovery Time	65		35		35		ns
t_{CS}	Write Setup Time	0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		ns
t_{CP}	$\overline{CE}$ Pulse Width	25		40		65		ns
t_{CPH}	$\overline{CE}$ HIGH Recovery Time	100		30		30		ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	25		25		50		ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	25		25		50		ns
t_{DS}(6)	Data Setup Time	12		20		40		ns
t_{DH}(6)	Data Hold Time	5		5		5		ns
t_{WPSU}(7)	$\overline{WP}$ HIGH Setup	100		100		150		ns
t_{WPHD}(7)	$\overline{WP}$ Hold HIGH	100		100		150		ns

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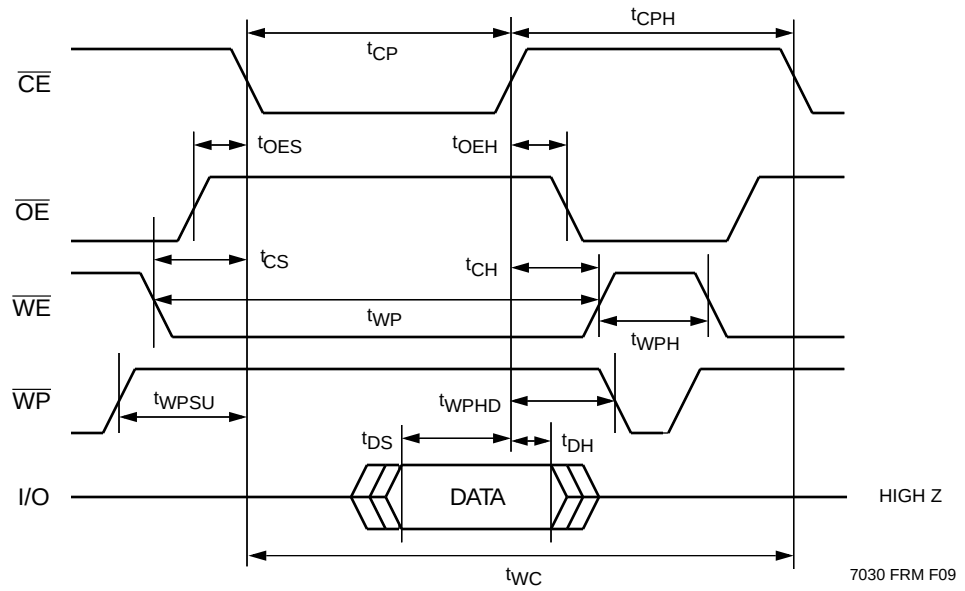
Notes: (5) t_{NVWC} is the time from the falling edge of $\overline{OE}$ or $\overline{CE}$ (whichever occurs last) of the second read cycle in the “start nonvolatile write cycle” sequence until the self-timed, internal nonvolatile write cycle is completed.

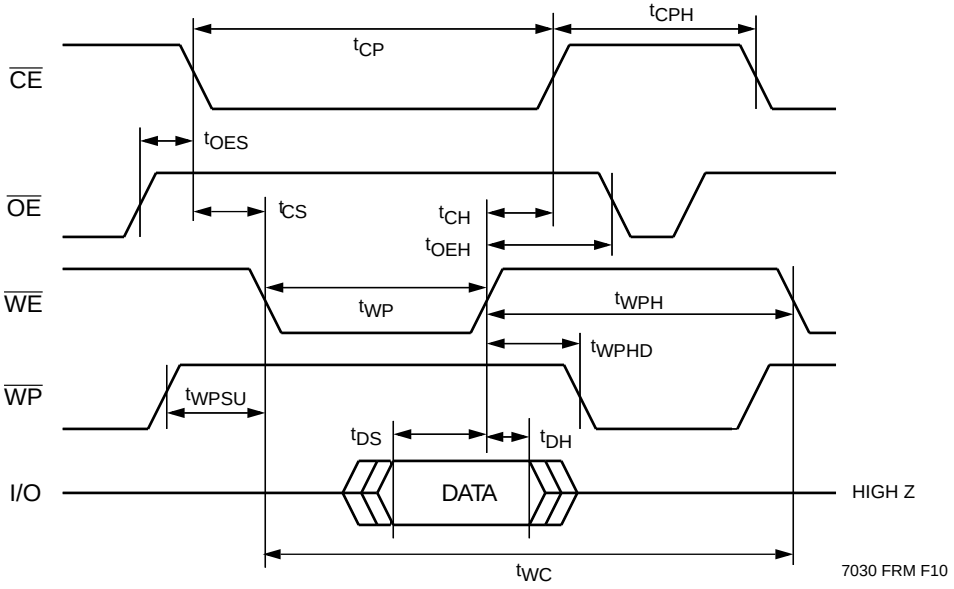
(6) Data is latched into the X84047/X84087 on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.

(7) Periodically sampled, but not 100% tested.

$\overline{CE}$ Controlled Write Cycle

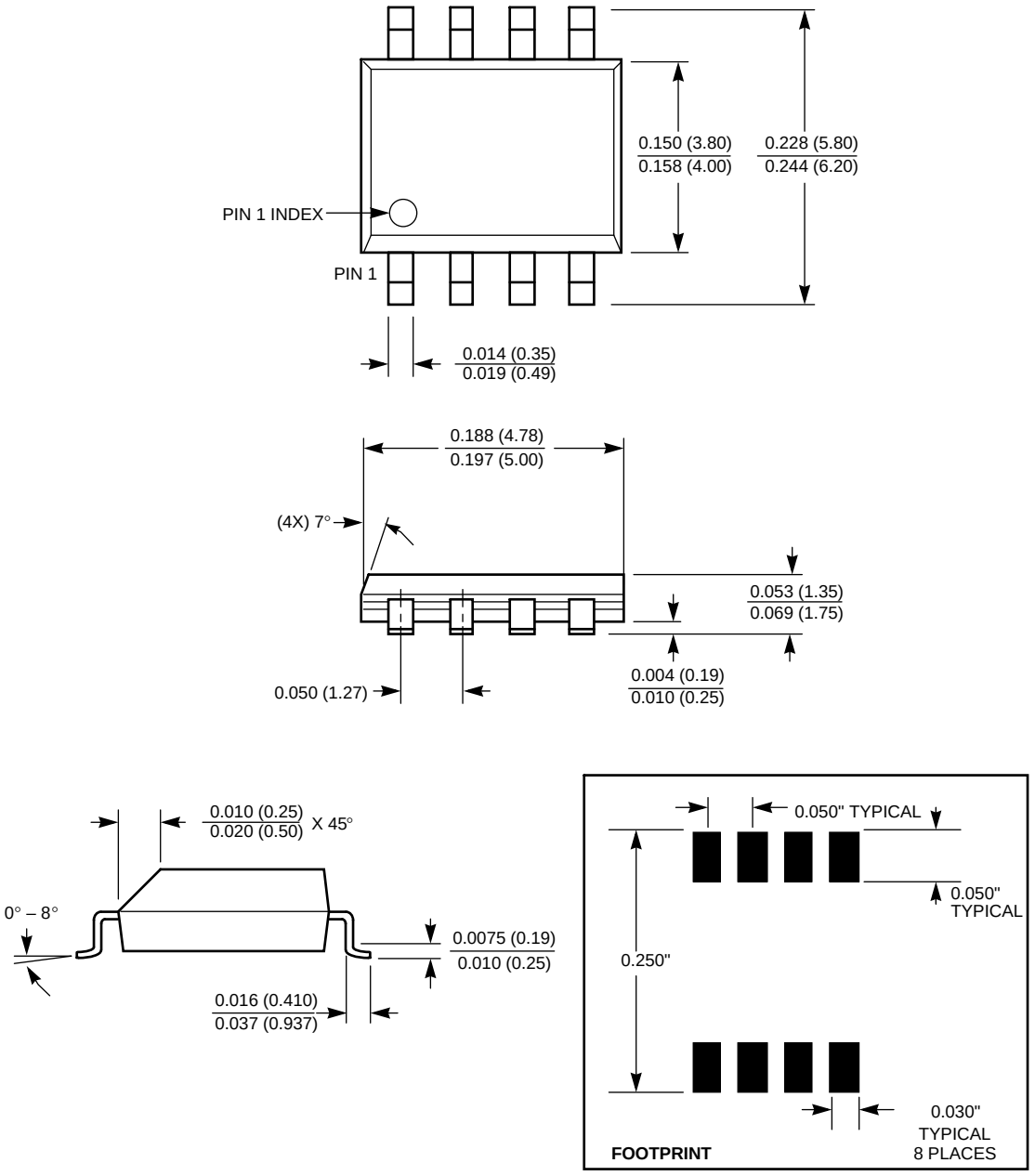


$\overline{WE}$ Controlled Write Cycle



PACKAGING INFORMATION

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

7030 FRM F12

ORDERING INFORMATION