APPLICATION NOTE
A V A I L A B L E
AN84

XICOR®

128K X24F128 16K x 8 Bit

2-Wire SerialFlash with Block Lock™ Protection

FEATURES

- **Save Critical Data with Programmable Block Lock Protection**
  - **—Block lock (0, 1/4, 1/2, or all of E^2PROM array)**
  - **—Software program protection**
  - **—Programmable hardware program protect**
- **In Circuit Programmable ROM Mode**
- **Longer Battery Life with Lower Power**
  - **—Active read current less than 1mA**
  - **—Active program current less than 3mA**
  - **—Standby current less than 1µA**
- **1.8V to 3.6V or 5V "Univolt" Read and Program Power Supply Versions**
- **32 Word Sector Program Mode**
  - **—Minimizes total program time per word**
- **100KHz 2-Wire Serial Interface**
- **Internally Organized 16K x 8**
- **Bidirectional Data Transfer Protocol**
- **Self-Timed Program Cycle**
  - **—Typical program cycle time of 5ms**
- **High Reliability**
  - **—Endurance: 100,000 cycles**
  - **—Data retention: 100 years**
- **8-Lead DIP**
- **16-Lead SOIC**

DESCRIPTION

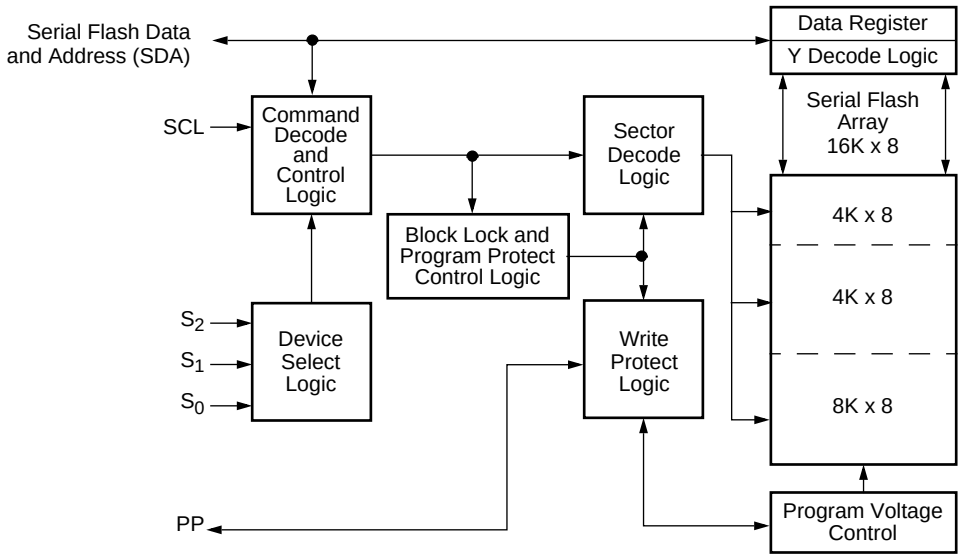
The X24F128 is a CMOS SerialFlash Memory, internally organized 16K x 8. The device features a serial interface and software protocol allowing operation on a simple two wire bus.

Three device select inputs (S_0–S_2) allow up to eight devices to share a common two wire bus.

A Program Protect Register at the address location FFFFh provides three program protection features: Software Program Protect, Block Lock Protect, and Hardware Program Protect. The Software Program Protect feature prevents any nonvolatile writes to the device until the PEL bit in the Program Protect Register is set. The Block Lock Protection feature allows the user to individually block protect four blocks of the array by programming two bits in the Program Protect Register. The Programmable Hardware Program Protect feature allows the user to install the device with PP tied to V_{CC}, program the entire memory array in circuit, and then enable the hardware program protection by programming a PPEN bit in the Program Protect Register. After this, selected blocks of the array, including the Program Protect Register itself, are permanently protected from being erased.

Xicor SerialFlash Memories are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-up resistor selection graph at the end of this data sheet.

Device Select (S_0, S_1, S_2)

The device select inputs (S_0, S_1, S_2) are used to set the first three bits of the 8-bit slave address. This allows up to eight devices to share a common bus. These inputs can be static or actively driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If actively driven, they must be driven with CMOS levels.

Program Protect (PP)

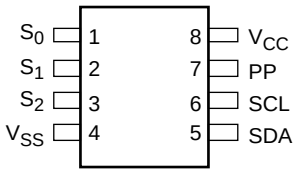
The Program Protect input controls the Hardware Program Protect feature. When held LOW, hardware program protection is disabled and the device can be programmed normally. When this input is held HIGH, and the PPEN bit in the Program Protect Register is set HIGH, program protection is enabled, and nonvolatile writes are disabled to the selected blocks as well as the Program Protect Register itself.

PIN NAMES

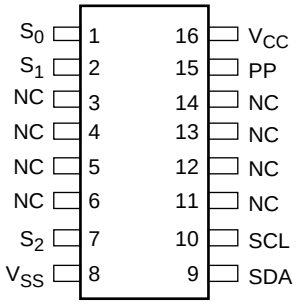
Symbol	Description
S_0, S_1, S_2	Device Select Inputs
SDA	Serial Data
SCL	Serial Clock
PP	Program Protect
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

PIN CONFIGURATION

8-Lead DIP & SOIC



16-Lead TSSOP



DEVICE OPERATION

The device supports a bidirectional, bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24F128 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

Figure 1. Data Validity

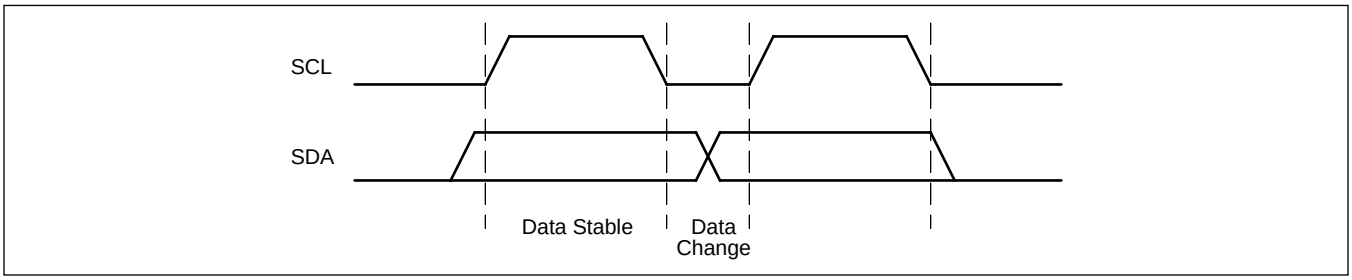
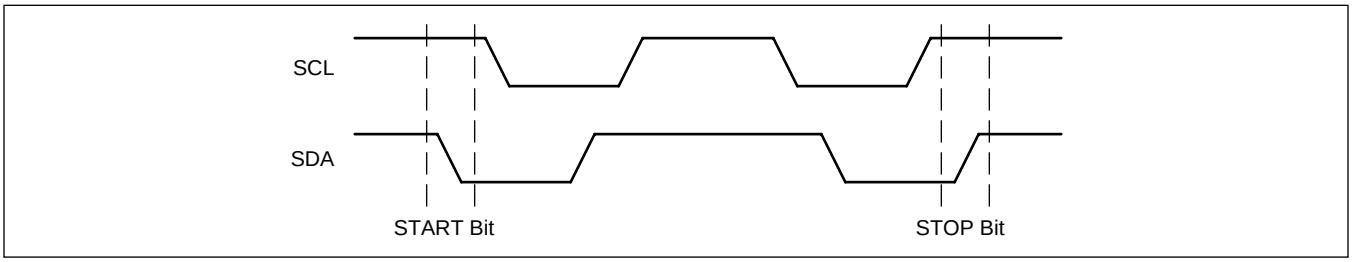


Figure 2. Definition of Start and Stop



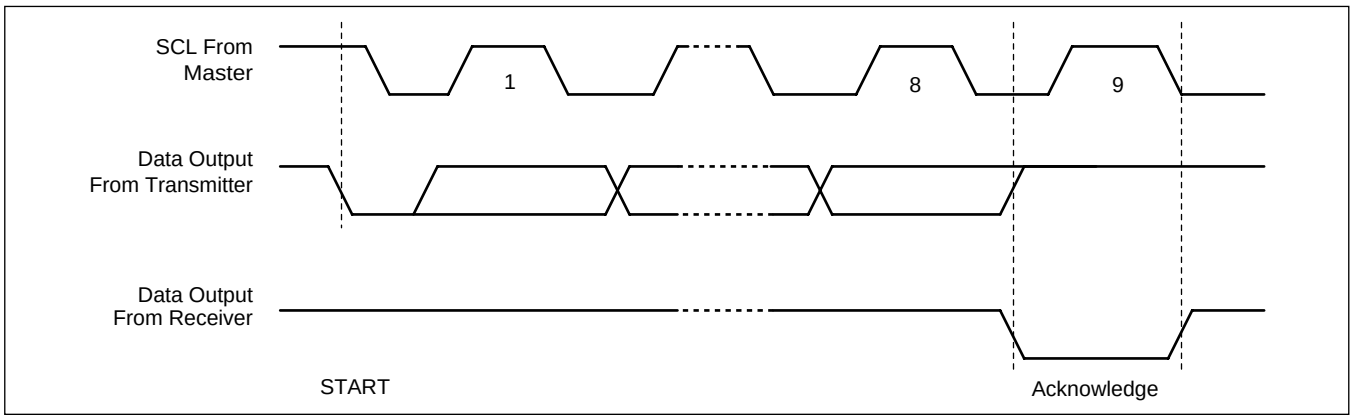
Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The device will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a program operation have been selected, the device will respond with an acknowledge after the receipt of each subsequent byte.

In the read mode the device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. If an acknowledge is not detected, the device will terminate further data transmissions. The master must then issue a stop condition to return the device to the standby power mode and place the device into a known state.

Figure 3. Acknowledge Response From Receiver



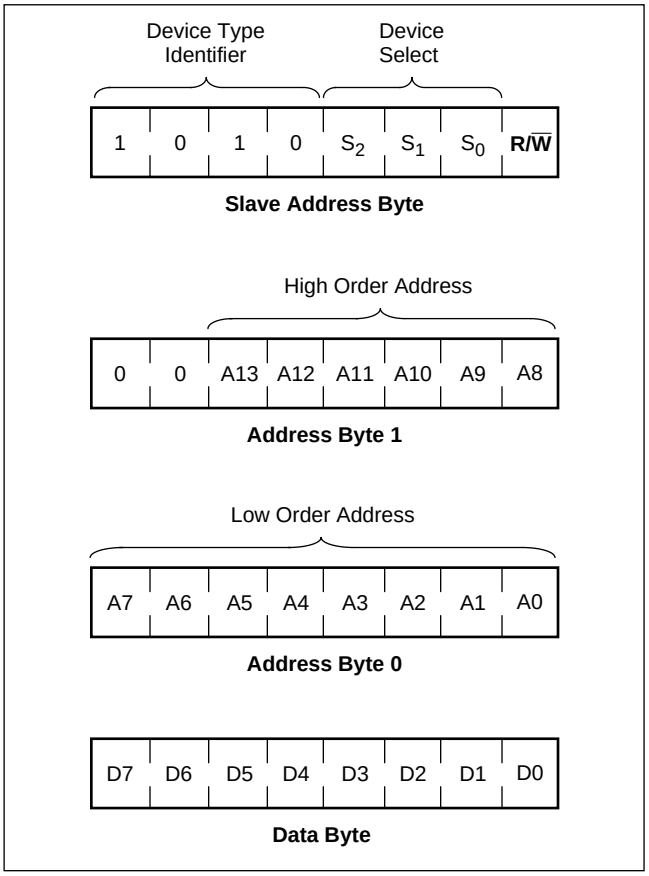
DEVICE ADDRESSING

Following a start condition, the master must output the address of the slave it is accessing. The first four bits of the Slave Address Byte are the device type identifier bits. These must equal “1010”. The next 3 bits are the device select bits S_0, S_1, and S_2. This allows up to 8 devices to share a single bus. These bits are compared to the S_0, S_1, and S_2 device select input pins. The last bit of the Slave Address Byte defines the operation to be performed. When the R/$\overline{W}$ bit is a one, then a read operation is selected. When it is zero then a program operation is selected. Refer to Figure 4. After loading the Slave Address Byte from the SDA bus, the device compares the device type bits with the value “1010” and the device select bits with the status of the device select input pins. If the compare is not successful, no acknowledge is output during the ninth clock cycle and the device returns to the standby mode.

The byte address is either supplied by the master or obtained from an internal counter, depending on the operation. When required, the master must supply the two Address Bytes as shown in Figure 4.

The internal organization of the E^2 array is 512 sectors by 32 bytes per sector. The sector address is partially contained in the Address Byte 1 and partially in bits 7 through 5 of the Address Byte 0. The specific byte address is contained in bits 4 through 0 of the Address Byte 0. Refer to Figure 4.

Figure 4. Slave Address

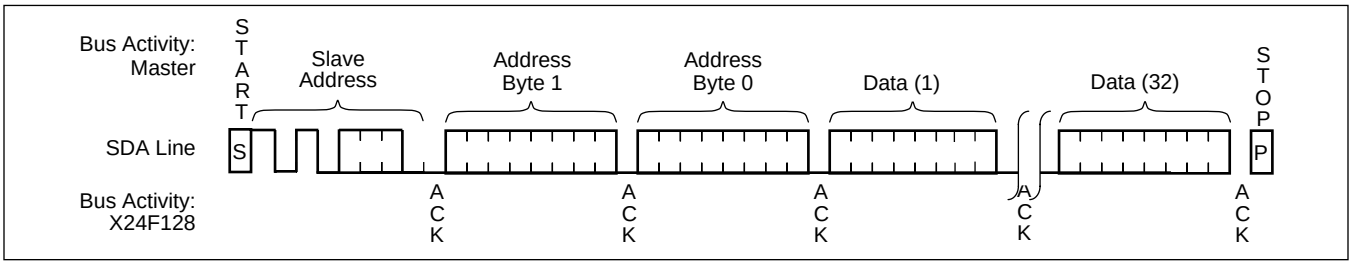


PROGRAMMING OPERATIONS

Sector Program Operation

The device executes a thirty-two byte sector program operation. For a sector program operation, the device requires the Slave Address Byte, Address Byte 1, and Address Byte 0. Address Byte 0 must contain the first byte of the sector to be programmed. Upon receipt of Address Byte 0, the device responds with an acknowledge, and waits for the first eight bits of data. After receiving the 8 bits of the first data byte, the device again responds with an acknowledge. The device will respond with an acknowledge after the receipt of each of 31 more bytes. Each time the byte address is internally incremented by one, while the sector address remains constant. When the counter reaches the end of the sector, the master terminates the data loading by issuing a stop condition, which causes the device to begin the nonvolatile write cycle. All inputs are disabled until completion of the nonvolatile write cycle. The SDA pin is at high impedance. Refer to Figure 5 for the address, acknowledge, and data transfer sequence.

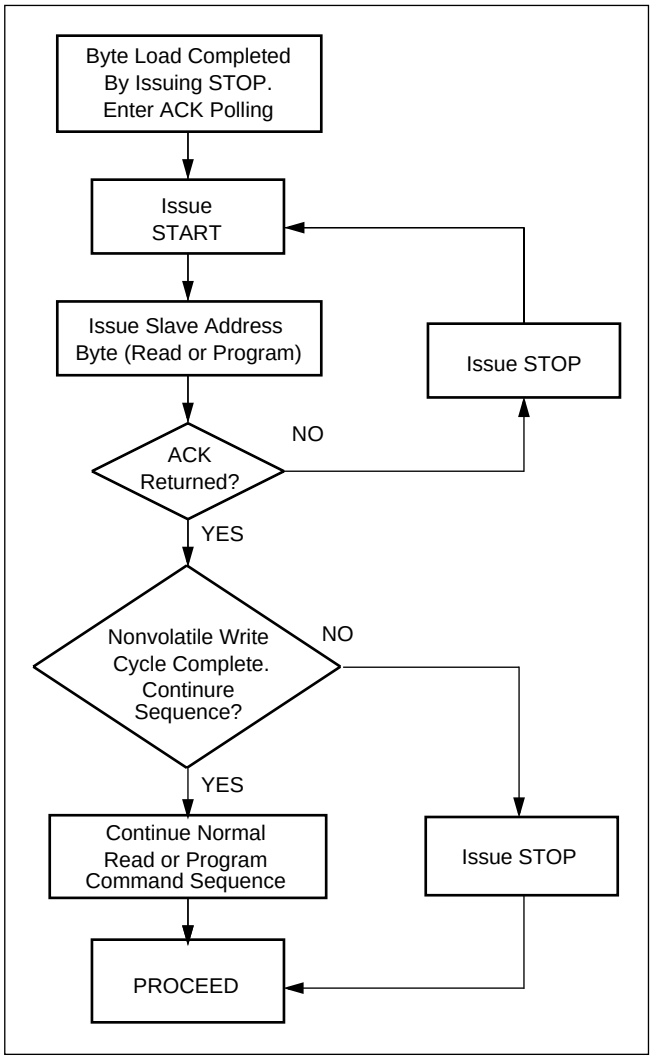
Figure 5. Sector Program Sequence



Acknowledge Polling

The maximum program cycle time can be significantly reduced using Acknowledge Polling. To initiate Acknowledge Polling, the master issues a start condition followed by the Slave Address Byte for a program or read operation. If the device is still busy with the nonvolatile write cycle, then no ACK will be returned. If the device has completed the nonvolatile write operation, an ACK will be returned and the host can then proceed with the read or program operation. Refer to Figure 6.

Figure 6. ACK Polling Sequence



READ OPERATIONS

Read operations are initiated in the same manner as program operations with the exception that the R/$\overline{W}$ bit of the Slave Address Byte is set to one. There are three basic read operations: Current Address Reads, Random Reads, and Sequential Reads.

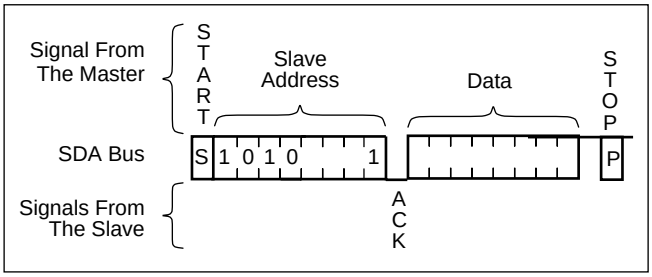
Current Address Read

Internally, the device contains an address counter that maintains the address of the last byte read or programmed, incremented by one. After a read operation from the last address in the array, the counter will “roll over” to the first address in the array. After a program operation to the last address in a given sector, the counter will “roll over” to the first address of the same sector.

Upon receipt of the Slave Address Byte with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and then transmits the byte at the current address. The master terminates the read operation when it does not respond with an acknowledge during the ninth clock and then issues a stop condition. Refer to Figure 7 for the address, acknowledge, and data transfer sequence.

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Figure 7. Current Address Read



Random Read

Random read operation allows the master to access any memory location in the array. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to one, the master must first perform a “Dummy” program operation. The master issues the start condition and the Slave Address Byte with the R/$\overline{W}$ bit low, receives an acknowledge, then issues Address Byte 1, receives another acknowledge, then issues Address Byte 0 containing the address of the byte to be read. After the device acknowledges receipt of Address Byte 0, the master issues another start condition and the Slave Address Byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge and then eight bits of data from the device. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. Refer to Figure 8 for the address, acknowledge, and data transfer sequence.

The device will perform a similar operation called “Set Current Address” if a stop is issued instead of the second start shown in Figure 9. The device will go into standby mode after the stop and all bus activity will be ignored until a start is detected. The effect of this operation is that the new address is loaded into the address counter, but no data is output by the device.

The next Current Address Read operation will read from the newly loaded address.

Figure 8. Random Read Sequence

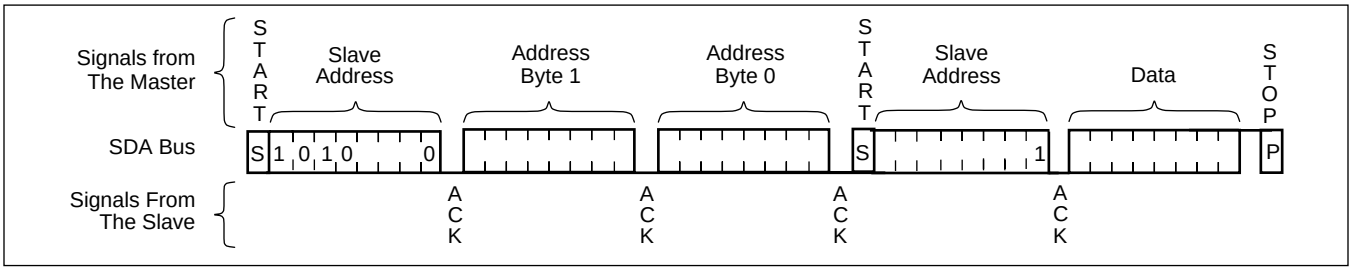
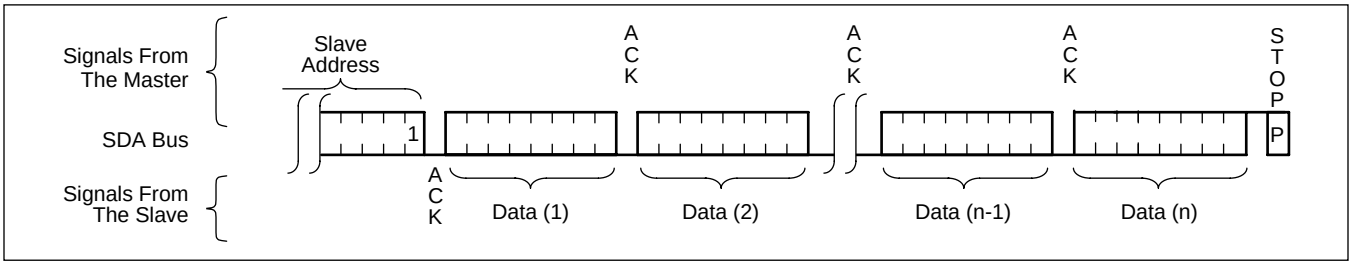


Figure 9. Sequenctial Read Sequence



Sequential Read

Sequential reads can be initiated as either a current address read or random read. The first byte is transmitted as with the other modes; however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. The address counter for read operations increments through all byte addresses, allowing the entire memory contents to be read during one operation. At the end of the address space the counter “rolls over” to address 0000h and the device continues to output data for each acknowledge received. Refer to Figure 9 for the acknowledge and data transfer sequence.

PROGRAM PROTECT REGISTER (PPR)

Register Program Operation

The Program Protect Register can only be modified by programming one data byte directly to the address FFFFh as described below.

The data byte must contain zeroes where indicated in the procedural descriptions below; otherwise the operation will not be performed. Only one data byte is allowed for each Register Program Operation. The part will not acknowledge any data bytes after the first byte

is entered. The user then has to issue a stop to initiate the nonvolatile write cycle that programs BL0, BL1, and PPEN to the nonvolatile bits. A stop must also be issued after volatile register program operations to put the device into Standby.

The state of the Program Protect Register can be read by performing a random read at FFFFh at any time. The part will reset itself after the first byte is read. The master should supply a stop condition to be consistent with the protocol. After the read, the address counter contains 0000h.

Program Protect Register: PPR (ADDR = $FFFF_h$)

7	6	5	4	3	2	1	0
PPEN	0	0	BL1	BL0	RPEL	PEL	0

PEL: Program Enable Latch (Volatile)

0 = PEL reset, programming disabled.

1 = PEL set, programming enabled.

RPEL: Register Program Enable Latch (Volatile)

0 = RPEL reset, programs to the Program Protect Register disabled.

1 = RPEL set, programs to the Program Protect Register enabled.

BL0, BL1: Block Lock Protect Bits (Nonvolatile)

The Block Lock Protect Bits, BL0 and BL1, determine which blocks of the array are protected. A program to a protected block of memory is ignored, but will receive an acknowledge. The master must issue a stop to put the part into standby, just as it would for a valid program; but the stop will not initiate an internal nonvolatile write cycle. See Figure 10.

PPEN: Program Protect Enable Bit (Nonvolatile)

The Program Protect ($\overline{PP}$) pin and the Program Protect Enable (PPEN) bit in the Program Protect Register control the Programmable Hardware Program Protection feature. Hardware Program Protection is enabled when the $\overline{PP}$ pin is HIGH and the PPEN bit is HIGH, and disabled when either the $\overline{PP}$ pin is LOW or the PPEN bit is LOW. When the chip is Hardware Program Protected, nonvolatile writes are disabled to the Program Protect Register, including the Block Lock Protect bits and the PPEN bit itself, as well as to the Block Lock protected sections in the memory array. Only the sections of the memory array that are not Block Lock protected, and the volatile bits PEL and RPEL, can be programmed.

In Circuit Programmable ROM Mode

Note that since the PPEN bit is program protected, it cannot be changed back to a LOW state; so program protection is enabled as long as the PP pin is held HIGH. Thus an In Circuit Programmable ROM function can be implemented by hardwiring the PP pin to V_{CC}, programming and Block Locking the desired portion of the array to be ROM, and then programming the PPEN bit HIGH. Figure 11 defines the program protect status for each combination of PPEN and PP.

Programming the PEL and RPEL Bits

PEL and RPEL are volatile latches that power up in the LOW (disabled) state. While the PEL bit is LOW, program operations to any address other than FFFFh will be ignored (no acknowledge will be issued after the data byte). The PEL bit is set by programming 00000010 to address FFFFh. Once set, PEL remains HIGH until either it is reset to 0 (by programming 00000000 to FFFFh) or until power cycles. Programming PEL and RPEL does not cause a nonvolatile write cycle, so the device is ready for the next operation immediately after the stop condition.

The RPEL bit controls programming to the Block Lock Protect bits, BL0 and BL1, and the PPEN bit. If RPEL is 0 then no programming operations can be performed on BL0, BL1, or PPEN. RPEL is reset when power cycles or after any nonvolatile write, including those to the Block Lock Protect bits, the PPEN bit, or any sector in the memory array. RPEL must be reset before PEL can be reset. RPEL and PEL cannot be reset in one program operation. RPEL can also be reset by programming u00xy010 to FFFFh ONLY when the PPR is NOT protected. This is the same operation as in step 3 described below, and will result in programming BL0, BL1, and PPEN.

Programming to the BL and PPEN Bits

A 3 step sequence is required to change the nonvolatile Block Lock Protect or Program Protect Enable bits:

1) Set PEL=1, Program 00000010 to address FFFFh (Volatile Write Cycle.)

2) Set RPEL=1, Program 00000110 to address FFFFh (Volatile Write Cycle.)

3) Set BL1, BL0, and/or PPEN bits, Program u00xy010 to address FFFFh, where u=PPEN, x=BL1, and y=BL0. (Nonvolatile Write Cycle.)

The three step sequence was created to make it difficult to change the contents of the Program Protect Register accidentally. If PEL was set to one by a previous register program operation, the user may start at step 2. RPEL is reset to zero in step 3 so that user is required to perform steps 2 and 3 to make another change. RPEL must be 0 in step 3. If the RPEL bit in the data byte for step 3 is a one, then no changes are made to the Program Protect Register and the device remains at step 2.

The PP pin must be LOW or the PPEN bit must be LOW before a nonvolatile register program operation is initiated. Otherwise, the program operation will abort and the device will go into standby mode after the master issues the stop condition in step 3.

Step 3 is a nonvolatile write operation, requiring 10mS max to complete (acknowledge polling may be used to reduce this time requirement). It should be noted that step 3 MUST end with a stop condition. If a start condition is issued during or at the end of step 3 (instead of a stop condition) the device will abort the nonvolatile register program and remain at step 2. If the operation is aborted with a start condition, the master must issue a stop to put the device into standby mode.

Table 1. Block Lock Protect Bits and Protected Addresses

BL1	BL0	Protected Addresses	Array Location
		X24F128	
0	0	None	No Protect
0	1	3000h - 3FFFh	Upper 1/4
1	0	2000h - 3FFFh	Upper 1/2
1	1	0000h - 3FFFh	Full Array

Table 2. PP Pin and PPEN Bit Functionality

PP	PPEN	Memory Array Not Lock Block Protected	Memory Array Block Lock Protected	Block Lock Bits	PPEN Bit
0	X	Programmable	Protected	Programmable	Programmable
X	0	Programmable	Protected	Programmable	Programmable
1	1	Programmable	Protected	Protected	Protected

ABSOLUTE MAXIMUM RATINGS

Temperature under bias
X24F128 .....–65 to +135°C
Storage Temperature.....–65 to +150°C
Voltage on any pin with respect to V_{SS}.....–1V to +7V
D.C. output current 5mA
Lead temperature (soldering, 10 seconds).....300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Extended	–20°C	+85°C

Supply Voltage	Limits
X24F128	1.8V to 3.6V
X24F128–5	4.5V to 5.5V

D.C. OPERATING CHARACTERISTICS

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	SCL = V_{CC} X 0.1/V_{CC} X 0.9 Levels @ 100KHz, SDA = Open, All Other Inputs = V_{SS} or V_{CC} – 0.3V
I_{CC2}	V_{CC} Supply Current (Program)		3	mA	
I_{SB1}(1)	V_{CC} Standby Current		10	µA	SCL = SDA = V_{CC} – 0.3V, All Other Inputs = V_{SS} or V_{CC} – 0.3V, V_{CC} = 5V ± 10%
I_{SB2}(1)	V_{CC} Standby Current		1	µA	SCL = SDA = V_{CC} – 0.1V, All Other Inputs = V_{SS} or V_{CC} – 0.1V, V_{CC} = 1.8V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(2)	Input LOW Voltage	–0.5	V_{CC} x 0.3	V	
V_{IH}(2)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 3mA
V_{hys}(3)	Hysteresis of Schmitt Trigger Inputs	V_{CC} x 0.05		V	

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

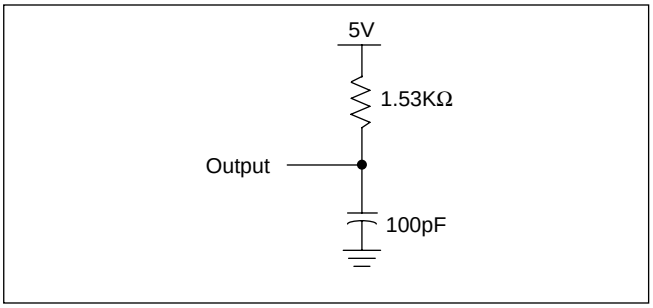
Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (S_0, S_1, S_2, SCL, PP)	6	pF	V_{IN} = 0V

Notes: (1) Must perform a stop command prior to measurement.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not 100% tested.
(3) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing levels	V_{CC} X 0.5

EQUIVALENT A.C. LOAD CIRCUIT



A.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read & Program Cycle Limits

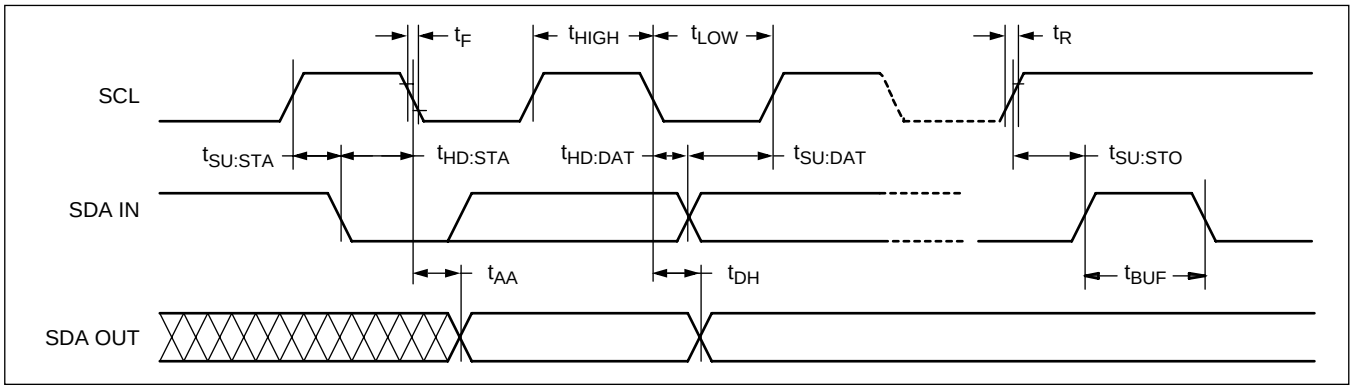
Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs	50	100	ns
t_{AA}	SCL LOW to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4		µs
t_{LOW}	Clock LOW Period	4.7		µs
t_{HIGH}	Clock HIGH Period	4		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

POWER-UP TIMING(4)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	5	ms

Notes: (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Bus Timing



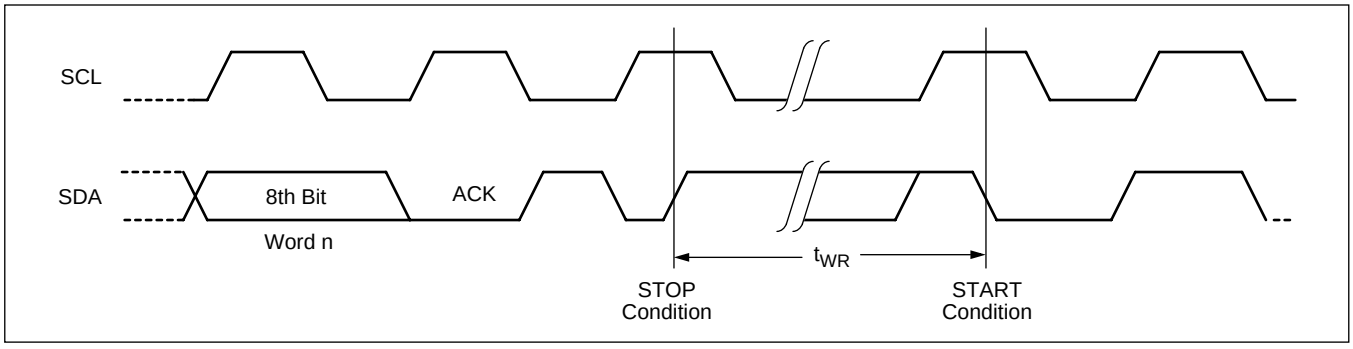
Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{WC}(6)	Write Cycle Time		5	10	ms

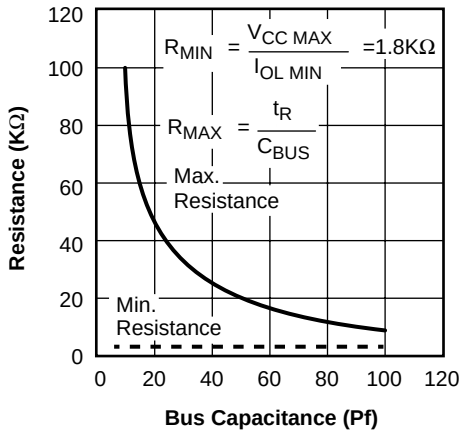
Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage (5V).
(6) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/write cycle. During the write cycle, the X24F128 bus interface circuits are disabled, SDA is allowed to remain HIGH, and the device does not respond to its slave address.

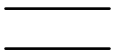
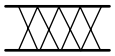
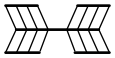
Bus Timing



Guidelines for Calculating Typical Values of Bus Pull-Up Resistors

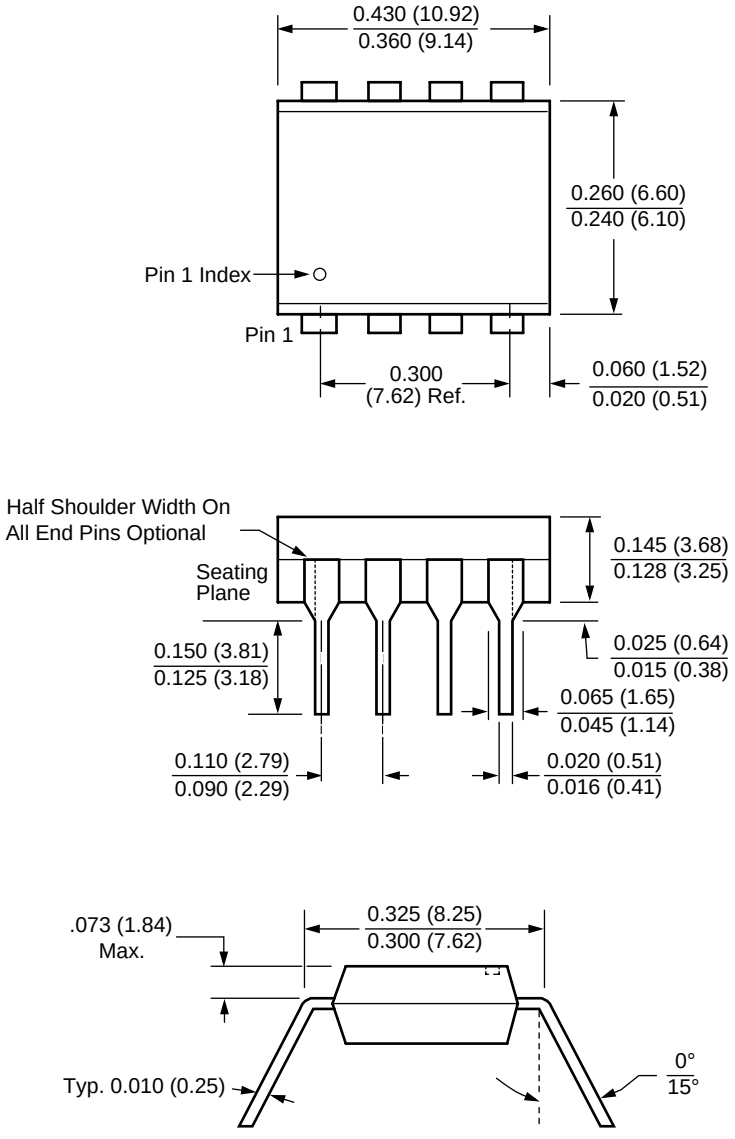


Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

PACKAGING INFORMATION

8-Lead Plastic Dual In-Line Package Type P

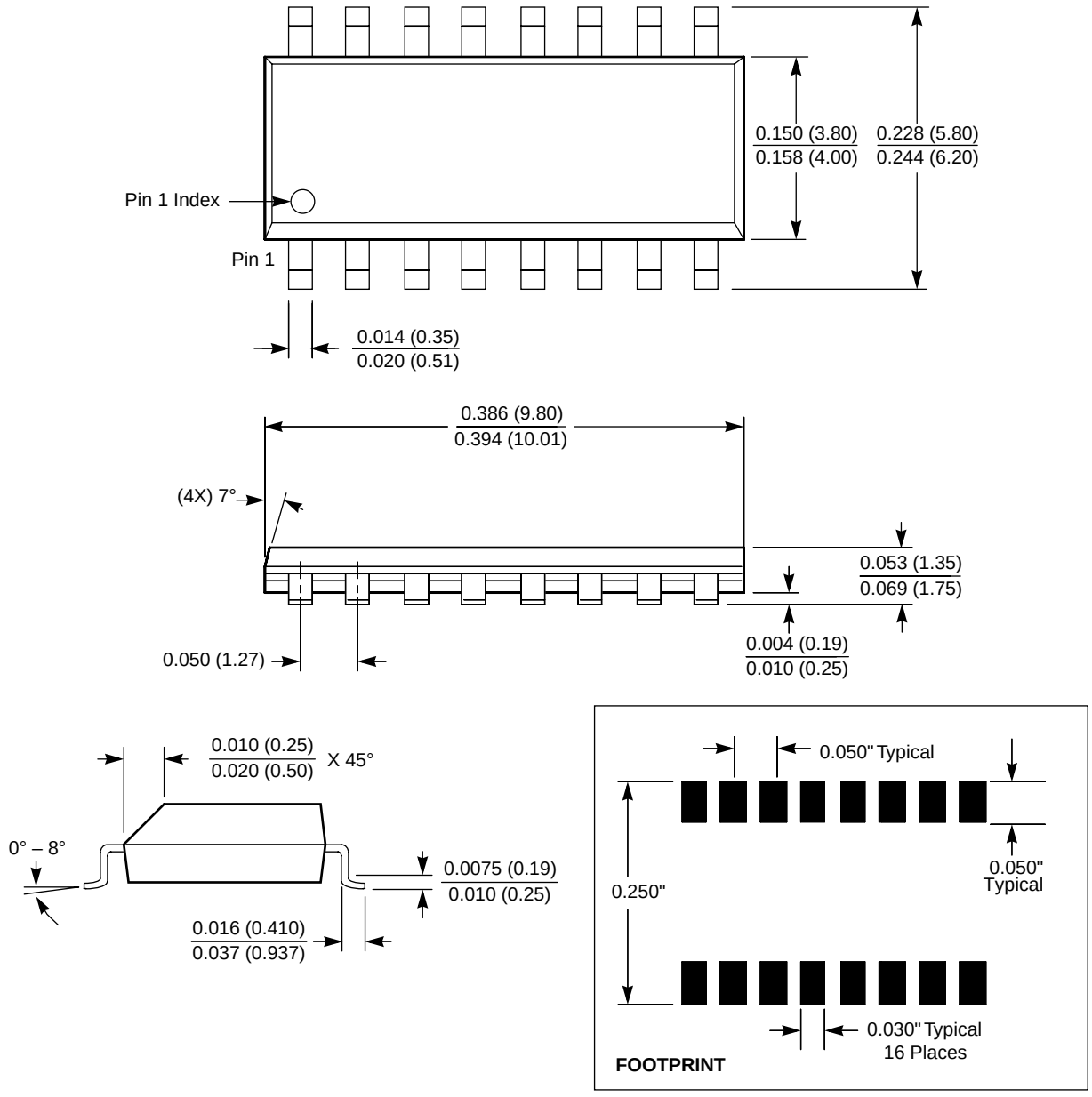


NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

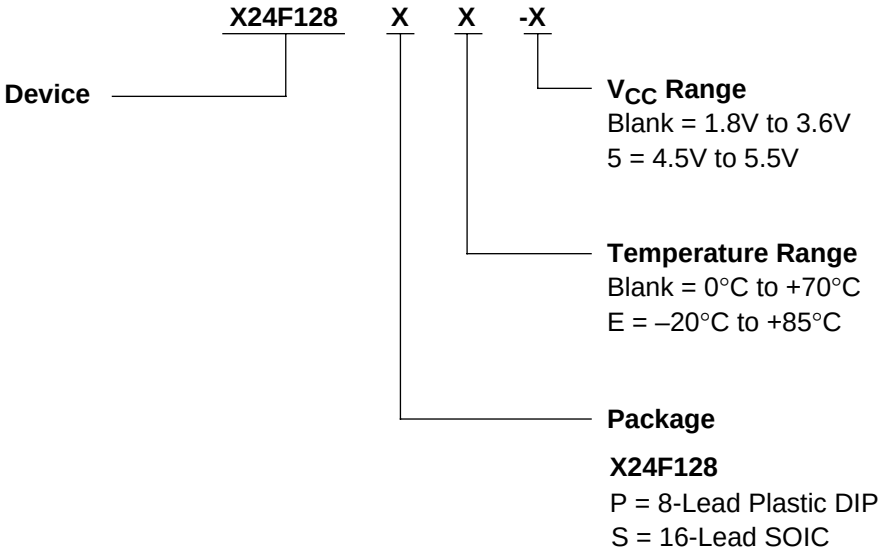
PACKAGING INFORMATION

16-Lead Plastic Small Outline Gull Wing Package Type S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Ordering Information



Part Mark Convention