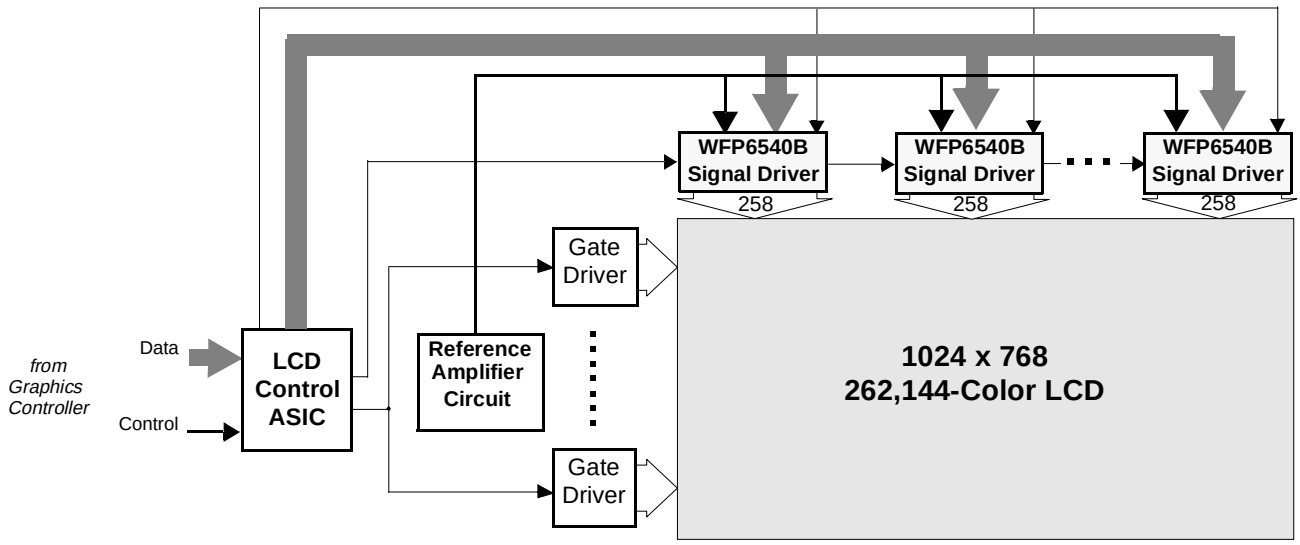
1. PRODUCT DESCRIPTION

COG Signal Driver

258-Channel, 6-Bit Signal Driver for XGA COG Applications

The WFP6540B is a 6-bit, 258-channel signal driver designed for 11.x and 12.x XGA chip-on-glass (COG) TFT-LCDs. The WFP6540B's minimum form factor and optimized COG layout permit the design of high-display-quality, low-power 6-bit TFT-LCD's with minimum bezel area.

The WFP6540B's internal architecture includes a resistor-string DAC with the value of the individual resistor segments weighted to reduce signal driver power dissipation by as much as 20% to 40% when compared to non-weighted resistor string DAC architectures.



2. FEATURES & BENEFITS

Features	Benefits
• Full Color Display	• 64 gray scales per primary color • 262,144 (256K) color palette
• High Speed Operation • 65 MHz (**3.3 V** and 5.0V logic supply)	• Support for wide range of color LCD resolutions • Single driver bank supports up to 1024 x 768
• Minimum Form Factor • 17.35 mm x 1.26 mm • 64 μm output pitch • 675 μm ± 25 μm chip thickness	• Minimum Bezel Size
• High Integration • 258 output voltage channels • Bi-directional shift register	• Minimizes external components and circuitry • 12 drivers for 1024x768 color LCDs • Easy re-configuration from backlit operation to over-head projector (OHP) operation
• Data Inversion Feature	• Data inversion capability enables a complete internal solution for Vcom modulation by data inversion. • May be used to reduce data transitions.
• Low-power operation • Logic Supply: 3.3 V ± 0.3 or 5.0 V ± 0.5 • Analog Supply: 3.3 V ± 0.3 to 5.0 V ± 0.5 • Automatic standby function	• Extends battery-based operation • Low power and EMI from 3.3 V operation • Minimum dynamic-power dissipation
• Excellent Output Uniformity	• Output Error (max) ± 0.15 LSB
• Weighted R-String: See Figure 2-1 & Table 2-1	• Reduces Power Dissipation 20-40% or more. • Reduces dc current drive requirements of external reference amplifiers

- Rseg Value
  - Internal weighted R-String for low power operation (see Table 2-1 and Figure 2-1).

Table 2-1: Weighted R_{SEG} Values (ignoring bus resistance)

R-Segment	Proportion	Value
V7 ~ V8 (V55~V63)	2x	20Ω,20Ω,20Ω,20Ω,20Ω,20Ω,20Ω,20Ω
V6 ~V7	1.2x	12 Ω X 8
V5 ~V6	1x	10 Ω X 8
V4 ~V5	1x	10 Ω X 8
V3 ~V4	1x	10 Ω X 8
V2 ~V3	1x	10 Ω X 8
V1 ~V2	1.2x	12 Ω X 8
V0 ~V1 (V00~V07)	1.75x	20Ω, 20Ω 20Ω, 20Ω, 20Ω, 20Ω, 20Ω

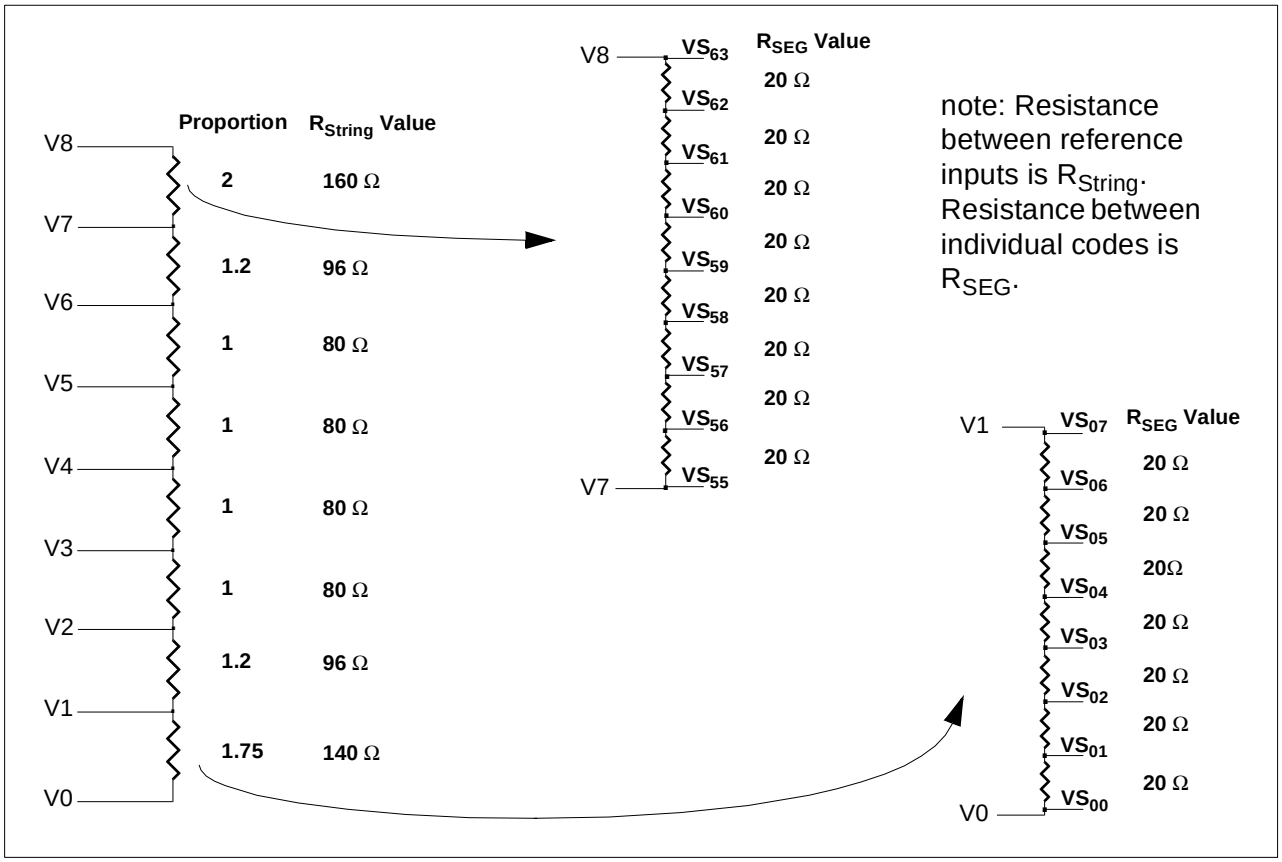


Figure 2-1: Weighted R-String Detail

3. WFP6540B DIMENSIONS & SPECIFICATIONS

3.1. DIE DIMENSIONS

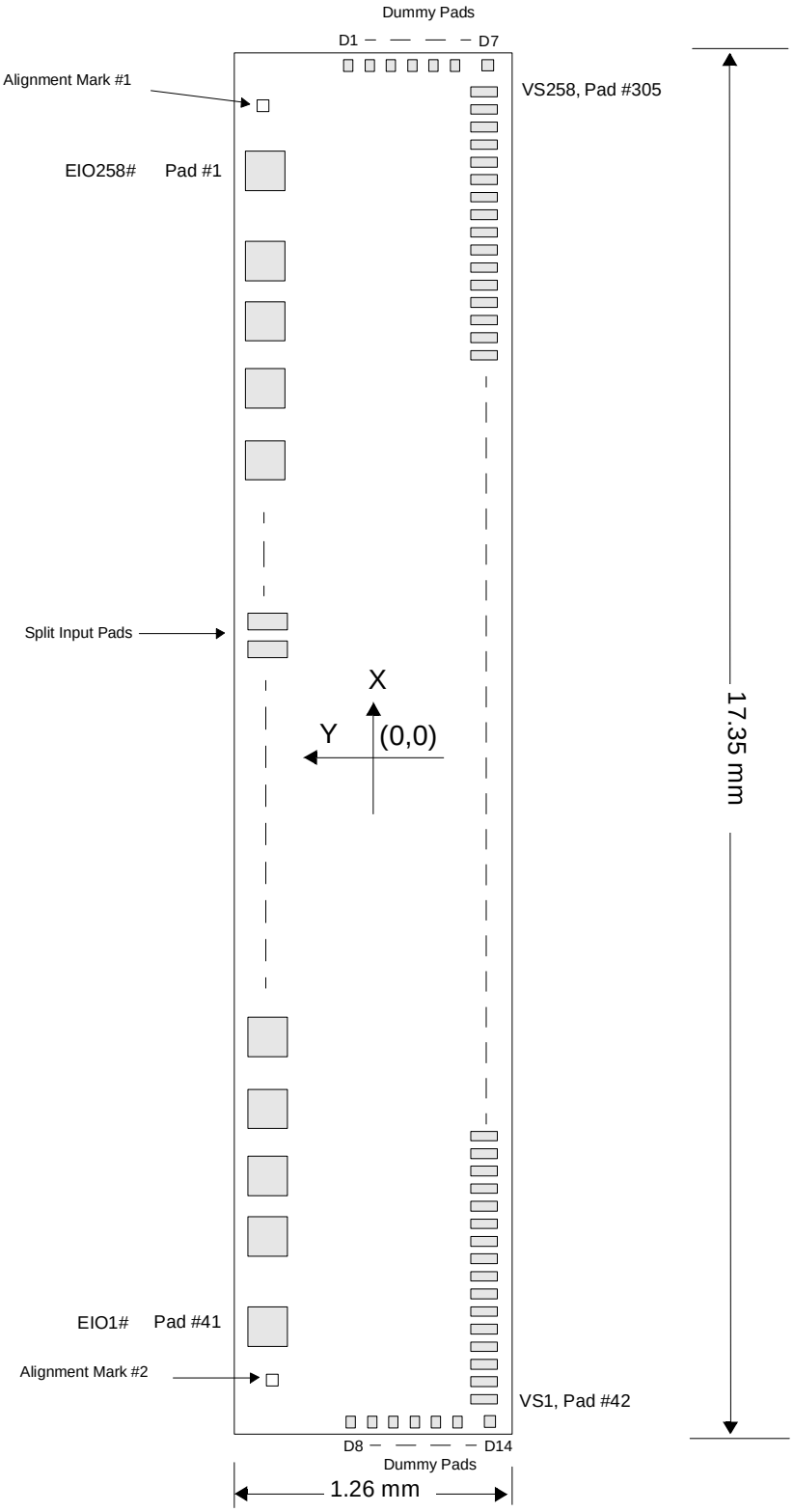


Figure 3-1: FP6530B Die

3.2. Bump Specifications

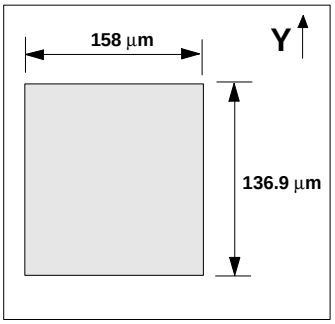


Figure 3-2: Single Input Pad Bump

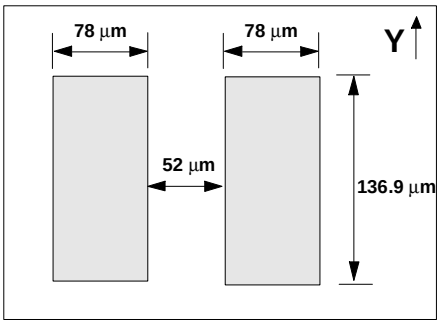


Figure 3-3: Split Input Pad Bump

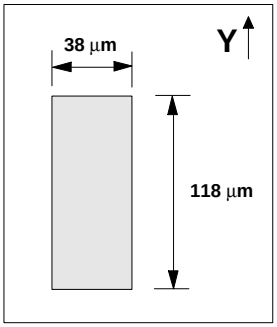


Figure 3-4: Output Pad Bump

Table 3–1. Dummy Bump Sizes

Name	Pad #	Size (Y by X) μm
D7,D14	306,319	73 by 73
D1,D8	312,313	43 by 73
D6-D2,D9-D13	307-311,314-318	53 by 73

- Bump Height: 15 μm ± 2 μm
- Bump Dimple: less than 2 μm (see Figure 3-5)
- Bump Material: Gold
- Bump Hardness: 30 HV ~ 80 HV,
- Bump Shape: Tapered wall, 80° ± 5 angle to plane of top of die

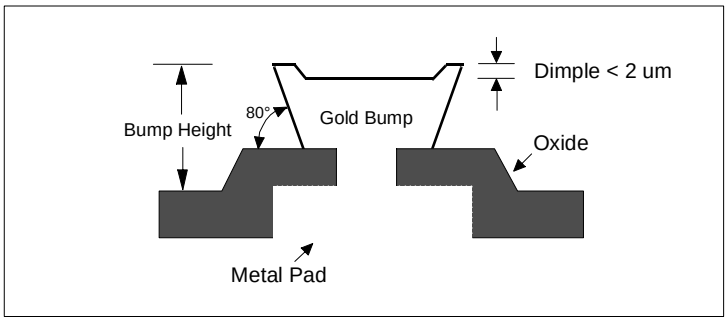
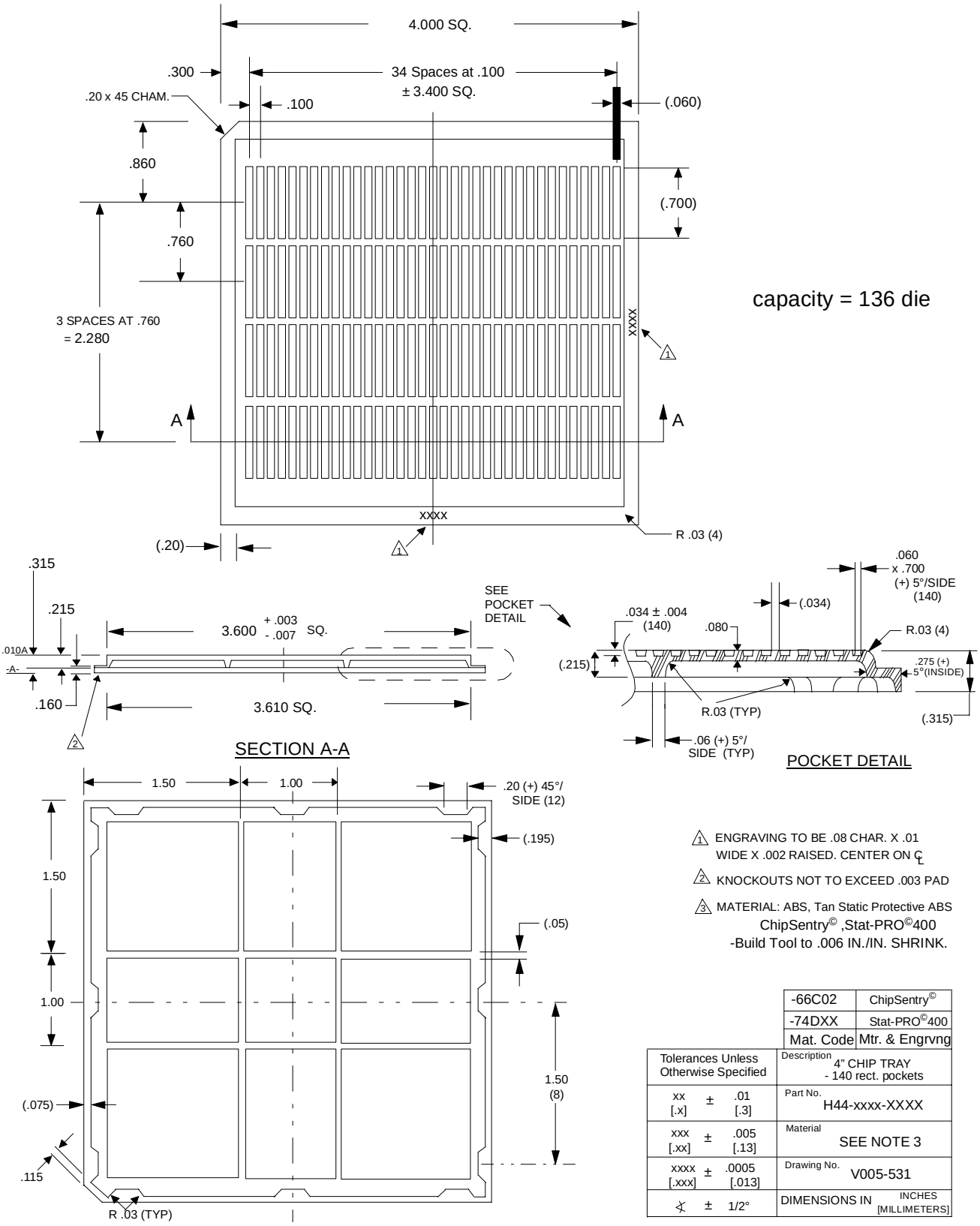


Figure 3-5: Bump Specification Definitions

3.3. Alignment Mark Coordinates

Coordinates		
Mark	X	Y
#1	8363.20	441.3
#2	-8363.20	441.3

3.4. Waffle Pack Specification



1. ENGRAVING TO BE .08 CHAR. X .01 WIDE X .002 RAISED. CENTER ON ℄
2. KNOCKOUTS NOT TO EXCEED .003 PAD
3. MATERIAL: ABS, Tan Static Protective ABS ChipSentry© ,Stat-PRO©400 -Build Tool to .006 IN./IN. SHRINK.

-66C02	ChipSentry©
-74DXX	Stat-PRO©400
Mat. Code	Mtr. & Engrvng

Tolerances Unless Otherwise Specified	Description: 4" CHIP TRAY - 140 rect. pockets
xx [.x] ± .01 [.3]	Part No.: H44-xxxx-XXXX
xxx [.xx] ± .005 [.13]	Material: SEE NOTE 3
xxxx [.xxx] ± .0005 [.013]	Drawing No.: V005-531
∠ ± 1/2°	DIMENSIONS IN INCHES [MILLIMETERS]

4. PAD INFORMATION

4.1. Input Bond Pad Coordinates

Pad #	Signal	x Coordinate (in μm)	y Coordinate (in μm)	Pad Type
1	EIO258#	8174.2	436.55	Single
2	D_{25}	7570.0	436.55	Single
3	D_{24}	7221.8	436.55	Single
4	D_{23}	6791.0	436.55	Single
5	D_{22}	6442.8	436.55	Single
6	D_{21}	5988.8	436.55	Single
7	D_{20}	5640.6	436.55	Single
8	D_{15}	5209.8	436.55	Single
9	LD258_1	4909.8	436.55	Single
10.1	V_0	4492.2	436.55	Split
10.2	V_0	4362.2	436.55	Split
11.1	V_8	4069.4	436.55	Split
11.2	V_8	3939.4	436.55	Split
12	2xCLK	3560.6	436.55	Single
13	D_{14}	3212.4	436.55	Single
14	D_{13}	2864.2	436.55	Single
15	DCLK	2556.0	436.55	Single
16.1	V_{DDD}	2127.8	436.55	Split
16.2	V_{DDD}	1997.8	436.55	Split
17.1	V_{DDA}	1722.8	436.55	Split
17.2	V_{DDA}	1592.8	436.55	Split
18.1	V_7	1300.0	436.55	Split
18.2	V_7	1170.0	436.55	Split
19.1	V_2	792.4	436.55	Split
19.2	V_2	662.4	436.55	Split
20.1	V_5	369.6	436.55	Split
20.2	V_5	239.6	436.55	Split
21.1	V_4	-138.0	436.55	Split
21.2	V_4	-268.0	436.55	Split
22.1	V_3	-560.8	436.55	Split
22.2	V_3	-690.8	436.55	Split
23.1	V_6	-983.6	436.55	Split
23.2	V_6	-1113.6	436.55	Split
24.1	V_1	-1406.4	436.55	Split
24.2	V_1	-1536.4	436.55	Split
25.1	A_{GND}	-1848.6	436.55	Split
25.2	A_{GND}	-1978.6	436.55	Split
26.1	D_{GND}	-2290.8	436.55	Split
26.2	D_{GND}	-2420.8	436.55	Split
27	D_{12}	-2729.0	436.55	Single
28	D_{11}	-3077.2	436.55	Single
29	D_{10}	-3531.2	436.55	Single
30	CLAMP#	-3867.4	436.55	Single
31.1	V_8	-4206.4	436.55	Split
31.2	V_8	-4336.4	436.55	Split
32.1	V_0	-4629.2	436.55	Split
32.2	V_0	-4759.2	436.55	Split
33	DATA_INV	-5140.2	436.55	Single
34	LP	-5440.2	436.55	Single
35	D_{05}	-5871.0	436.55	Single
36	D_{04}	-6219.2	436.55	Single
37	D_{03}	-6673.2	436.55	Single
38	D_{02}	-7021.4	436.55	Single
39	D_{01}	-7369.6	436.55	Single
40	D_{00}	-7717.8	436.55	Single
41	EIO1#	-8176.2	436.55	Single

Table 4-1: WFP6540B Input Bond Pad Coordinates

4.2. Output Bond Pad Coordinate

Table 4–2: Output Bond Pad Coordinates

Pad #	Signal	X coor.	Y coor.
42	VS1	-8416.0	-450.1
43	VS2	-8352.0	-450.1
44	VS3	-8288.0	-450.1
45	VS4	-8224.0	-450.1
46	VS5	-8160.0	-450.1
47	VS6	-8096.0	-450.1
48	VS7	-8032.0	-450.1
49	VS8	-7968.0	-450.1
50	VS9	-7904.0	-450.1
51	VS10	-7840.0	-450.1
52	VS11	-7776.0	-450.1
53	VS12	-7712.0	-450.1
54	VS13	-7648.0	-450.1
55	VS14	-7584.0	-450.1
56	VS15	-7520.0	-450.1
57	VS16	-7456.0	-450.1
58	VS17	-7392.0	-450.1
59	VS18	-7328.0	-450.1
60	VS19	-7264.0	-450.1
61	VS20	-7200.0	-450.1
62	VS21	-7136.0	-450.1
63	VS22	-7072.0	-450.1
64	VS23	-7008.0	-450.1
65	VS24	-6944.0	-450.1
66	VS25	-6880.0	-450.1
67	VS26	-6816.0	-450.1
68	VS27	-6752.0	-450.1
69	VS28	-6688.0	-450.1
70	VS29	-6624.0	-450.1
71	VS30	-6560.0	-450.1
72	VS31	-6496.0	-450.1
73	VS32	-6432.0	-450.1
74	VS33	-6368.0	-450.1
75	VS34	-6304.0	-450.1
76	VS35	-6240.0	-450.1
77	VS36	-6176.0	-450.1
78	VS37	-6112.0	-450.1
79	VS38	-6048.0	-450.1

Table 4–2: Output Bond Pad Coordinates

Pad #	Signal	X coor.	Y coor.
80	VS39	-5984.0	-450.1
81	VS40	-5920.0	-450.1
82	VS41	-5856.0	-450.1
83	VS42	-5792.0	-450.1
84	VS43	-5728.0	-450.1
85	VS44	-5664.0	-450.1
86	VS45	-5600.0	-450.1
87	VS46	-5536.0	-450.1
88	VS47	-5472.0	-450.1
89	VS48	-5408.0	-450.1
90	VS49	-5344.0	-450.1
91	VS50	-5280.0	-450.1
92	VS51	-5216.0	-450.1
93	VS52	-5152.0	-450.1
94	VS53	-5088.0	-450.1
95	VS54	-5024.0	-450.1
96	VS55	-4960.0	-450.1
97	VS56	-4896.0	-450.1
98	VS57	-4832.0	-450.1
99	VS58	-4768.0	-450.1
100	VS59	-4704.0	-450.1
101	VS60	-4640.0	-450.1
102	VS61	-4576.0	-450.1
103	VS62	-4512.0	-450.1
104	VS63	-4448.0	-450.1
105	VS64	-4384.0	-450.1
106	VS65	-4320.0	-450.1
107	VS66	-4256.0	-450.1
108	dummy	-4192.0	-450.1
109	dummy	-4128.0	-450.1
110	dummy	-4064.0	-450.1
111	VS67	-4000.0	-450.1
112	VS68	-3936.0	-450.1
113	VS69	-3872.0	-450.1
114	VS70	-3808.0	-450.1
115	VS71	-3744.0	-450.1
116	VS72	-3680.0	-450.1
117	VS73	-3616.0	-450.1
118	VS74	-3552.0	-450.1
119	VS75	-3488.0	-450.1

Table 4–2: Output Bond Pad Coordinates

Pad #	Signal	X coor.	Y coor.
120	VS76	-3424.0	-450.1
121	VS77	-3360.0	-450.1
122	VS78	-3296.0	-450.1
123	VS79	-3232.0	-450.1
124	VS80	-3168.0	-450.1
125	VS81	-3104.0	-450.1
126	VS82	-3040.0	-450.1
127	VS83	-2976.0	-450.1
128	VS84	-2912.0	-450.1
129	VS85	-2848.0	-450.1
130	VS86	-2784.0	-450.1
131	VS87	-2720.0	-450.1
132	VS88	-2656.0	-450.1
133	VS89	-2592.0	-450.1
134	VS90	-2528.0	-450.1
135	VS91	-2464.0	-450.1
136	VS92	-2400.0	-450.1
137	VS93	-2336.0	-450.1
138	VS94	-2272.0	-450.1
139	VS95	-2208.0	-450.1
140	VS96	-2144.0	-450.1
141	VS97	-2080.0	-450.1
142	VS98	-2016.0	-450.1
143	VS99	-1952.0	-450.1
144	VS100	-1888.0	-450.1
145	VS101	-1824.0	-450.1
146	VS102	-1760.0	-450.1
147	VS103	-1696.0	-450.1
148	VS104	-1632.0	-450.1
149	VS105	-1568.0	-450.1
150	VS106	-1504.0	-450.1
151	VS107	-1440.0	-450.1
152	VS108	-1376.0	-450.1
153	VS109	-1312.0	-450.1
154	VS110	-1248.0	-450.1
155	VS111	-1184.0	-450.1
156	VS112	-1120.0	-450.1
157	VS113	-1056.0	-450.1
158	VS114	-992.0	-450.1
159	VS115	-928.0	-450.1

Table 4–2: Output Bond Pad Coordinates

Pad #	Signal	X coor.	Y coor.
160	VS116	-864.0	-450.1
161	VS117	-800.0	-450.1
162	VS118	-736.0	-450.1
163	VS119	-672.0	-450.1
164	VS120	-608.0	-450.1
165	VS121	-544.0	-450.1
166	VS122	-480.0	-450.1
167	VS123	-416.0	-450.1
168	VS124	-352.0	-450.1
169	VS125	-288.0	-450.1
170	VS126	-224.0	-450.1
171	VS127	-160.0	-450.1
172	VS128	-96.0	-450.1
173	VS129	-32.0	-450.1
174	VS130	32.0	-450.1
175	VS131	96.0	-450.1
176	VS132	160.0	-450.1
177	VS133	224.0	-450.1
178	VS134	288.0	-450.1
179	VS135	352.0	-450.1
180	VS136	416.0	-450.1
181	VS137	480.0	-450.1
182	VS138	544.0	-450.1
183	VS139	608.0	-450.1
184	VS140	672.0	-450.1
185	VS141	736.0	-450.1
186	VS142	800.0	-450.1
187	VS143	864.0	-450.1
188	VS144	928.0	-450.1
189	VS145	992.0	-450.1
190	VS146	1056.0	-450.1
191	VS147	1120.0	-450.1
192	VS148	1184.0	-450.1
193	VS149	1248.0	-450.1
194	VS150	1312.0	-450.1
195	VS151	1376.0	-450.1
196	VS152	1440.0	-450.1
197	VS153	1504.0	-450.1
198	VS154	1568.0	-450.1
199	VS155	1632.0	-450.1

Table 4–2: Output Bond Pad Coordinates

Pad #	Signal	X coor.	Y coor.
200	VS156	1696.0	-450.1
201	VS157	1760.0	-450.1
202	VS158	1824.0	-450.1
203	VS159	1888.0	-450.1
204	VS160	1952.0	-450.1
205	VS161	2016.0	-450.1
206	VS162	2080.0	-450.1
207	VS163	2144.0	-450.1
208	VS164	2208.0	-450.1
209	VS165	2272.0	-450.1
210	VS166	2336.0	-450.1
211	VS167	2400.0	-450.1
212	VS168	2464.0	-450.1
213	VS169	2528.0	-450.1
214	VS170	2592.0	-450.1
215	VS171	2656.0	-450.1
216	VS172	2720.0	-450.1
217	VS173	2784.0	-450.1
218	VS174	2848.0	-450.1
219	VS175	2912.0	-450.1
220	VS176	2976.0	-450.1
221	VS177	3040.0	-450.1
222	VS178	3104.0	-450.1
223	VS179	3168.0	-450.1
224	VS180	3232.0	-450.1
225	VS181	3296.0	-450.1
226	VS182	3360.0	-450.1
227	VS183	3424.0	-450.1
228	VS184	3488.0	-450.1
229	VS185	3552.0	-450.1
230	VS186	3616.0	-450.1
231	VS187	3680.0	-450.1
232	VS188	3744.0	-450.1
233	VS189	3808.0	-450.1
234	VS190	3872.0	-450.1
235	VS191	3936.0	-450.1
236	VS192	4000.0	-450.1
237	dummy	4064.0	-450.1
238	dummy	4128.0	-450.1
239	dummy	4192.0	-450.1

Table 4–2: Output Bond Pad Coordinates

Pad #	Signal	X coor.	Y coor.
240	VS193	4256.0	-450.1
241	VS194	4320.0	-450.1
242	VS195	4384.0	-450.1
243	VS196	4448.0	-450.1
244	VS197	4512.0	-450.1
245	VS198	4576.0	-450.1
246	VS199	4640.0	-450.1
247	VS200	4704.0	-450.1
248	VS201	4768.0	-450.1
249	VS202	4832.0	-450.1
250	VS203	4896.0	-450.1
251	VS204	4960.0	-450.1
252	VS205	5024.0	-450.1
253	VS206	5088.0	-450.1
254	VS207	5152.0	-450.1
255	VS208	5216.0	-450.1
256	VS209	5280.0	-450.1
257	VS210	5344.0	-450.1
258	VS211	5408.0	-450.1
259	VS212	5472.0	-450.1
260	VS213	5536.0	-450.1
261	VS214	5600.0	-450.1
262	VS215	5664.0	-450.1
263	VS216	5728.0	-450.1
264	VS217	5792.0	-450.1
265	VS218	5856.0	-450.1
266	VS219	5920.0	-450.1
267	VS220	5984.0	-450.1
268	VS221	6048.0	-450.1
269	VS222	6112.0	-450.1
270	VS223	6176.0	-450.1
271	VS224	6240.0	-450.1
272	VS225	6304.0	-450.1
273	VS226	6368.0	-450.1
274	VS227	6432.0	-450.1
275	VS228	6496.0	-450.1
276	VS229	6560.0	-450.1
277	VS230	6624.0	-450.1
278	VS231	6688.0	-450.1
279	VS232	6752.0	-450.1

Table 4–2: Output Bond Pad Coordinates

Pad #	Signal	X coor.	Y coor.
280	VS233	6816.0	-450.1
281	VS234	6880.0	-450.1
282	VS235	6944.0	-450.1
283	VS236	7008.0	-450.1
284	VS237	7072.0	-450.1
285	VS238	7136.0	-450.1
286	VS239	7200.0	-450.1
287	VS240	7264.0	-450.1
288	VS241	7328.0	-450.1
289	VS242	7392.0	-450.1
290	VS243	7456.0	-450.1
291	VS244	7520.0	-450.1
292	VS245	7584.0	-450.1
293	VS246	7648.0	-450.1
294	VS247	7712.0	-450.1
295	VS248	7776.0	-450.1
296	VS249	7840.0	-450.1
297	VS250	7904.0	-450.1
298	VS251	7968.0	-450.1
299	VS252	8032.0	-450.1
300	VS253	8096.0	-450.1
301	VS254	8160.0	-450.1
302	VS255	8224.0	-450.1
303	VS256	8288.0	-450.1
304	VS257	8352.0	-450.1
305	VS258	8416.0	-450.1
306	D7	8503.6	-467.6
307	D6	8503.6	-340.2
308	D5	8503.6	-243.0
309	D4	8503.6	-145.8
310	D3	8503.6	-48.6
311	D2	8503.6	48.6
312	D1	8503.6	140.8
313	D8	-8503.6	140.8
314	D9	-8503.6	48.6
315	D10	-8503.6	-48.6
316	D11	-8503.6	-145.8
317	D12	-8503.6	-243.0
318	D13	-8503.6	-340.2
319	D14	-8503.6	-467.6

5. DETAILED PAD DESCRIPTIONS

The following abbreviations are used for pad types in the following sections: (I) input; (O) output; (I/O) Input/Output, (#) active 'low' signal.

Name	Number	Type	Description
LD258_1	9	I	**LOAD DIRECTION:** Controls the direction in which the data is loaded into the Input Register: When LD258_1 = '0', data is loaded from Channel V_{S1} to V_{S258}. When LD258_1 = '1', data is loaded from Channel V_{S258} to V_{S1}.
EIO1#, EIO258#	41,1	I/O	**ENABLE IN/OUT**: The EIO1# and EIO258# active 'low' signals initiate the loading of data into the Input Register of the WFP6540B. When one of the EIOx# pads is configured as an input, the other is configured as an output, with the direction determined by the LD258_1 input (see Table 5-1). The EIOx# output pads are designed to be connected to the EIOx# input pads of adjacent devices to allow a series of drivers to operate sequentially. When a 'low' is applied to the EIOx# pin configured as an input on the first device in the series, data is loaded from the three sets of 6-bit Data Inputs into the first three 6-bit Input-Register locations. On subsequent transitions of the DCLK, data continues to be loaded into the remaining 6-bit Input-Register locations. When the register is full (258 words), the EIOx# pin configured as an output goes 'low', enabling the next driver. The data load sequence is summarized in Table 5-1, Figure 5-1 and Figure 5-2.

Table 5-1: Input/Output Selection for EIO1# and EIO258#

LD258_1 Input	EIO1#, EIO258# Functionality		Data Loading Sequence
	EIO1#	EIO258#	
'0'	Input	Output	Channel 1 to 258
'1'	Output	Input	Channel 258 to 1

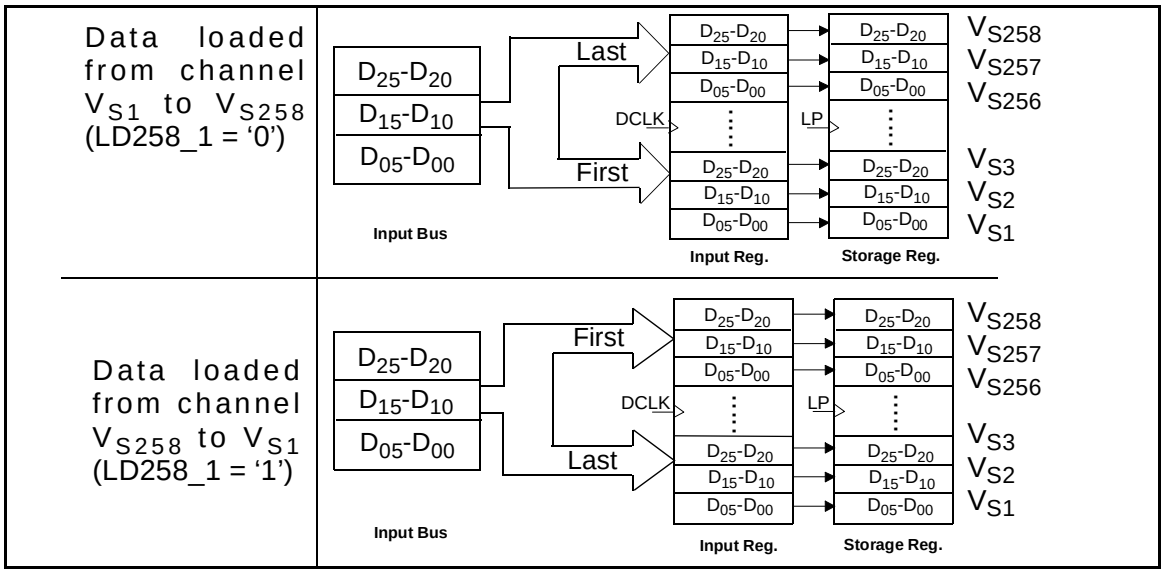


Figure 5–1. Display Data Sampling and Output Direction

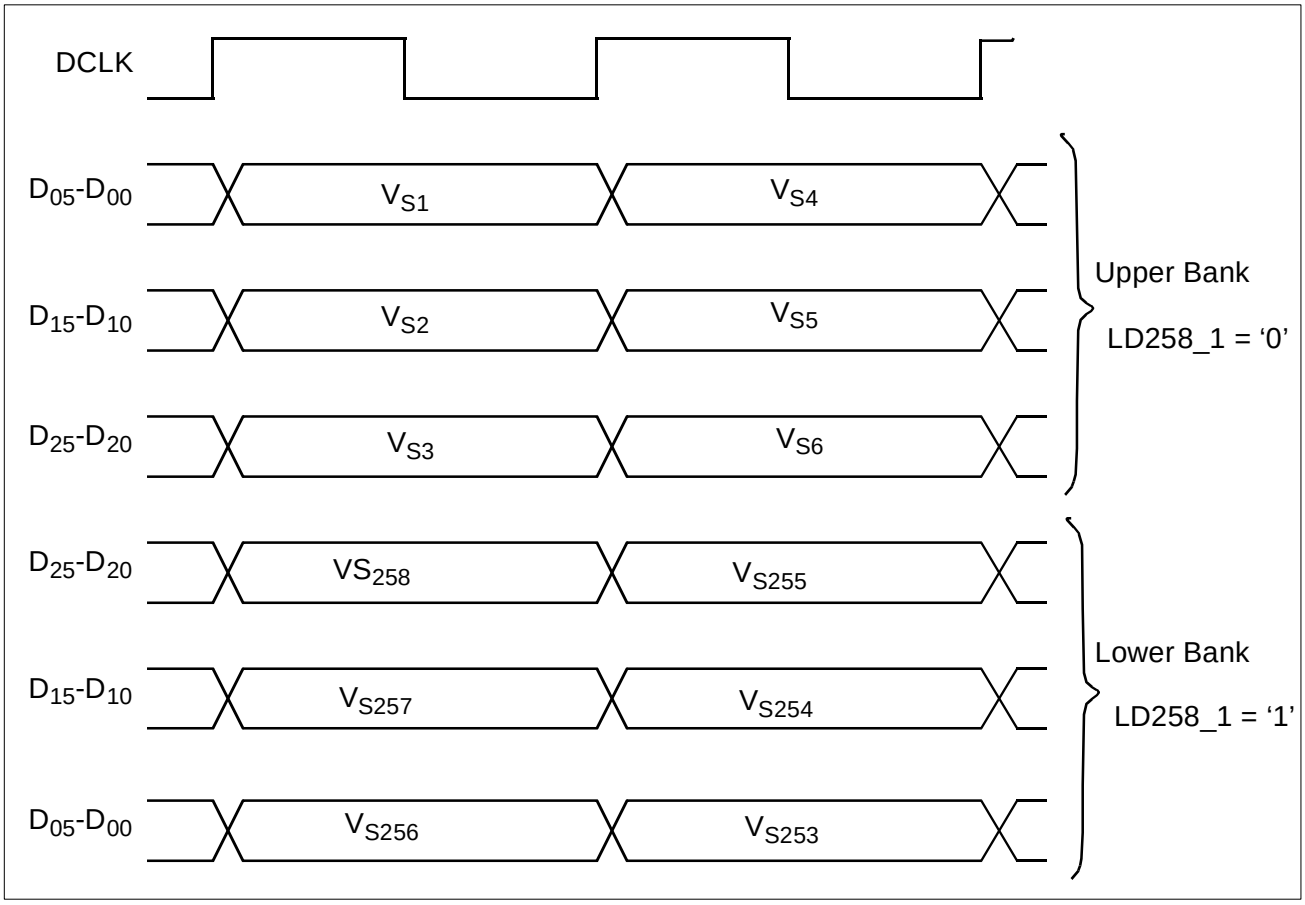


Figure 5–2. Display Data Channel Assignment and Output Sequence

Name	Number	Type	Description (*Cont.*)
V_{S1}-V_{S258}	42-300	O	**VOLTAGE OUTPUTS**: These outputs drive all 258 pixel inputs of the LCD simultaneously after the high-to-low transition of LP. Outputs are high impedance while LP is high.
D_{05}-D_{00} D_{15}-D_{10} D_{25}-D_{20}	35-40 8,13,14,27-29 2-7	I	**DATA**: The Data inputs consist of 6-bit words for each of three channels. At the falling edge of DCLK, three 6-bit words for three adjacent channels are loaded in parallel. Each data bit is represented as Dij where: i = 2-0 indicates the channel j = 5-0 indicates the significance of the bit in each word. D_{i5} indicates the MSB and D_{i0} indicates the LSB of the input word.
LP	34	I	**Latch Pulse**: When LP is asserted, the data is transferred from the Input Register into the Storage Register, and the selected analog voltages drive the LCD. The EIOx# output is reset to the 'high' level.
DCLK	15	I	**DATA CLOCK**: Data is loaded into the input registers on the high-to-low transition of DCLK for 2xCLK= low and on both rising and falling edges of DCLK for 2xCLK = high.
CLAMP#	30	I	**CLAMP**: The CLAMP# input controls the active pulldown devices which are present on the DCLK and D_{00}-D_{25} inputs. When the CLAMP# signal drives low, these clamp devices connect DCLK and D_{00}-D_{25} to the WFP6540B's GND through a low impedance. **The CLAMP# pin should be connected to V_{DDD} in applications where level shifting is not used (i.e. when V_{COM} modulation is employed).**
V_{DDD}	16	I	**DIGITAL SUPPLY VOLTAGE**: Either 3.3 V or 5.0 V should be provided on this pin to supply digital power to the device.
V_{DDA}	17	I	**ANALOG SUPPLY VOLTAGE**: Up to 5.0 V should be provided on this pin to supply analog power to the device.
V_8 V_7 V_6 V_5 V_4 V_3 V_2 V_1 V_0	11,31 18 23 20 21 22 19 24 10,32	I	**REFERENCE ANALOG VOLTAGE INPUTS:** These nine inputs are used to supply the adjustable-reference voltage inputs to the resistive-string DAC to provide the transmissivity-voltage response required for each type of LCD. Note: both V_8 pads must be connected to each other and to the same potential; also, both V_0 pads must be . connected to each other and to the same potential
A_{GND}	25	I	**ANALOG GROUND**
D_{GND}	26	I	**DIGITAL GROUND**

DATA_INV	33	I	**DATA INVERSION**: The data inversion input signal, when logic high, enables inversion of the input display data (D_{ij}). This pad should be tied “low” if data inversion is not used. See Figure 6-1,6-2 and 6-6 for timing information for this signal.
2xCLK	12	I	**2xCLK**: When logic high, the 2xCLK input enables sampling of input display data (D_{ij}) on both rising and falling edges of the DCLK input (see Figure 6-2). When logic low, input display data is sampled on the falling edge of DCLK only (see Figure 6-1).

Table 5-2: Input Data vs. Output Voltage

MSB	Display Data				LSB	Refer. Voltage	Output Voltage
D_5	D_4	D_3	D_2	D_1	D_0		
0	0	0	0	0	0	V_0, V_0	V_0
0	0	0	0	0	1	V_0, V_1	$V_0 + 1/7 \times (V_1 - V_0)$
0	0	0	0	1	0	V_0, V_1	$V_0 + 2/7 \times (V_1 - V_0)$
0	0	0	0	1	1	V_0, V_1	$V_0 + 3/7 \times (V_1 - V_0)$
0	0	0	1	0	0	V_0, V_1	$V_0 + 4/7 \times (V_1 - V_0)$
0	0	0	1	0	1	V_0, V_1	$V_0 + 5/7 \times (V_1 - V_0)$
0	0	0	1	1	0	V_0, V_1	$V_0 + 6/7 \times (V_1 - V_0)$
0	0	0	1	1	1	V_0, V_1	V_1
0	0	1	0	0	0	V_1, V_2	$V_1 + 1/8 \times (V_2 - V_1)$
0	0	1	0	0	1	V_1, V_2	$V_1 + 2/8 \times (V_2 - V_1)$
0	0	1	0	1	0	V_1, V_2	$V_1 + 3/8 \times (V_2 - V_1)$
0	0	1	0	1	1	V_1, V_2	$V_1 + 4/8 \times (V_2 - V_1)$
0	0	1	1	0	0	V_1, V_2	$V_1 + 5/8 \times (V_2 - V_1)$
0	0	1	1	0	1	V_1, V_2	$V_1 + 6/8 \times (V_2 - V_1)$
0	0	1	1	1	0	V_1, V_2	$V_1 + 7/8 \times (V_2 - V_1)$
0	0	1	1	1	1	V_1, V_2	V_2
0	1	0	0	0	0	V_2, V_3	$V_2 + 1/8 \times (V_3 - V_2)$
0	1	0	0	0	1	V_2, V_3	$V_2 + 2/8 \times (V_3 - V_2)$
0	1	0	0	1	0	V_2, V_3	$V_2 + 3/8 \times (V_3 - V_2)$
0	1	0	0	1	1	V_2, V_3	$V_2 + 4/8 \times (V_3 - V_2)$
0	1	0	1	0	0	V_2, V_3	$V_2 + 5/8 \times (V_3 - V_2)$
0	1	0	1	0	1	V_2, V_3	$V_2 + 6/8 \times (V_3 - V_2)$
0	1	0	1	1	0	V_2, V_3	$V_2 + 7/8 \times (V_3 - V_2)$
0	1	0	1	1	1	V_2, V_3	V_3
0	1	1	0	0	0	V_3, V_4	$V_3 + 1/8 \times (V_4 - V_3)$
0	1	1	0	0	1	V_3, V_4	$V_3 + 2/8 \times (V_4 - V_3)$
0	1	1	0	1	0	V_3, V_4	$V_3 + 3/8 \times (V_4 - V_3)$
0	1	1	0	1	1	V_3, V_4	$V_3 + 4/8 \times (V_4 - V_3)$
0	1	1	1	0	0	V_3, V_4	$V_3 + 5/8 \times (V_4 - V_3)$
0	1	1	1	0	1	V_3, V_4	$V_3 + 6/8 \times (V_4 - V_3)$
0	1	1	1	1	0	V_3, V_4	$V_3 + 7/8 \times (V_4 - V_3)$
0	1	1	1	1	1	V_3, V_4	V_4
1	0	0	0	0	0	V_4, V_5	$V_4 + 1/8 \times (V_5 - V_4)$
1	0	0	0	0	1	V_4, V_5	$V_4 + 2/8 \times (V_5 - V_4)$
1	0	0	0	1	0	V_4, V_5	$V_4 + 3/8 \times (V_5 - V_4)$
1	0	0	0	1	1	V_4, V_5	$V_4 + 4/8 \times (V_5 - V_4)$
1	0	0	1	0	0	V_4, V_5	$V_4 + 5/8 \times (V_5 - V_4)$
1	0	0	1	0	1	V_4, V_5	$V_4 + 6/8 \times (V_5 - V_4)$
1	0	0	1	1	0	V_4, V_5	$V_4 + 7/8 \times (V_5 - V_4)$
1	0	0	1	1	1	V_4, V_5	V_5
1	0	1	0	0	0	V_5, V_6	$V_5 + 1/8 \times (V_6 - V_5)$
1	0	1	0	0	1	V_5, V_6	$V_5 + 2/8 \times (V_6 - V_5)$
1	0	1	0	1	0	V_5, V_6	$V_5 + 3/8 \times (V_6 - V_5)$
1	0	1	0	1	1	V_5, V_6	$V_5 + 4/8 \times (V_6 - V_5)$
1	0	1	1	0	0	V_5, V_6	$V_5 + 5/8 \times (V_6 - V_5)$
1	0	1	1	0	1	V_5, V_6	$V_5 + 6/8 \times (V_6 - V_5)$
1	0	1	1	1	0	V_5, V_6	$V_5 + 7/8 \times (V_6 - V_5)$
1	0	1	1	1	1	V_5, V_6	V_6
1	1	0	0	0	0	V_6, V_7	$V_6 + 1/8 \times (V_7 - V_6)$
1	1	0	0	0	1	V_6, V_7	$V_6 \times 2/8 \times (V_7 - V_6)$
1	1	0	0	1	0	V_6, V_7	$V_6 + 3/8 \times (V_7 - V_6)$
1	1	0	0	1	1	V_6, V_7	$V_6 + 4/8 \times (V_7 - V_6)$
1	1	0	1	0	0	V_6, V_7	$V_6 + 5/8 \times (V_7 - V_6)$
1	1	0	1	0	1	V_6, V_7	$V_6 + 6/8 \times (V_7 - V_6)$
1	1	0	1	1	0	V_6, V_7	$V_6 + 7/8 \times (V_7 - V_6)$
1	1	0	1	1	1	V_6, V_7	V_7
1	1	1	0	0	0	V_7, V_8	$V_7 + 1/8 \times (V_8 - V_7)$
1	1	1	0	0	1	V_7, V_8	$V_7 + 2/8 \times (V_8 - V_7)$
1	1	1	0	1	0	V_7, V_8	$V_7 + 3/8 \times (V_8 - V_7)$
1	1	1	0	1	1	V_7, V_8	$V_7 + 4/8 \times (V_8 - V_7)$
1	1	1	1	0	0	V_7, V_8	$V_7 + 5/8 \times (V_8 - V_7)$
1	1	1	1	0	1	V_7, V_8	$V_7 + 6/8 \times (V_8 - V_7)$
1	1	1	1	1	0	V_7, V_8	$V_7 + 7/8 \times (V_8 - V_7)$
1	1	1	1	1	1	V_7, V_8	V_8

6. ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{DDD}	Digital Power Supply Voltage	-0.3	smaller of 6.0 or V_{DDA}	Volts	1,2,4
V_{DDA}	Analog Power Supply Voltage	-0.3	6.0	Volts	1,2,4
V_8 - V_0	Analog Reference Voltage Inputs	-0.3	V_{DDA} + 0.3	Volts	1,2
V_{S258}-V_{S1}	Output Voltage	-0.3	V_{DDA} + 0.3	Volts	1,2
V_{IN}	Voltage on any Digital Input	-0.3	V_{DDD} + 0.3	Volts	1,2,3
P_D	Operating Power Dissipation		300	mW	
T_A	Operating Temperature (Ambient Temperature under bias)	-10	85	°C	1
T_{STR}	Storage Temperature	-20	85	°C	1

NOTES: 1) Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

2) All voltages are with respect to ground (GND) unless otherwise noted.

3) For D_{25}-D_{20}, D_{15}-D_{10}, D_{05}-D_{00}, DCLK, LP, CLAMP#, EIO1#, EIO258# and LD258_1 input pads.

4) **V_{DDA} must be greater than or equal to V_{DDD} for proper circuit operation**. For this reason, V_{DDA} should be powered on first (or at the same time as V_{DDD}). Also, V_{DDD} should be powered off first, or at same time as V_{DDA}.

6.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{DDD}	Digital Supply Voltage	3.0 4.5	3.3 5.0	3.6 5.5	Volts Volts	1 1
V_{DDA}	Analog Supply Voltage	4.5	5.0	5.5	Volts	1
T_A	Ambient Temperature	0	25	70	°C	
V_8 - V_0	Analog Reference Voltage	0		V_{DDA}	Volts	1, 2
I_{REF}	Analog Reference Current			20	mA	

NOTES: 1) All voltages are with respect to ground (GND) unless otherwise noted.
2) Case I: $V_{DDA} \geq V_8 \geq V_7 \geq V_6 \geq V_5 \geq V_4 \geq V_3 \geq V_2 \geq V_1 \geq V_0$
Case II: $V_{DDA} \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_6 \geq V_7 \geq V_8$

6.3 DC Characteristics (Preliminary data – subject to change)

V_{DDA} = 5 V ± 0.5 V, T_A = 25° C, unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units	Test Conditions	Note
V_S	Analog Output Voltage				VDDA-0.03	Volts		1
V_{ST}	Analog Output Transition Band				$\|V_8-V_0\|$	Volts		
V_{ERR}	Analog Output Error Voltage		-0.15		+0.15	LSB		2
V_{IH}	Logic Input high Voltage		$0.8V_{DDD}$			Volts		3
V_{IL}	Logic Input low Voltage				$0.2V_{DDD}$	Volts		3
V_{OH}	Logic Output high Voltage		V_{DDD} - 0.4			Volts	I_{OH} = - 0.4 mA	4
V_{OL}	Logic Output low Voltage				0.4	Volts	I_{OL} = 0.4 mA	4
I_{QR}	Reference Quiescent Current		4.2	6.0	7.8	mA		5
I_{DDA}	Analog Supply Current				400	µA	V_{DDA} = 5.0 V	6
I_{DDD}	Digital-Supply Current (active)			3.8 6.4	7 10	mA mA	V_{DDD} = 3.3 V V_{DDD} = 5.0 V	6
I_{DDD}	Digital-Supply Current (Stand-by)			80 200	400 600	µA µA	V_{DDD} = 3.3 V V_{DDD} = 5.0 V	7
I_{IN}	Input Leakage Current		-5		+5	µA	$0 < V_{IN} < V_{DDD}$	
C_{IN}	Input Capacitance				5	pF		
R_{String}	String Resistance	V0-V1	112	160	208	Ω		
		V1-V2	81	116	151			
		V2-V3	70	100	130			
		V3-V4	70	100	130			
		V4-V5	70	100	130			
		V5-V6	70	100	130			
		V6-V7	81	116	151			
		V7-V8	126	180	208			
R_{OUT}	Output Resistance							
	V0-V1 (at code 3)				13.78	kΩ		8
	V1-V2 (at code 11)				10.6			
	V2-V3 (at code 19)				9.35			
	V3-V4 (at code 27)				9.35			
	V4-V5 (at code 35)				9.35			
	V5-V6 (at code 43)				9.35			
	V6-V7 (at code 51)				10.6			
	V7-V8 (at code 59)				15.59			

NOTES: 1) See Table 5-2 for digital code-Voltage relationship.

2) For all codes. Error is difference between measured voltage & Table 5-2 value.

NOTES: **cont'd**

3) DCLK, LP, CLAMP#, D_{25}-D_{20}, D_{15}-D_{10}, D_{05}-D_{00}, EIO1#, EIO258#, and LD258_1 inputs
4) EIO1# and EIO258# outputs
5) Quiescent current between V_0 and V_8 with $|V_0-V_8|$ = 5.0 V and all other references floating
6) f_{DCLK}=12.5 MHz, f_{LP} = 30 kHz, device is loading ,100% of data lines toggle each DCLK cycle
7) f_{DCLK}=12.5 MHz, f_{LP} = 30 kHz, device is not loading,100% of data lines toggle each DCLK cycle.
8) The output resistance of the FP6540B varies as a function of channel position and code. R_{OUT} represents the worst case output resistance on any channel and code combination. See Figure 6-5 for equivalent circuit.

6.4 AC Characteristics (V_{DDD} = 3.3 V ± 0.3 V) – (Preliminary data – subject to change)

See Figures 6-1 to 6-3 for waveforms.
Conditions: V_{DDA} = 5.0 V ± 0.5 V, T_A = 25° C

Symbol	Parameter	Min	Typical	Max	Units	Note
f_{CLK}	Guaranteed DCLK frequency	65			MHz	
t_{CLK}	DCLK period	15.4			ns	
$t2x_{CLK}$	DCLK period (2xCLK mode)	30.8			ns	
t_1	DCLK high pulse width	6			ns	
t_2	DCLK low pulse width	6			ns	
t_3	DCLK, LP rise time			10	ns	
t_4	DCLK, LP fall time			10	ns	
t_5	Data, DATA_INV setup time to DCLK Falling Edge	4			ns	
t_6	Data, DATA_INV hold time from DCLK Falling Edge	8			ns	
t_7	LP high pulse width	50			ns	2
t_8	Enable-In setup time to DCLK	4			ns	
t_9	Enable-Out low delay from DCLK			10	ns	1
t_{10}	DCLK low LP high	50			ns	
t_{11}	LP low to DCLK high	50			ns	
t_{12}	Data, DATA_INV setup time to DCLK Rising Edge	4			ns	
t_{13}	Data, DATA_INV hold time from DCLK Rising Edge	8			ns	

NOTES: 1) C_{LOAD} = 15 pF (See Figure 6-4)

2) LP width should not be wider than necessary since outputs don't drive to the next value until LP is low.

6.5 AC Characteristics (V_{DDD} = 5.0 V ± 0.5 V) – (Preliminary data – subject to change)

See Figures 6-1 to 6-3 for waveforms.
Conditions: V_{DDA} = 5.0 V ± 0.5 V, T_A = 25° C

Symbol	Parameter	Min	Typical	Max	Units	Note
f_{CLK}	Guaranteed DCLK frequency	65			MHz	
t_{CLK}	DCLK period	15.4			ns	
$t2x_{CLK}$	DCLK period (2xLCK mode)	30.8			ns	
t_1	DCLK high pulse width	6			ns	
t_2	DCLK low pulse width	6			ns	
t_3	DCLK, LP rise time			10	ns	
t_4	DCLK, LP fall time			10	ns	
t_5	Data, DATA_INV setup time to DCLK Falling Edge	4			ns	
t_6	Data, DATA_INV hold time from DCLK Falling Edge	8			ns	
t_7	LP high pulse width	40			ns	2
t_8	Enable-In setup time to DCLK	4			ns	
t_9	Enable-Out low delay from DCLK			10	ns	1
t_{10}	DCLK low to LP high	40			ns	
t_{11}	LP low to DCLK high	40			ns	
t_{12}	Data, DATA_INV setup time to DCLK Rising Edge	4			ns	
t_{13}	Data, DATA_INV hold time from DCLK Rising Edge	8			ns	

NOTES: 1) C_{LOAD} = 15 pF (See Figure 6-4).

2) LP width should not be wider than necessary since outputs don't drive to the next value until LP is low.

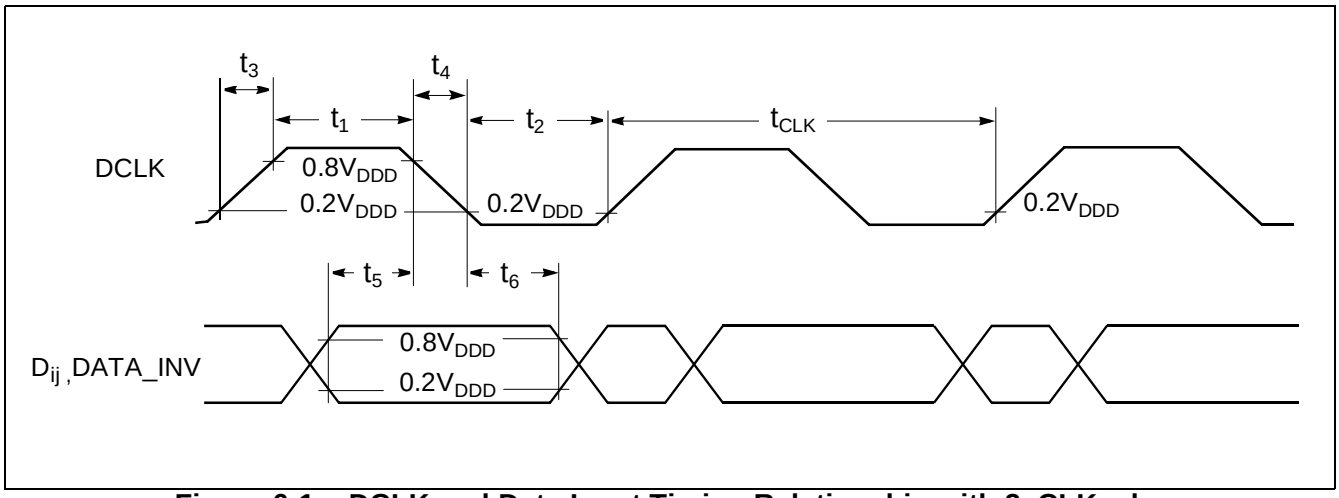


Figure 6-1: DCLK and Data Input Timing Relationship with 2xCLK = low

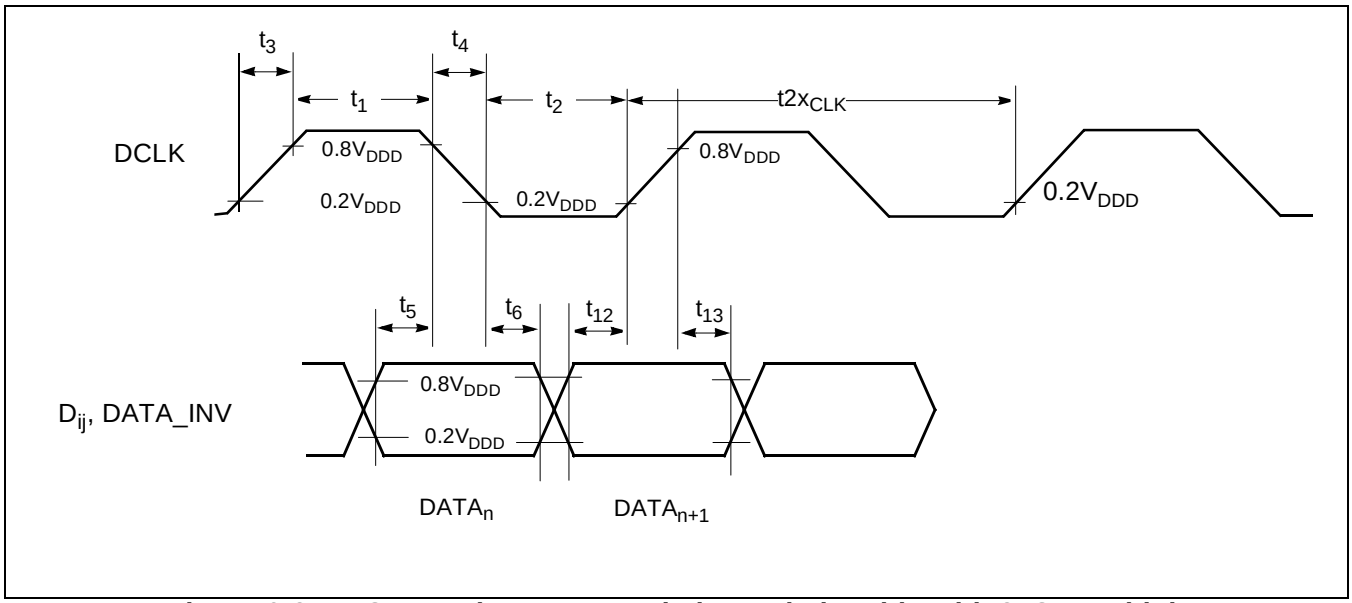


Figure 6-2: DCLK and Data Input Timing Relationship with 2xCLK = high

Note: When 2xCLK = high, the first rising edge of DCLK after LP falling edge clocks in the first display data word

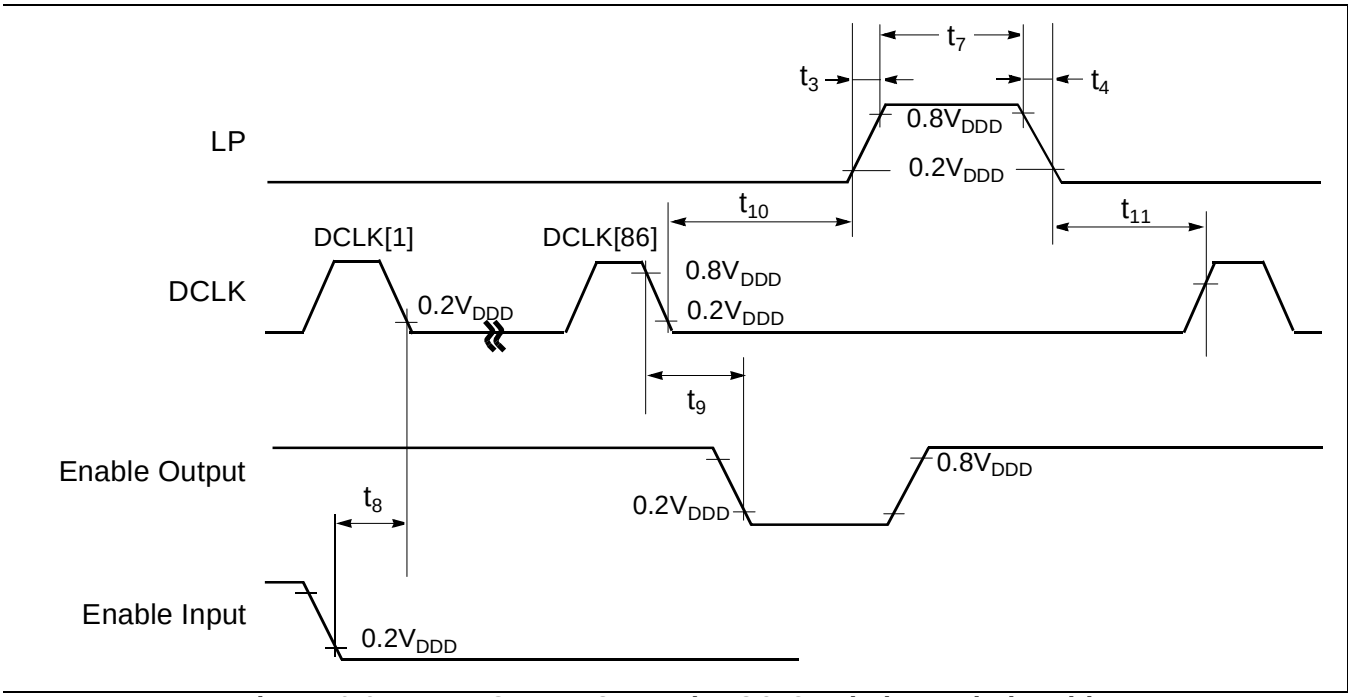


Figure 6-3: LP, DCLK, EIO1#and EIO258# Timing Relationship

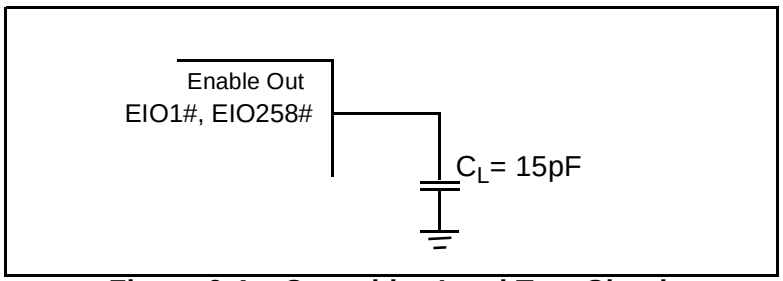


Figure 6-4: Capacitive Load Test Circuit

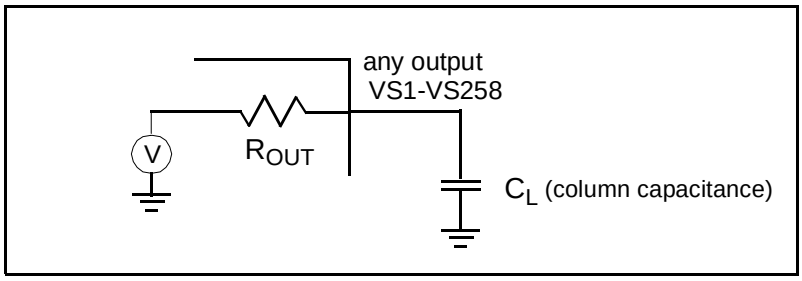


Figure 6-5: R_{OUT} Definition

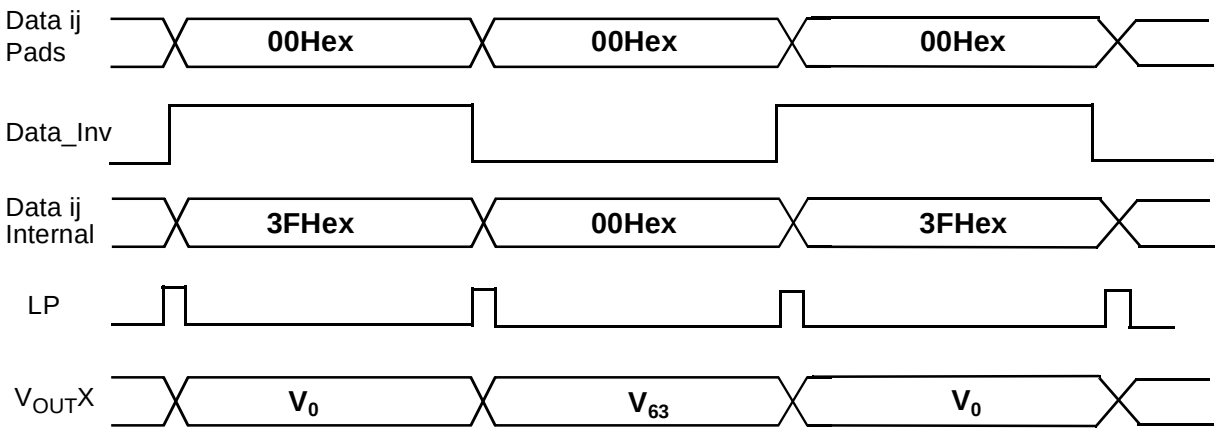


Figure 6-6: Data Inversion Example