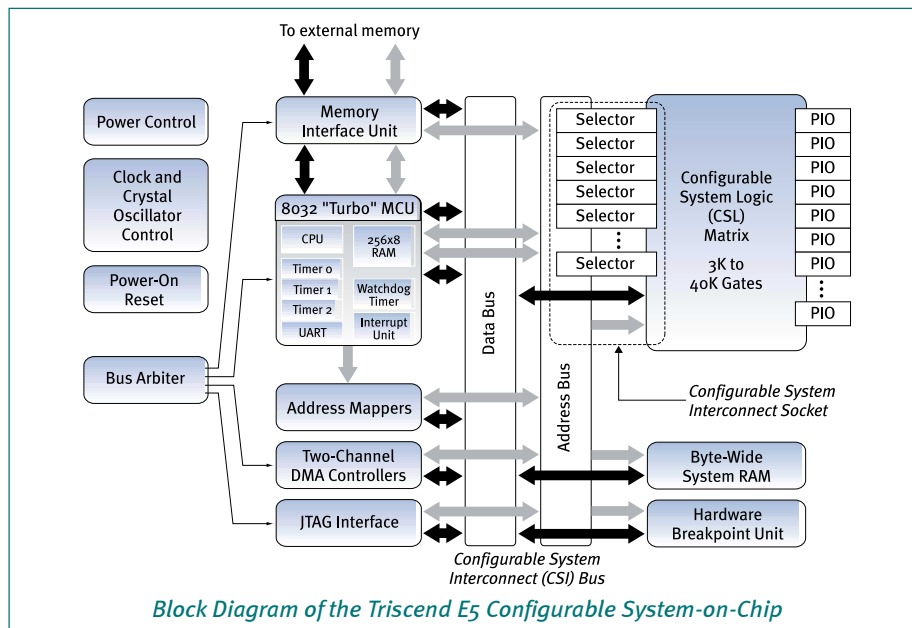


Triscend E5™

8-bit Configurable System-on-Chip

The E5 family of Configurable System-on-Chip devices from Triscend combines a high-performance industry standard 8032 microcontroller, programmable logic, RAM, a high-speed bus, and many other system functions onto a single chip. With Triscend's FastChip CSoC Development Software, designers can quickly create an 8032 microcontroller derivative optimized for a particular application.



E5 Device Highlights

- High-performance, industry-standard accelerated 8051 MCU core
 - 40 MHz operation (up to 10 MIPS)
 - 4 clock cycles/instruction cycle
 - Binary and source code compatible with standard 8051/8032 variants
 - Three 16-bit timer/counters
 - Programmable, full duplex UART
 - Up to 316 programmable I/O (PIO) ports
 - Protected watch-dog timer
 - Programmable interrupts
 - 3 external
 - 10 internal, including watch-dog timer, software and hardware breakpoints, and DMA transfer
- Up to 64 Kbytes of on-chip, dedicated system SRAM
- Advanced debug capability
 - In-system breakpoint unit

- Stand-alone operation from a single external memory
- Power-down and power-management modes
- Embedded support functions
 - 2-channel DMA controller
 - IEEE 1149.1 enhanced JTAG interface
- Power-on reset
- Memory Interface Unit (MIU) for flexible, glue-less interface to external memory
- Wait state generation
- Embedded SRAM-based Configurable System Logic (CSL) matrix
 - Over 3,800 flip-flops and 300 programmable inputs and outputs (PIOs)
 - Abundant, flexible interconnect structure with easy access to and from system bus
 - Dedicated circuitry for fast adders, counters, and multipliers
 - CSL cells can be configured as memory, including true dual-port operation
 - 6 independent low-skew clock or global signal distribution buffers (in addition to system clock)
- High performance dedicated system bus
 - Configurable System Interconnect (CSI) bus integrates CSOC operation
 - Up to 40 Mbytes per second DMA transfer rate
 - Up to 32-bit address bus and 8-bit data bus
 - CSI Socket is openly defined CSI bus interface to CSL matrix
 - Soft peripheral logical addresses stay independent of placement in CSL matrix
 - All soft peripherals compatible with past and future CSoC families
- Pinout compatibility allows easy migration to larger or smaller devices in the same package

Product Family Name	Data Path Width	Embossed Processor Core	Device Name	Configurable System Logic Cells	System RAM	Programmable I/O (max)	Packages
E5	8	40 MHz	TE502So8	256	8K x 8	92	128LQFP
			TE505S16	512	16K x 8	124	128LQFP, 208QFP
		10 MIPS "TURBO"	TE512S32	1152	32K x 8	188	128LQFP, 208QFP
			TE520S40	2048	40K x 8	252	208QFP, 484BGA
			TE532S64	3200	64K x 8	316	208QFP, 484BGA
8032							