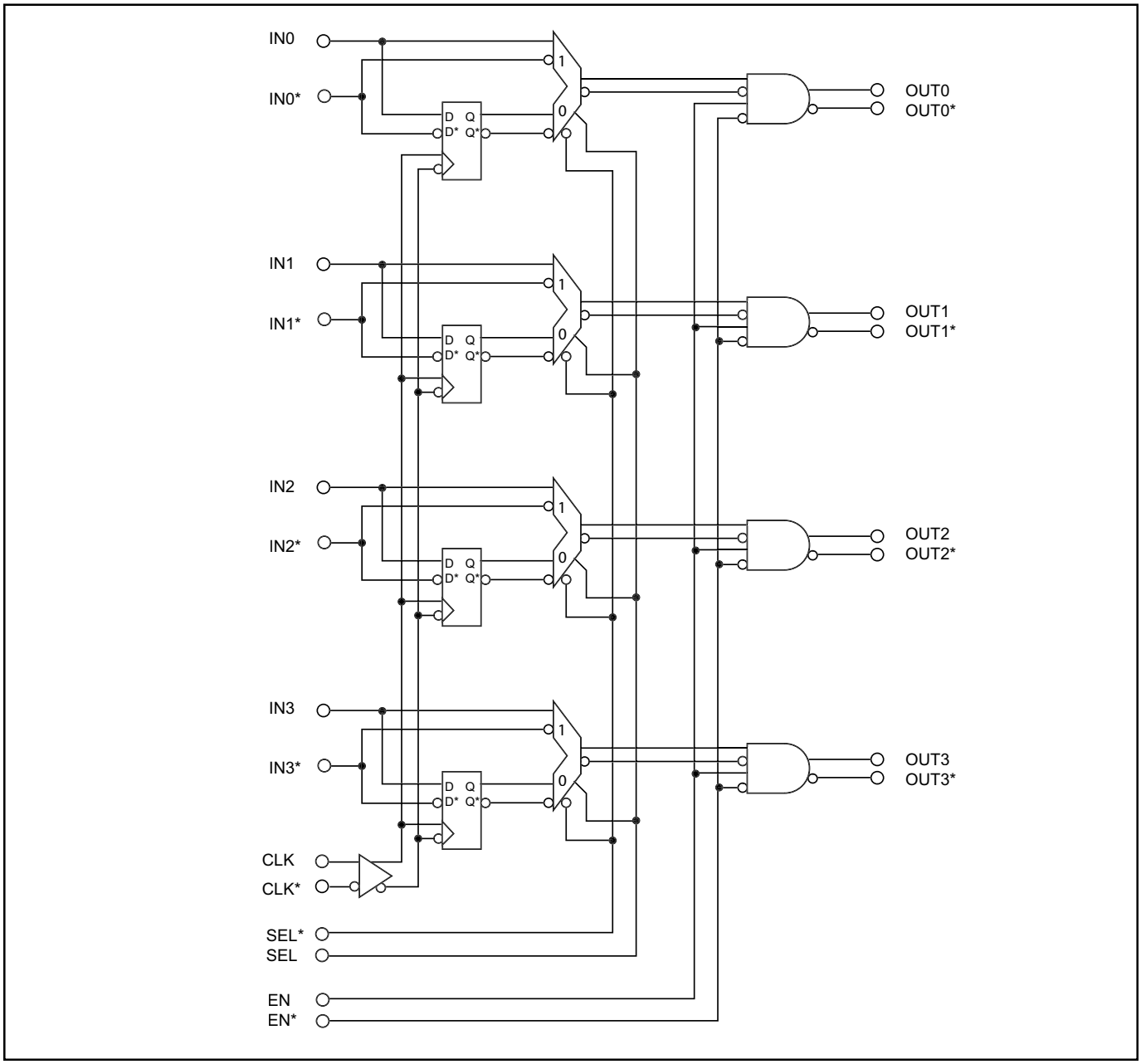
SK44XX Family Functional Block Diagram



SK44XX Family Product Selection Guide

Quad Buffer/Receiver	*3 GHz*	*Synch / Asynch Operation*

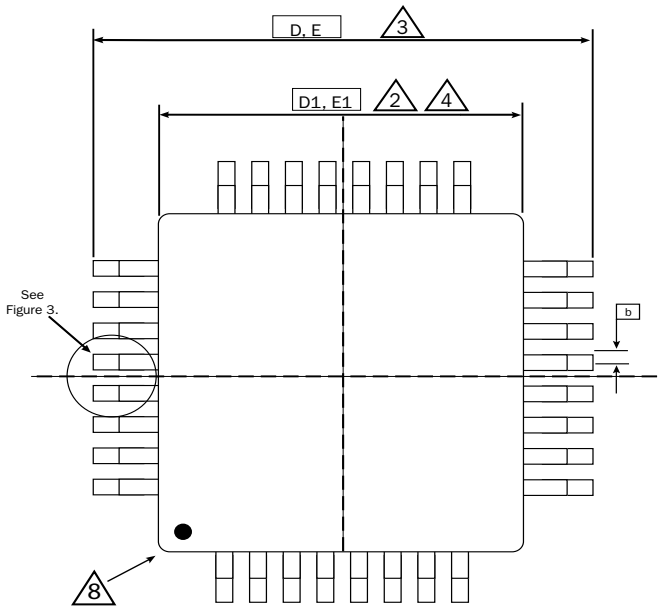
Logic Family

	Power Supply		Input Termination		Output Configuration		Output Swing	Availability
Product	3.3V	5.2V	Open	100Ω	Open Emitter	50Ω Output	Output Swing	
SK4400	●	●	●		●		ECL / PECL	Now
SK4401		●	●		●		Double Swing / TTL	Now
SK4404	●	●	●			●	ECL / PECL	Now
SK4410	●	●		●	●		ECL / PECL	Now
SK4411		●		●	●		Double Swing / TTL	Now
SK4414	●	●		●		●	ECL / PECL	Now

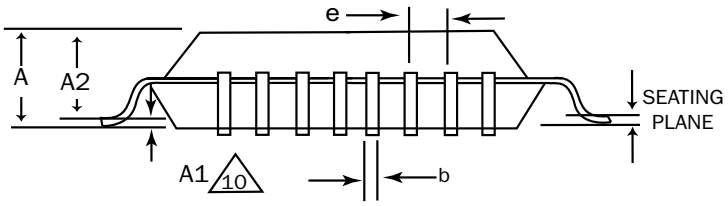
Logic / Translation Family

	Translation	Input Termination		Output Configuration		Availability
Product		Open	100Ω	Open Emitter	50Ω Output	
SK4425	Anything to PECL	●		●		Now
SK4426	Anything to ECL	●		●		Now
SK4429	Anything to PECL	●			●	Now
SK4430	Anything to ECL	●			●	Now
SK4435	Anything to PECL		●	●		Now
SK4436	Anything to ECL		●	●		Now
SK4439	Anything to PECL		●		●	Now
SK4440	Anything to ECL		●		●	Now

SK44XX Family Package Information
5mm x 5mm TQFP



Top View



Side View

SK44XX Family Package Information (continued)
5mm x 5mm TQFP

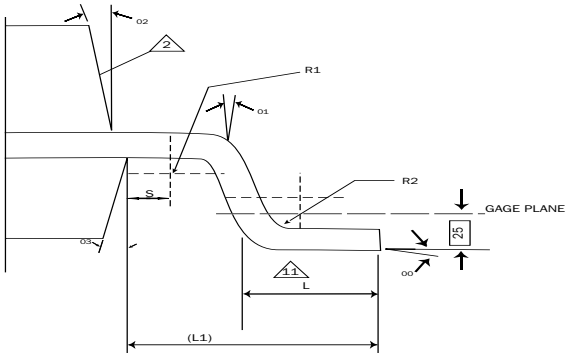


Figure 1.

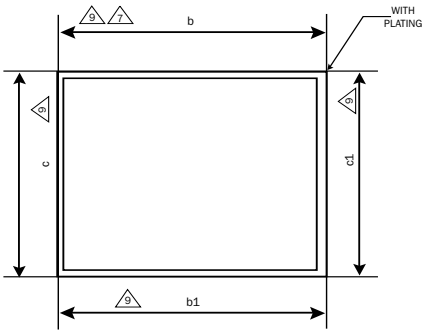


Figure 2.

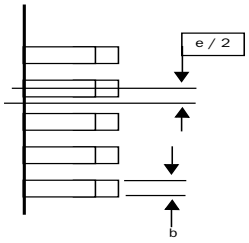


Figure 3.

1. All dimensions and tolerancing conforms to ANSI Y14.5M-1982.
2. The top package body size may be smaller than the bottom package body size by as much as 0.15 mm.
3. To be determined at seating plane.
4. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
5. Details of Pin 1 identifier optional, but must be located within the zone indicated.
6. All dimensions are in millimeters.
7. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
8. Exact shape of each corner is optional.
9. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
10. A1 is defined as the distance from the seating plane to the lowest point of the package body.

JEDEC Variation All Dimensions in Millimeters					
Symbol	**MIN**	**NOM**	**MAX**	**Note**	**Comments**
A	1.00	1.10	1.20		Package Stand Off Height
A1	0.05	0.10	0.15		Air Gap
A2	0.95	1.00	1.05		Package Body Thickness
D		7.00 BSC		3	
D1		5.00 BSC		4, 2	Package Body Length
E		7.00 BSC		3	
E1		5.00 BSC		4, 2	Package Body Width
N		32			Lead Count
e		0.50 BSC			Lead Pitch
b	0.17	0.22	0.27	7	Lead Thickness
b1	0.17	0.20	0.23		
R1	0.08	–	–		
R2	0.08	–	0.20		
00	0°	3.5°	7°		
01	0°	–	–		
02	11°	12°	13°		
03	11°	12°	13°		
S	0.20	–	–		
c	0.09	–	0.20		
c1	0.09	–	0.16		
L	0.45	0.60	0.75		
L1		1.00 REF			
aaa		0.20			
bbb		0.20			
ccc		0.08			
ddd		0.08			

Absolute Maximum Ratings*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	-6.0 to 0	V
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	V
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	-6.0 to 0	V
V_I	Input Voltage (V_E = 0V, V_I not more positive than V_{CC})	6.0 to 0	V
I_{OUT}	Output Current Continuous Surge	 50 100	 mA mA
T_A	Operating Temperature Range	0 to +70	^{0}C
T_{stg}	Storage Temperature	-65 to +150	^{0}C
T_{sol}	Solder Temperature (<2 to 3 seconds: 245^{0}C desired)	265	^{0}C

* Maximum Ratings are those values beyond which damage to the device may occur.

Note:

1. Pay attention to handling of this device because it is ESD sensitive.

Description

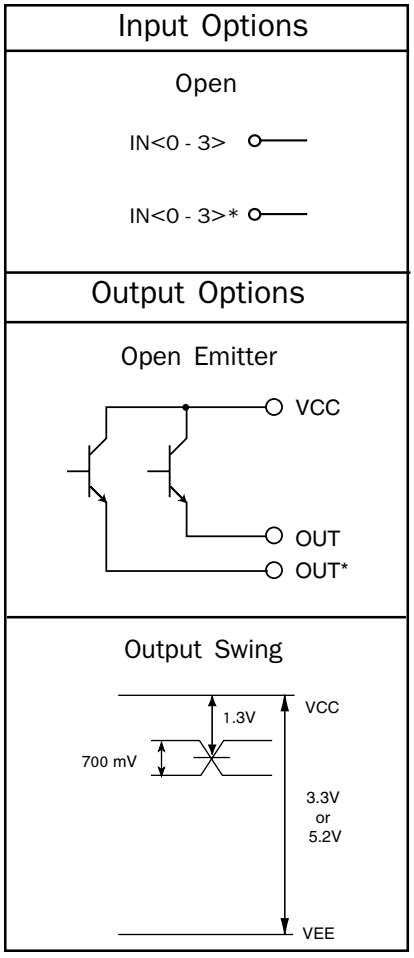
The SK4400 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asychronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input.

The SK4400 uses standard open emitter ECL outputs optimized for:

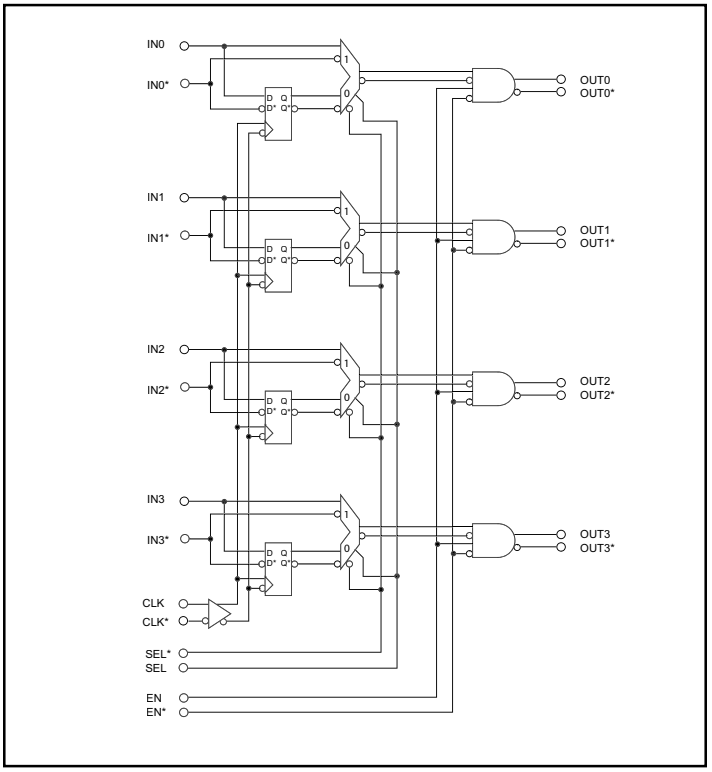
- Standard, general purpose ECL applications
- Multiple destinations (daisy chain).

Features

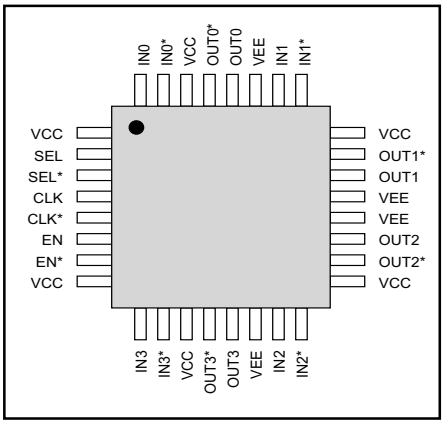
- Quad Buffer/Receiver
- 3 GHz Fmax
- 3.3V / 5.2V Compatible



Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage (Note 1)	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	IIH IIL	+1 -1		+25 +1	µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range	| OUT - OUT* | (OUT + OUT*) / 2	600 VCC - 1.5	700 VCC - 1.3	 VCC - 1.1	mV V
Power Supply					
Power Supply Current Power Supply Voltage	IEE VCC - VEE	 3.0	90	115 5.5	mA V

DC Test Conditions: Outputs terminated with 50Ω to VCC – 2V.
Note 1: Production tested to a maximum V_{diff} = 2.0V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1) CLK to OUT[0:3] (SEL = 0)	 Tpd Tpd	 250 430	 350 530	 450 630	 ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient (Note 1)	ΔTpd /ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC – 2V
Note:
1. Guaranteed by characterization. Not production tested.

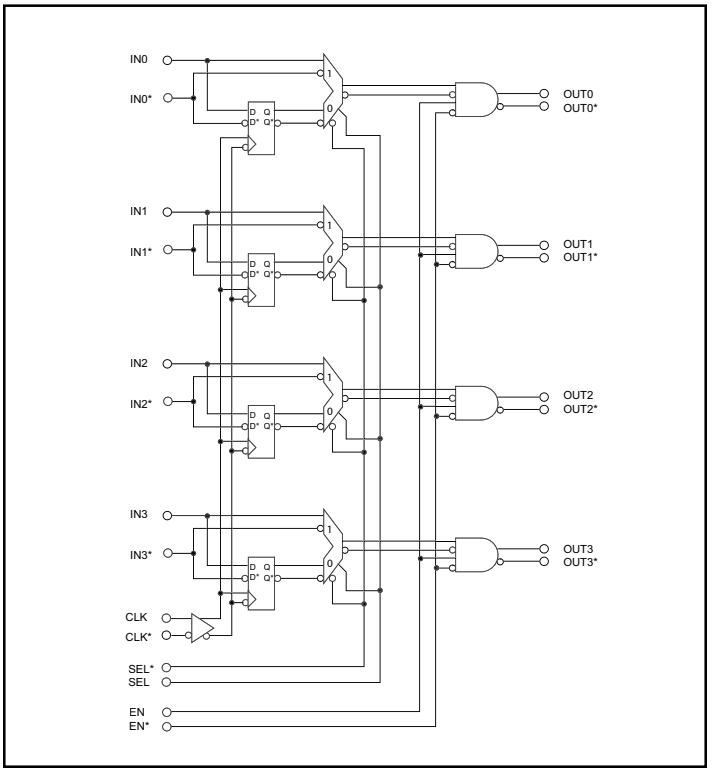
Description

The SK4401 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asychronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input.

The SK4401 uses open emitter outputs with a double amplitude swing suitable for the following applications:

- TTL compatible destinations
- Double termination situations that require a full swing at the destination
- Long cables

Functional Block Diagram

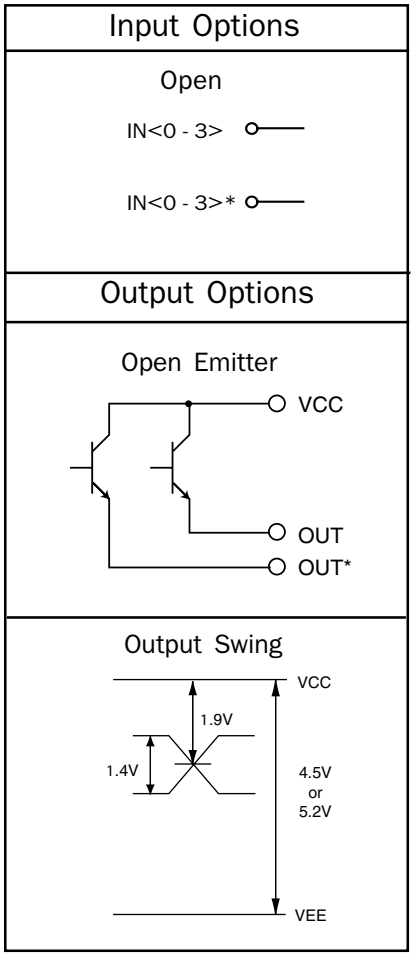


Package Information

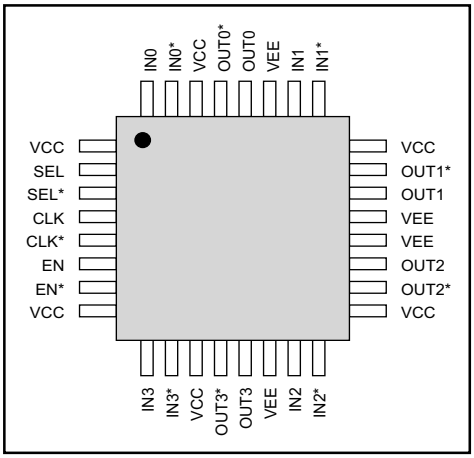
32 pin, 5 mm x 5 mm
TQFP Package

Features

- Quad Buffer/Receiver
- 2 GHz Fmax
- 4.5V / 5.2V Compatible



Pin Description



DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC -.2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL -SEL*) Differential Input Voltage	| Input -Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 +1 -1		 +25 +1	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range	| OUT -OUT* | (OUT + OUT*) / 2	1.2 VCC -2.1	1.4 VCC - 1.9	 VCC - 1.7	V V
Power Supply					
Power Supply Current Power Supply Voltage	IEE VCC -VEE	 4.2	90	115 5.5	mA V

DC Test Conditions: Outputs terminated with 50Ω to VCC – 3.3V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1) CLK to OUT[0:3] (SEL = 0)	 Tpd Tpd	 250 430	 350 530	 450 630	 ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	2.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% /80%)	Tr / Tf		200	250	ps
Temperature Coefficient (Note 1)	ΔTpd /ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC – 2V

Note:

1. Guaranteed by characterization. Not production tested.

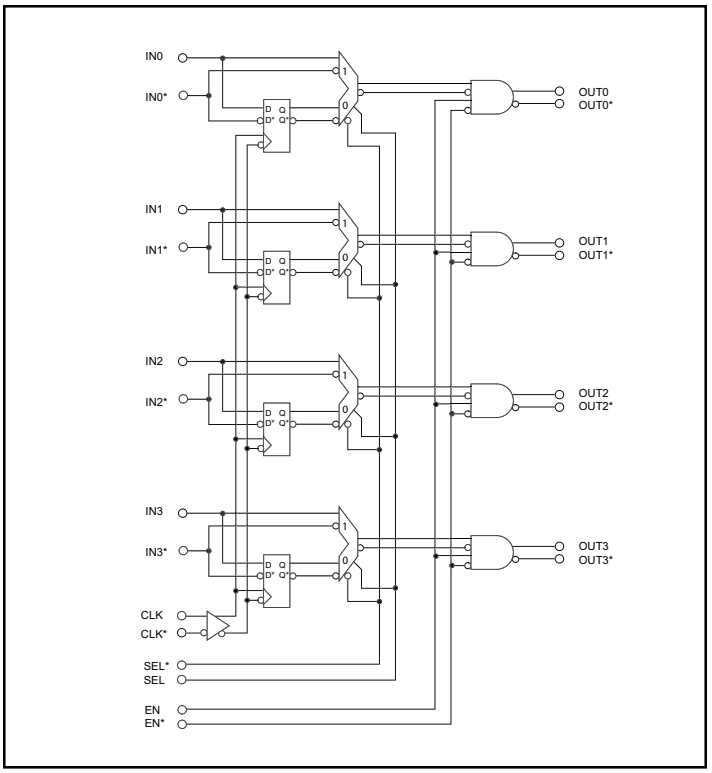
Description

The SK4404 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asychronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input.

The SK4404 uses 50Ω outputs with sink/source capability, and is optimized for applications that require:

- Point to point, double terminated, timing critical lines
- Point to point, series terminated, timing critical lines

Functional Block Diagram



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

Features

- Quad Buffer/Driver
- 3 GHz Fmax
- 3.3V / 5.2V Compatible

Input Options

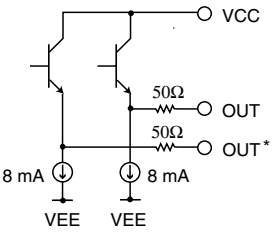
Open

IN<0 - 3>

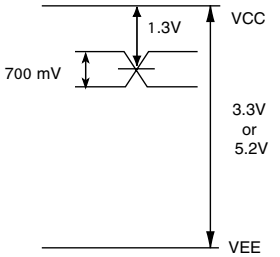
IN<0 - 3>*

Output Options

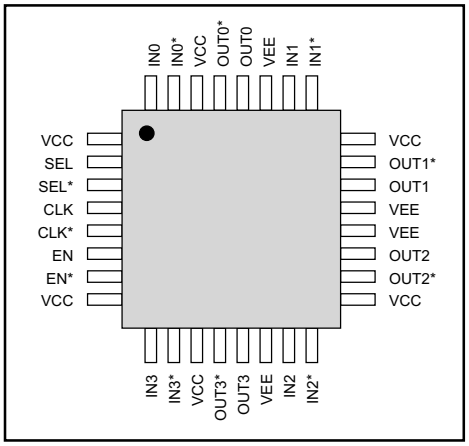
50Ω Source / Sink



Output Swing



Pin Description



DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 +1 -1		 +25 +1	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VCC - 1.5 6.5 40	700 VCC -1.3 8 45	 VCC - 1.1 10.0 50	mV V mA W
Power Supply					
Power Supply Current Power Supply Voltage	IEE VCC - VEE	 3.0	155	197 5.5	mA V

DC Test Conditions: Outputs unterminated.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1) CLK to OUT[0:3] (SEL = 0)	 Tpd Tpd	 250 430	 350 530	 450 630	 ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient (Note 1)	ΔTpd /ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC – 2V

Note:

1. Guaranteed by characterization. Not production tested.

Description

The SK4410 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asychronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input.

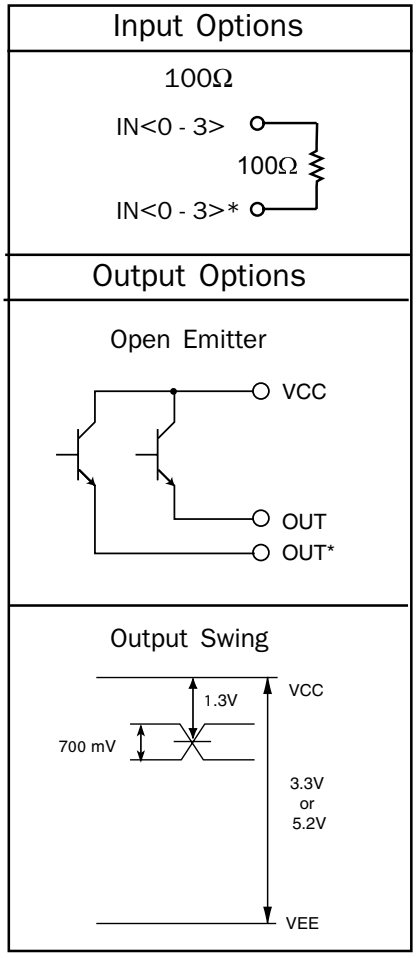
The SK4410 has 100Ω input termination resistors across each of the four inputs to help reduce system component count and increase integration.

The SK4410 uses standard open emitter ECL outputs optimized for:

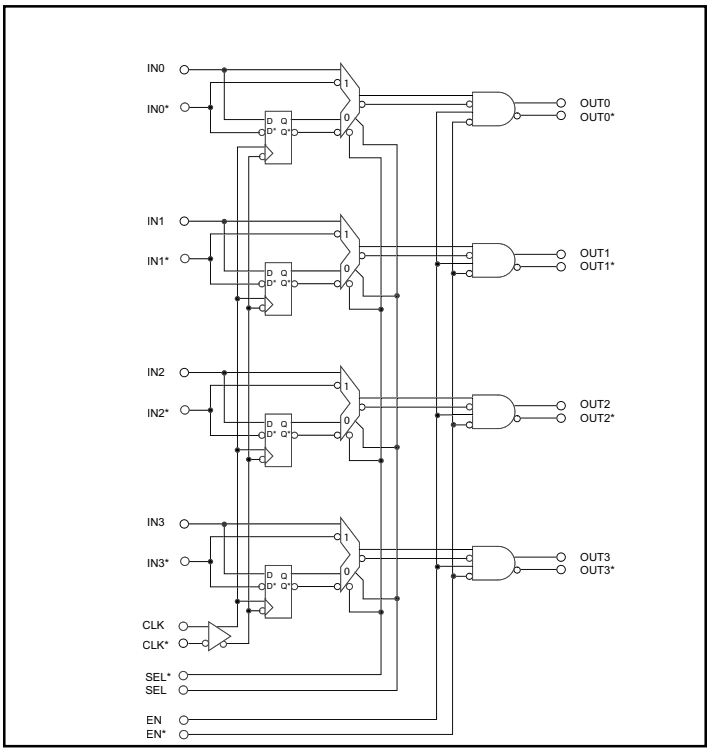
- Standard, general purpose ECL applications
- Multiple destinations (daisy chain).

Features

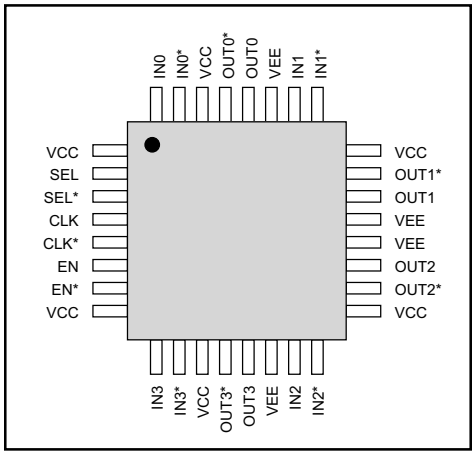
- Quad Buffer/Receiver
- 3 GHz Fmax
- 3.3V / 5.2V Compatible



Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current IN / IN* Differential Input Resistance	 IIH IIL RIN	 +1 -1 100 -- TBD	 100	 +25 +1 100 + TBD	 µA µA W
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range	| OUT - OUT* | (OUT + OUT*) / 2	600 VCC - 1.5	700 VCC -1.3	 VCC - 1.1	mV V
Power Supply					
Power Supply Current Power Supply Voltage	IEE VCC - VEE	 3.0	90	115 5.5	mA V

DC Test Conditions: Outputs terminated with 50Ω to VCC – 2V.

AC Characteristics

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
High Performance Option					
Propagation Delay IN[0:3] to OUT[0;3] (sel - 1) CLK to OUT[0:3] (SEL - 0)	 Tpd Tpd	 250 430	 350 530	 450 630	 ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
IN to CLK (Note 1) Setup Time Hold Time	 Tsu Th	 100 100			 ps ps
Output rise and Fall Times (20%/80%)	Tr/Tf		125	150	ps
Temperature Coefficient (Note 1)	ΔTpd/ΔT		<1		ps/°C

AC Test Conditions: Outputs terminated with 50Ω to VCC – 2V

Note:

1. Guaranteed by characterization. Not production tested.

Description

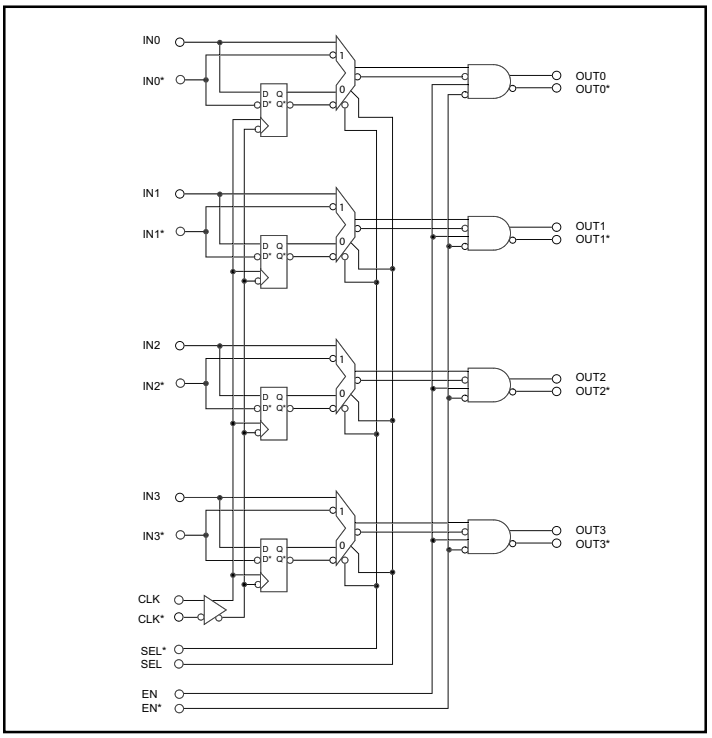
The SK4411 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asychronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input.

The SK4411 has 100Ω input termination resistors across each of the four inputs to help reduce system component count and increase integration.

The SK4411 uses open emitter outputs with a double amplitude swing suitable for the following applications:

- TTL compatible destinations
- Double termination situations that require a full swing at the destination
- Long cables

Functional Block Diagram

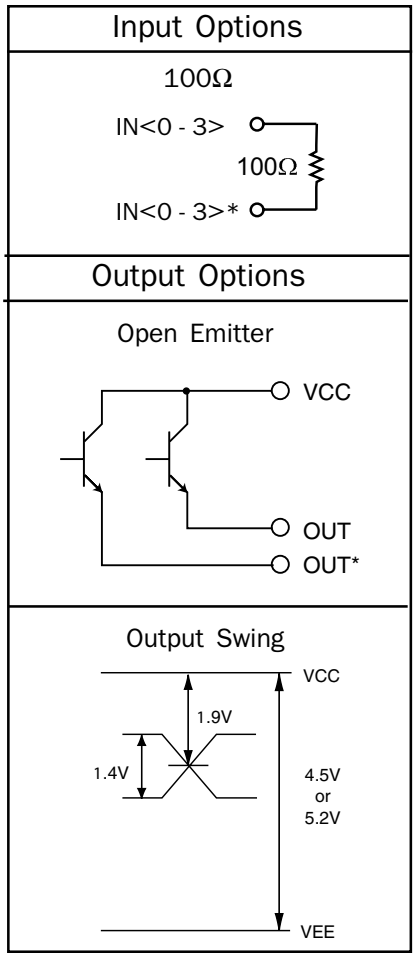


Package Information

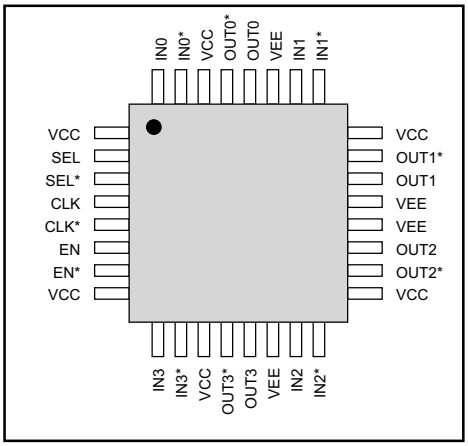
32 pin, 5 mm x 5 mm TQFP Package

Features

- Quad Buffer/Receiver
- 3 GHz Fmax
- 3.3V / 5.2V Compatible



Pin Description



DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	IIH IIL	+1 -1		+25 +1	µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range	| OUT - OUT* | (OUT + OUT*) / 2	1.2 VCC - 2.1	1.4 VCC -1.9	 VCC - 1.7	V V
Power Supply					
Power Supply Current Power Supply Voltage	IEE VCC - VEE	 4.2	90	115 5.5	mA V

DC Test Conditions: Outputs terminated with 50Ω to VCC – 3.3V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1) CLK to OUT[0:3] (SEL = 0)	 Tpd Tpd	 250 430	 350 530	 450 630	 ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	250			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		200	250	ps
Temperature Coefficient (Note 1)	ΔTpd /ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC – 2V

Note:

1. Guaranteed by characterization. Not production tested.

Description

The SK4414 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asychronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input.

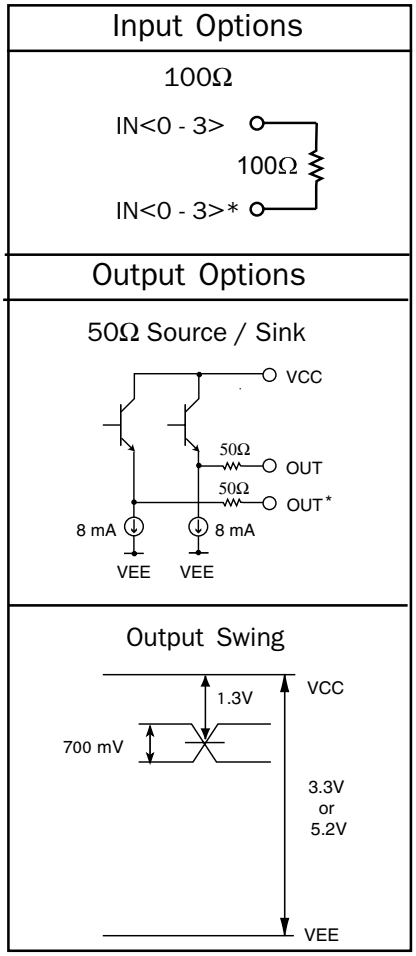
The SK4414 has 100Ω input termination resistors across each of the four inputs to help reduce system component count and increase integration.

The SK4414 uses 50Ω outputs with sink/source capability, and is optimized for applications that require:

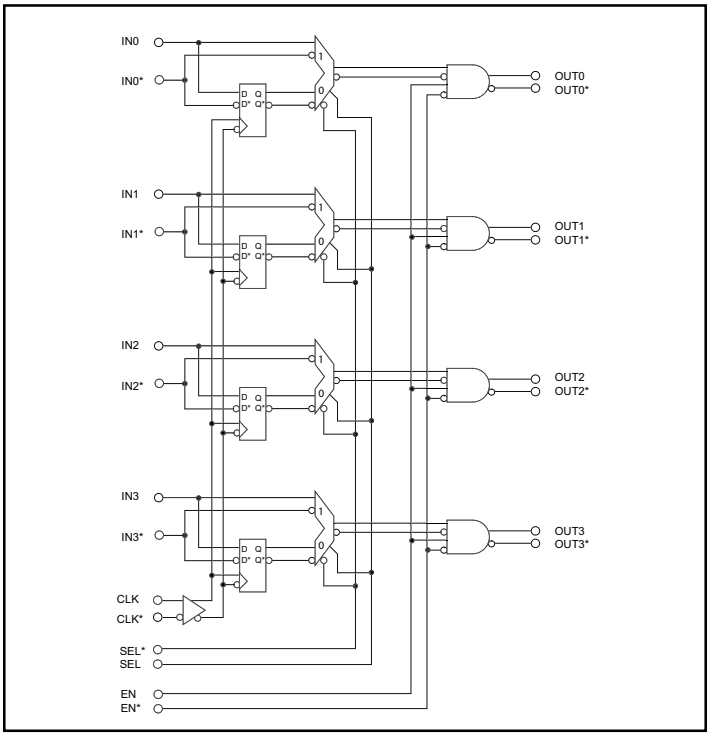
- Point to point, double terminated, timing critical lines
- Point to point, series terminated, timing critical lines

Features

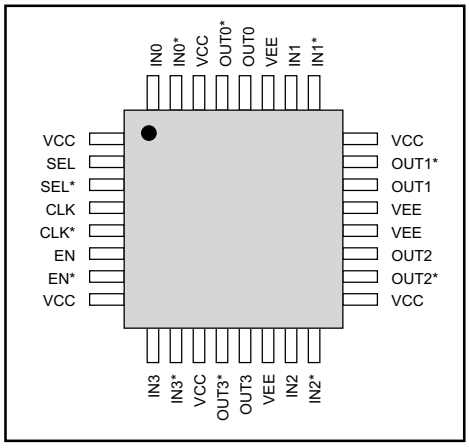
- Quad Buffer/Receiver
- 3 GHz Fmax
- 3.3V / 5.2V Compatible



Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current IN / IN* Differential Input Resistance	 IIH IIL RIN	 +1 -1 100 - TBD	 100	 +25 +1 100 + TBD	 µA µA W
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VCC - 1.5 6.5 40	700 VCC - 1.3 8 45	 VCC - 1.1 10.0 50	mV V mA W
Power Supply					
Power Supply Current Power Supply Voltage	IEE VCC - VEE	 3.0	155	197 5.5	mA V

DC Test Conditions: Outputs unterminated.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1) CLK to OUT[0:3] (SEL = 0)	 Tpd Tpd	 250 430	 350 530	 450 630	 ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient (Note 1)	ΔTpd /ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC – 2V

Note:

1. Guaranteed by characterization. Not production tested.

Description

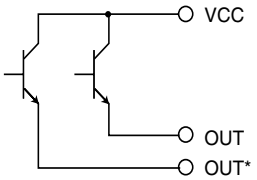
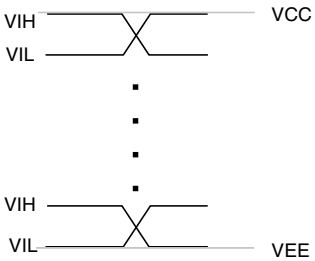
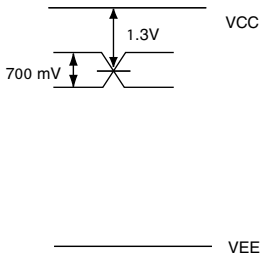
The SK4425 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asychronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

The SK4425 uses standard open emitter ECL outputs optimized for:

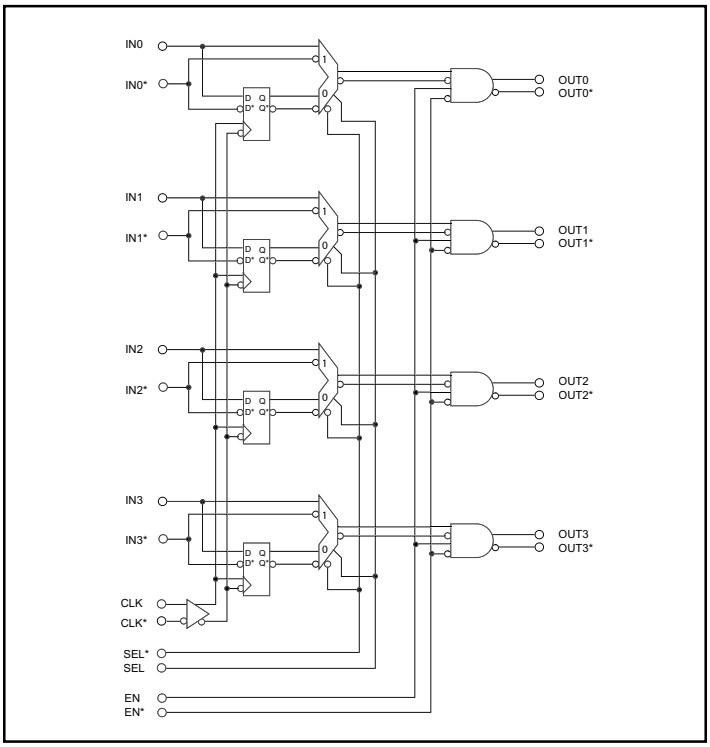
- Standard, general purpose ECL applications
- Multiple destinations (daisy chain).

Features

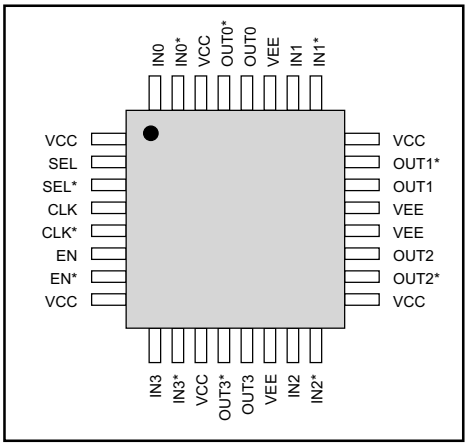
- Quad Buffer / Receiver
- 3 GHz Fmax
- Anything to PECL Translation

Input Options	Output Options
Open IN<0 - 3> IN<0 - 3>*	Open Emitter 
Input Swing	Output Swing
	

Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC -.2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL -SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	IIH IIL	+1 -1		+25 +1	µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range	| OUT -OUT* | (OUT + OUT*) / 2	600 VCC -1.5	700 VCC -1.3	 VCC -1.1	mV V
Power Supply					
Power Supply Current Positive Supply Voltage Negative Supply Voltage	IEE VCC VEE	 2.0 -3.6	90 3.3 -3.3	115 3.6 -2.0	mA V V

DCTest Conditions: Outputs terminated with 50Ω to VCC – 2V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1) CLK to OUT[0:3] (SEL = 0)	 Tpd Tpd	 250 430	 350 530	 450 630	 ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient (Note 1)	ΔTpd /ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC – 2V

Note:

1. Guaranteed by characterization. Not production tested.

Description

The SK4426 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asychronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

The SK4426 uses standard open emitter ECL outputs optimized for:

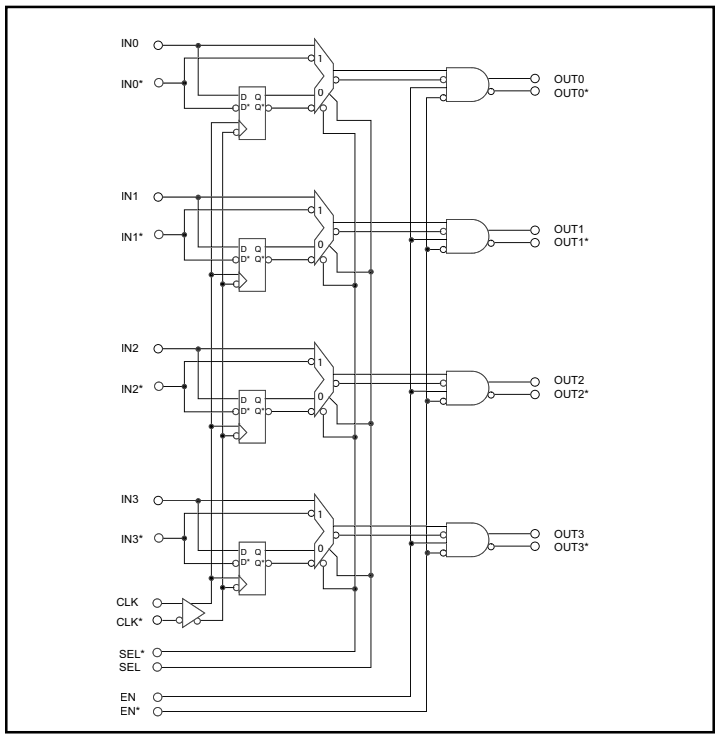
- Standard, general purpose ECL applications
- Multiple destinations (daisy chain).

Features

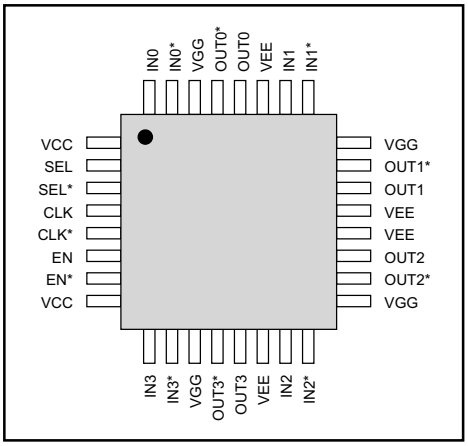
- Quad Buffer/Receiver
- 3 GHz Fmax
- Anything to ECL Translation

Input Options	Output Options
Open IN<0 - 3> IN<0 - 3>*	Open Emitter VGG OUT OUT*
Input Swing	Output Swing
VIH VIL VCC VIH VIL VEE	VGG 1.3V 700 mV VEE

Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC -.2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	IIH IIL	+1 -1		+25 +1	µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range	| OUT - OUT* | (OUT + OUT*) / 2	600 VGG -1.5	700 VGG - 1.3	VGG -1.1	mV V
Power Supply					
Power Supply Current Positive Supply Voltage Negative Supply Voltage	IEE ICC VCC VGG VEE VCC - VGG	 2.0 -.1 -3.6 2.0	90 50 3.3 0 -3.3	115 64 3.6 2.0 -3.0 3.6	mA mA V V V V

DC Test Conditions: Outputs terminated with 50Ω to VGG – 2V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1) CLK to OUT[0:3] (SEL = 0)	 Tpd Tpd	 250 430	 350 530	 450 630	 ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient (Note 1)	ΔTpd /ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC – 2V

Note:

1. Guaranteed by characterization. Not production tested.

Description

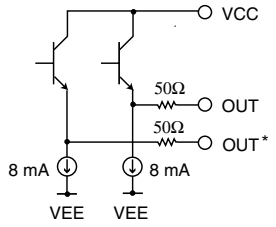
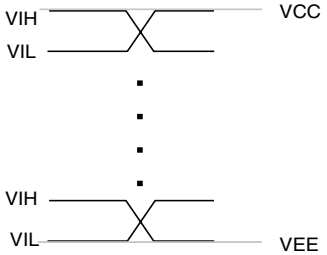
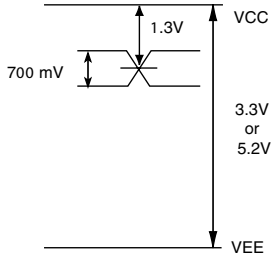
The SK4429 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asychronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

The SK4429 uses 50Ω outputs with sink/source capability, and is optimized for applications that require:

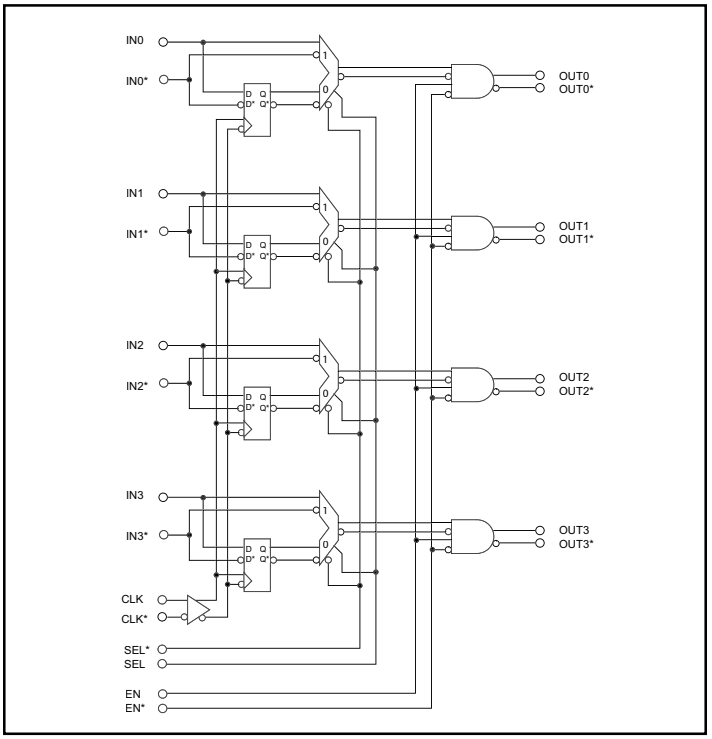
- Point to point, double terminated, timing critical lines
- Point to point, series terminated, timing critical lines

Features

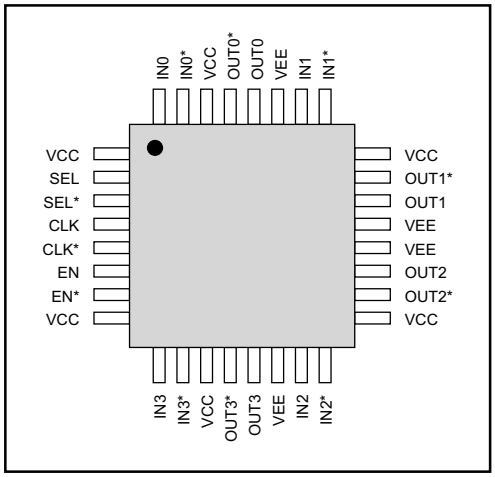
- Quad Buffer/Receiver
- 3 GHz Fmax
- Anything to PECL Translation

Input Options	Output Options
Open IN<0 - 3> IN<0 - 3>*	50Ω Source / Sink 
Input Swing	Output Swing
	

Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 +1 -1		 +25 +1	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VCC - 1.5 6.5 40	700 VCC -1.3 8 45	 VCC - 1.1 10 50	mV V mA W
Power Supply					
Power Supply Current Positive Supply Voltage Negative Supply Voltage	IEE VCC VEE	 2.0 -3.6	155 3.3 -3.3	197 3.6 -2.0	mA V V

DC Test Conditions: Outputs unterminated.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1) CLK to OUT[0:3] (SEL = 0)	 Tpd Tpd	 250 430	 350 530	 450 630	 ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient (Note 1)	ΔTpd / ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC – 2V

Note:

1. Guaranteed by characterization. Not production tested.

Description

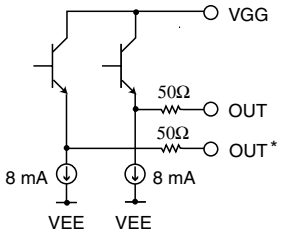
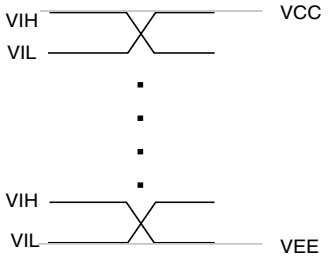
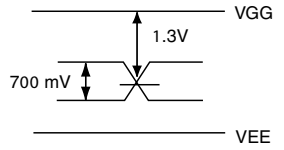
The SK4430 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asychronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

The SK4430 uses 50Ω outputs with sink/source capability, and is optimized for applications that require:

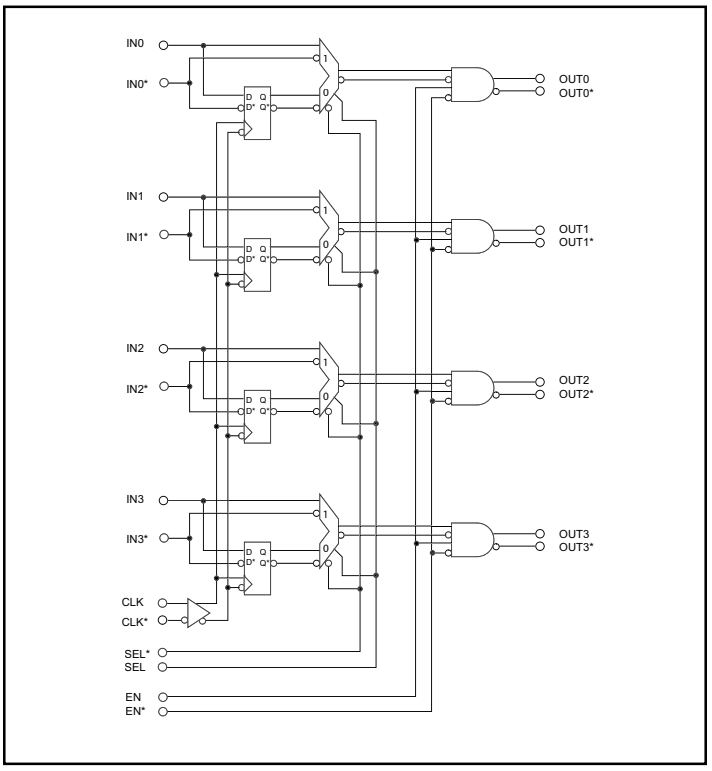
- Point to point, double terminated, timing critical lines
- Point to point, series terminataed, timing critical lines

Features

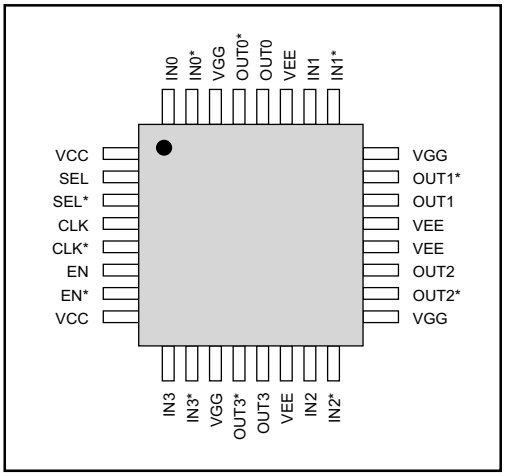
- Quad Buffer/Receiver
- 3 GHz Fmax
- Anything to ECL Translation

Input Options	Output Options
Open IN<0 - 3> IN<0 - 3>*	50Ω Source / Sink 
Input Swing	Output Swing
	

Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	 IIH IIL	 +1 -1		 +25 +1	 µA µA
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VGG - 1.5 6.5 40	700 VGG -1.3 8.0 45	 VGG - 1.1 10.0 50	mV V mA W
Power Supply					
Power Supply Current Positive Supply Voltage Negative Supply Voltage 	IEE ICC VCC VGG VEE VCC - VGG	 2.0 -.1 -3.6 2.0	155 50 3.3 0 -3.3 	197 64 3.6 2.0 -3.0 3.6	mA mA V V V V

DC Test Conditions: Outputs unterminated.

AC Characteristics

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
High Performance Option					
Propagation Delay IN[0:3] to OUT[0;3] (sel - 1) CLK to OUT[0:3] (SEL - 0)	 Tpd Tpd	 250 430	 350 530	 450 630	 ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3.0			GHz
IN to CLK (Note 1) Setup Time Hold Time	 Tsu Th	 100 100			 ps ps
Output rise and Fall Times (20%/80%)	Tr/Tf		125	150	ps
Temperature Coefficient (Note 1)	ΔTpd/ΔT		<1		ps/^{o}C

AC Test Conditions: Outputs terminated with 50Ω to VCC – 2V

Note:

1. Guaranteed by characterization. Not production tested.

Description

The SK4435 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asychronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

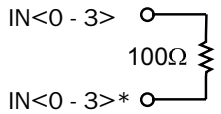
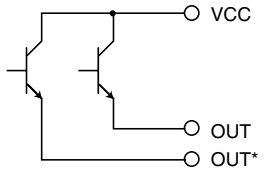
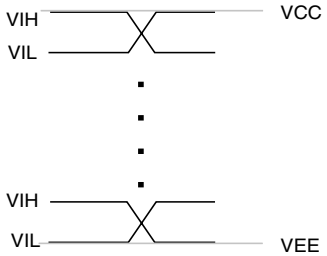
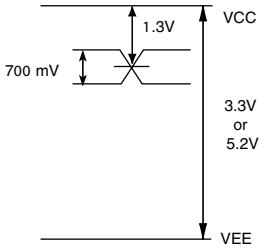
The SK4435 has 100Ω input termination resistors across each of the four inputs to help reduce system component count and increase integration.

The SK4435 uses standard open emitter ECL outputs optimized for:

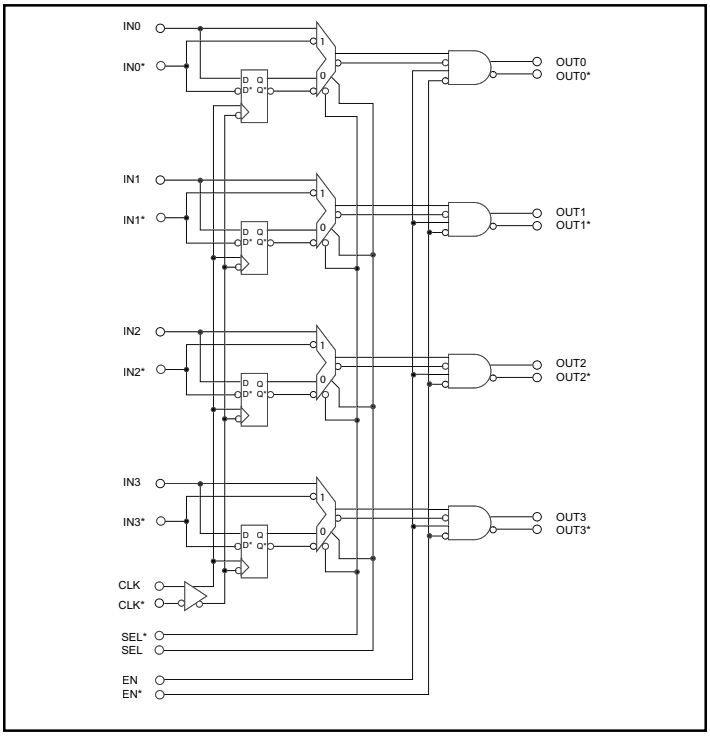
- Standard, general purpose applications
- Multiple destinations (daisy chain).

Features

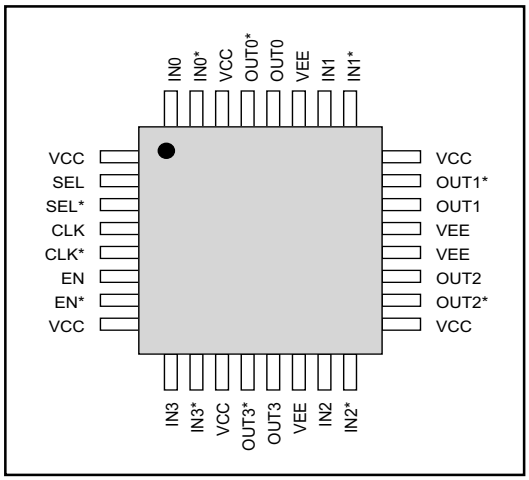
- Quad Buffer/Receiver
- 3 GHz Fmax
- Anything to PECL Translation

Input Options	Output Options
100Ω 	Open Emitter 
Input Swing	Output Swing
	

Functional Block Diagram



Pin Description



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current IN / IN* Differential Input Resistance	 IIH IIL RIN	 +1 -1 100 - TBD	 100	 +25 +1 100 + TBD	 µA µA W
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VCC - 1.5 6.5 40	700 VCC -1.3 8 45	 VCC - 1.1 10 50	mV V mA W
Power Supply					
Power Supply Current Positive Supply Voltage Negative Supply Voltage	IEE VCC VEE	 2.0 -3.6	90 3.3 -3.3	115 3.6 -2.0	mA V V

DC Test Conditions: Outputs terminated with 50Ω to VCC – 2V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1) CLK to OUT[0:3] (SEL = 0)	 Tpd Tpd	 250 430	 350 530	 450 630	 ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient (Note 1)	ΔTpd / ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC – 2V

Note:

1. Guaranteed by characterization. Not production tested.

Description

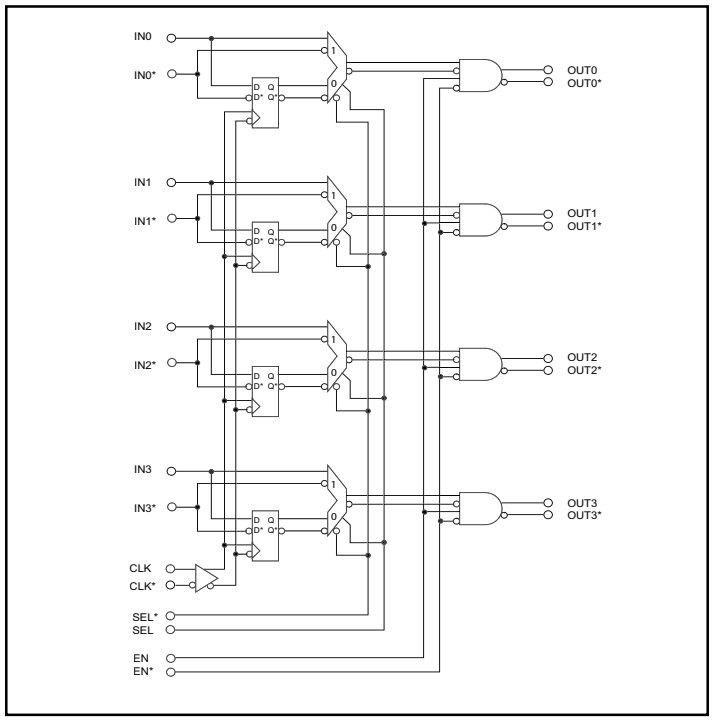
The SK4436 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asychronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

The SK4436 has 100Ω input termination resistors across each of the four inputs to help reduce system component count and increase integration.

The SK4436 uses standard open emitter ECL outputs optimized for:

- Standard, general purpose applications
- Multiple destinations (daisy chain).

Functional Block Diagram

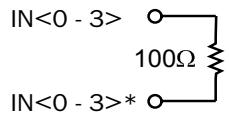
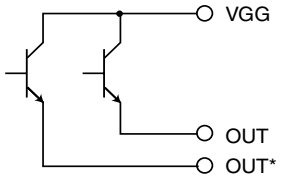
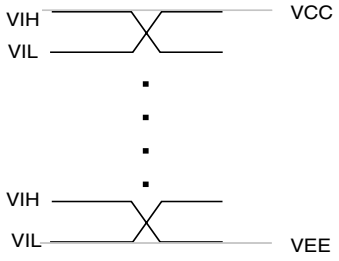
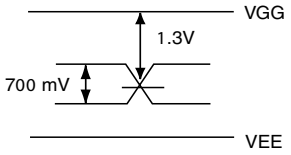


Package Information

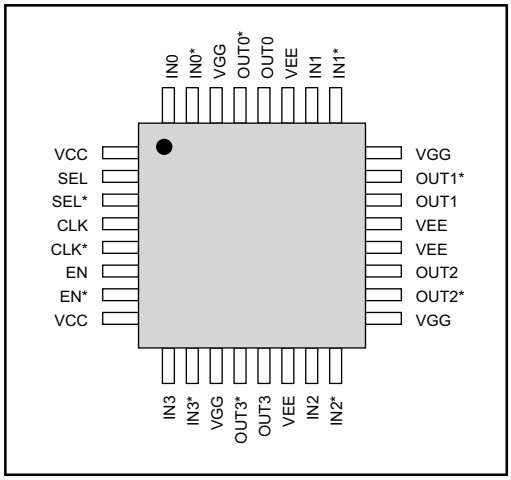
32 pin, 5 mm x 5 mm
TQFP Package

Features

- Quad Buffer/Receiver
- 3 GHz Fmax
- Anything to ECL Translation

Input Options	Output Options
100Ω 	Open Emitter 
Input Swing	Output Swing
	

Pin Description



DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current IN / IN* Differential Input Resistance	 IIH IIL RIN	 +1 -1 100 - TBD	 100	 +25 +1 100 + TBD	 µA µA W
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VGG - 1.5 6.5 40	700 VGG -1.3 8.0 45	 VGG - 1.1 10.0 50	mV V mA W
Power Supply					
Power Supply Current Positive Supply Voltage Negative Supply Voltage 	IEE ICC VCC VGG VEE VCC - VGG	 2.0 -0.1 -3.6 2.0	90 50 3.3 0 -3.3	115 64 3.6 2.0 -3.0 3.6	mA mA V V V V

DCTest Conditions: Outputs terminated with 50Ω to VGG – 2V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1) CLK to OUT[0:3] (SEL = 0)	 Tpd Tpd	 250 430	 350 530	 450 630	 ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient (Note 1)	ΔTpd / ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC – 2V

Note:

1. Guaranteed by characterization. Not production tested.

Description

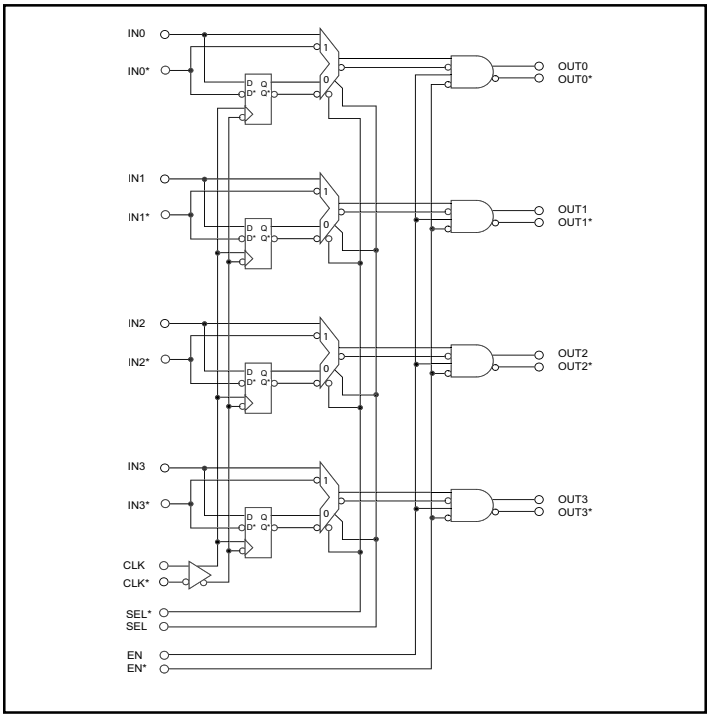
The SK4439 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asychronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

The SK4439 has 100Ω input termination resistors across each of the four inputs to help reduce system component count and increase integration.

The SK4439 uses 50Ω outputs with sink/source capability, and is optimized for applications that require:

- Point to point, double terminated, timing critical lines
- Point to point, series terminataed, timing critical lines

Functional Block Diagram

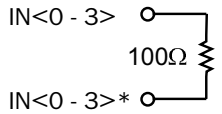
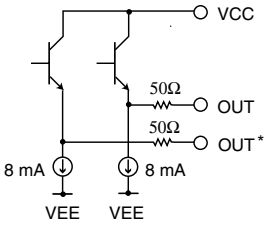
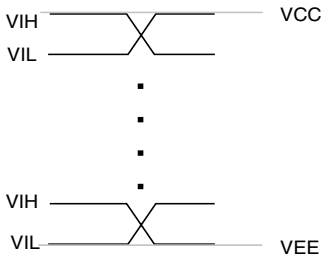
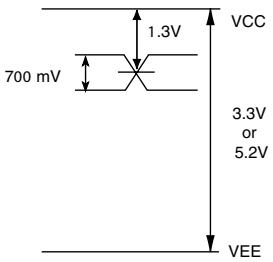


Package Information

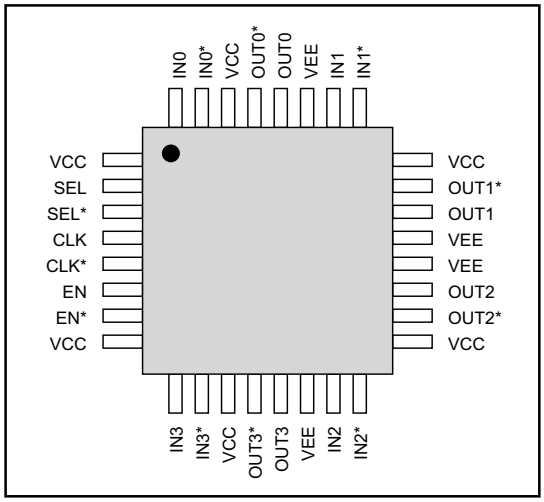
32 pin, 5 mm x 5 mm
TQFP Package

Features

- Quad Buffer/Receiver
- 3 GHz Fmax
- Anything to PECL Translation

Input Options	Output Options
100Ω 	50Ω Source / Sink 
Input Swing 	Output Swing 

Pin Description



DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current IN / IN* Differential Input Resistance	 IIH IIL RIN	 +1 -1 100 - TBD	 100	 +25 +1 100 + TBD	 µA µA W
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	 IIH, IIL	 -420		 +250	 µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VCC - 1.5 6.5 40	700 VCC -1.3 8 45	 VCC - 1.1 10 50	mV V mA W
Power Supply					
Power Supply Current Positive Supply Voltage Negative Supply Voltage	IEE VCC VEE	 2.0 -3.6	155 3.3 -3.3	197 3.6 -3.0	mA V V

DC Test Conditions: Outputs unterminated.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1) CLK to OUT[0:3] (SEL = 0)	 Tpd Tpd	 250 430	 350 530	 450 630	 ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient (Note 1)	ΔTpd / ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC – 2V

Note:

1. Guaranteed by characterization. Not production tested.

Description

The SK4440 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asychronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

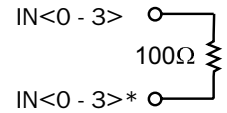
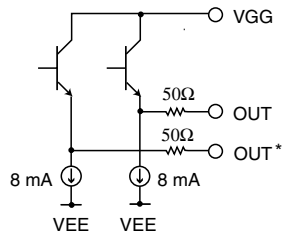
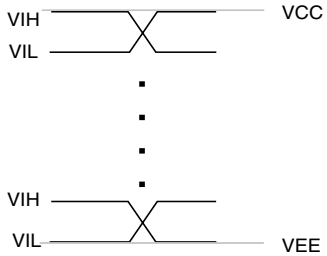
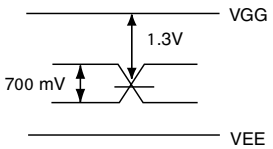
The SK4440 has 100Ω input termination resistors across each of the four inputs to help reduce system component count and increase integration.

The SK4440 uses 50Ω outputs with sink/source capability, and is optimized for applications that require:

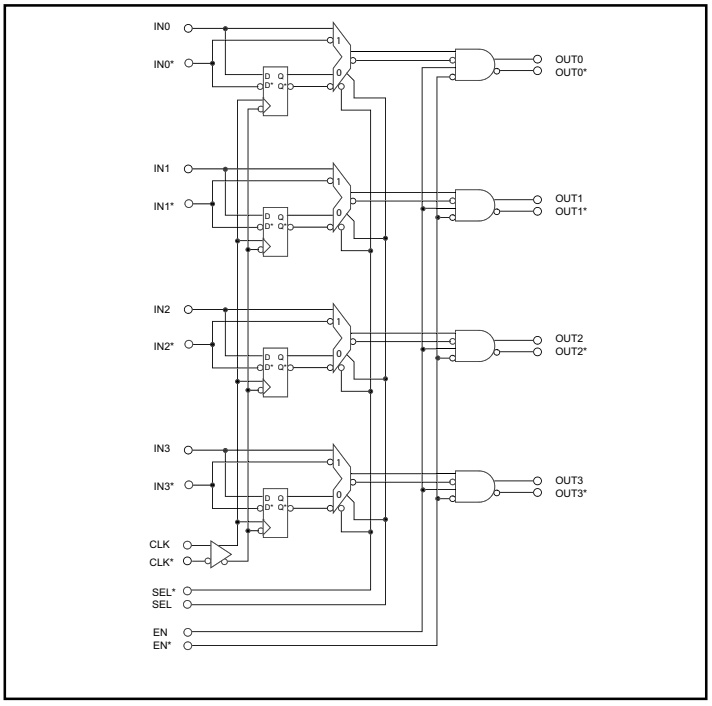
- Point to point, double terminated, timing critical lines
- Point to point, series terminated, timing critical lines

Features

- Quad Buffer/Receiver
- 3 GHz Fmax
- Anything to ECL Translation

Input Options	Output Options
100Ω 	50Ω Source / Sink 
Input Swing 	Output Swing 

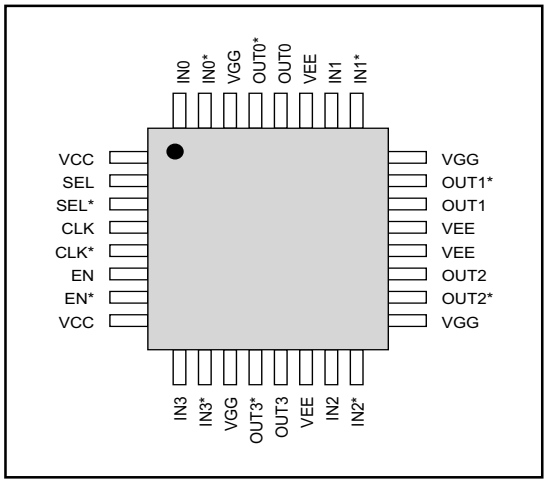
Functional Block Diagram



Package Information

32 pin, 5 mm x 5 mm
TQFP Package

Pin Description



DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - .2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	| Input - Input* |	.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current IN / IN* Differential Input Resistance	 IIH IIL RIN	 +1 -1 100 - TBD	 100	 +25 +1 100 + TBD	 µA µA W
Functional Inputs (IN / IN*, SEL / SEL*) Input Current	IIH, IIL	-420		+250	µA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	| OUT - OUT* | (OUT + OUT*) / 2 ISINK ROUT	600 VGG - 1.5 6.5 40	700 VGG -1.3 8.0 45	 VGG - 1.1 10.0 50	mV V mA W
Power Supply					
Power Supply Current Positive Supply Voltage Negative Supply Voltage 	IEE ICC VCC VGG VEE VCC - VGG	 2.0 -0.1 -3.6 2.0	155 50 3.3 0 -3.3 	197 64 3.6 0.2 -2.0 3.6	mA mA V V V V

DC Test Conditions: Outputs unterminated.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1) CLK to OUT[0:3] (SEL = 0)	 Tpd Tpd	 250 430	 350 530	 450 630	 ps ps
Channel to Channel Skew				<20	ps
Maximum Operating Frequency (Note 1)	Fmax	3			GHz
Minimum Pulse Width (Note 1)	PW min	160			ps
IN to CLK (Note 1) Set Up Time Hold Time	 Tsu Th	 100 100			 ps ps
Output Rise and Fall Times (20% / 80%)	Tr / Tf		125	150	ps
Temperature Coefficient (Note 1)	ΔTpd / ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC – 2V

Note:

1. Guaranteed by characterization. Not production tested.

Ordering Information

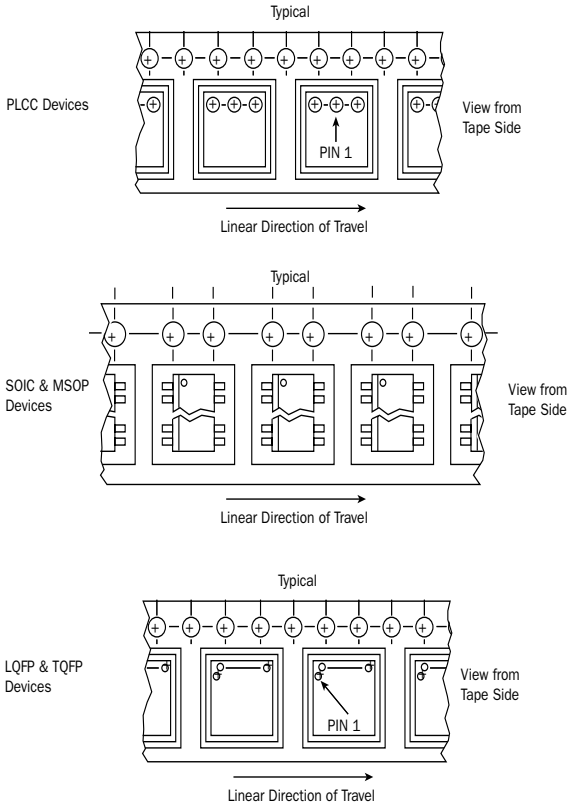
Ordering Code	Package ID	Temperature Range
SK4400	32-TQFP 5 x 5 mm	Commercial
SK4401	32-TQFP 5 x 5 mm	Commercial
SK4404	32-TQFP 5 x 5 mm	Commercial
SK4410	32-TQFP 5 x 5 mm	Commercial
SK4411	32-TQFP 5 x 5 mm	Commercial
SK4414	32-TQFP 5 x 5 mm	Commercial
SK4425	32-TQFP 5 x 5 mm	Commercial
SK4426	32-TQFP 5 x 5 mm	Commercial
SK4429	32-TQFP 5 x 5 mm	Commercial
SK4430	32-TQFP 5 x 5 mm	Commercial
SK4435	32-TQFP 5 x 5 mm	Commercial
SK4436	32-TQFP 5 x 5 mm	Commercial
SK4439	32-TQFP 5 x 5 mm	Commercial
SK4440	32-TQFP 5 x 5 mm	Commercial

Note: For tape and reel, add the letter “T” at the end of ordering code.

Device Type	Tape Width (mm)	Max Device/Reel	Reel Size (inch)	Max Device/Tube
PLCC-28	24	750	13	38
SOIC-8	12	2,500	13	98
SOIC-16	16	2,500	13	49
SOIC-20	24	1,000	13	38
MSOP-8	12	2,500	13	50
MSOP-10	12	2,500	13	50
LQFP-32 (7 x 7 mm)	16	1,000	13	250 (tray)
TQFP-32 (7 x 7 mm)	16	1,000	13	250 (tray)
TQFP-32 (5 x 5 mm)	16	1,000	13	360 (tray)

Tape and Reel

Semtech's tape and reel packaging fully conforms to the latest EIA-481-1A and EIA-481-2A specifications. The antistatic embossed tape provides a secure cavity sealed with a peel-back cover tape.



Ordering Information

To order devices which are to be delivered in Tape and Reel, add the suffix T to the device number being ordered.

Contact Information

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High-Performance Products Division

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San Diego, CA 92131
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FAX: (858)695-2633

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