SEMTECH

÷2, ÷4, ÷8 Clock Generation Chip

HIGH-PERFORMANCE PRODUCTS

Description

The SK10/100EL34W are low skew, ÷2, ÷4, ÷8 clock generation chips designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. This device is fully compatible with On-Semiconductor's MC10EL34 and MC100EL34. These devices can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the VBB output, a sinusoidal source can be AC-coupled into the device. The EL34W provides a VBB output for single-ended use or DC bias for AC coupling to the device. VBB is an output pin and should be used as a bias for the EL34W as its current source/sink capability is limited up to 0.5 mA. Whenever used, the VBB output should be bypassed to VCC via a 0.01 µF capacitor.

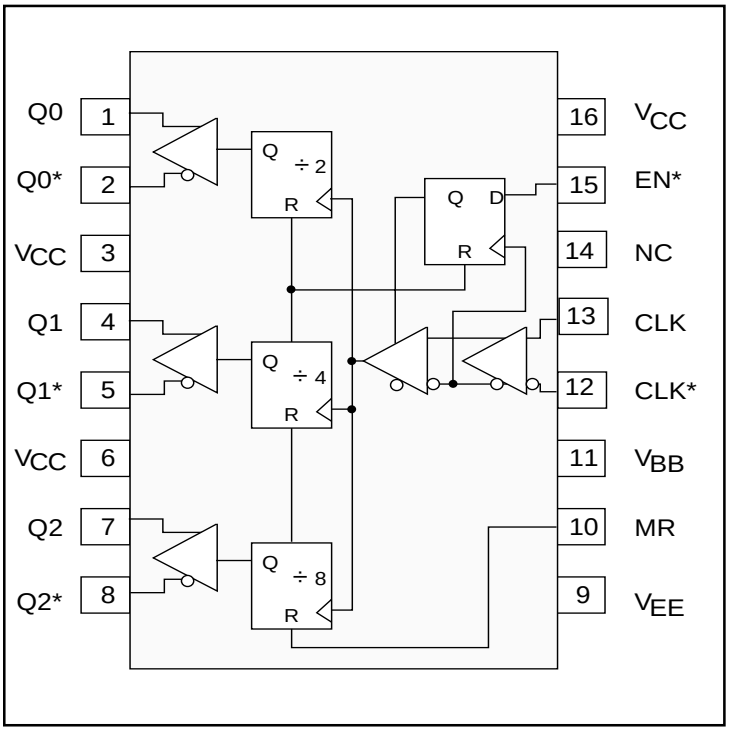
The common enable (EN*) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as for multiple EL34Ws in a system.

Features

- Extended Supply Voltage Range: (VEE = –3.0V to –5.5V, VCC = 0V) or (VCC = +3.0V to +5.5V, VEE = 0V)
- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- Internal 75KΩ Input Pull-Down Resistors
- Fully Compatible with MC10EL34 and MC100EL34
- Specified Over Industrial Temperature Range: –40°C to 85°C
- ESD Protection of >4000V
- Available in 16-Pin SOIC Package

Functional Block Diagram



Pin Descriptions

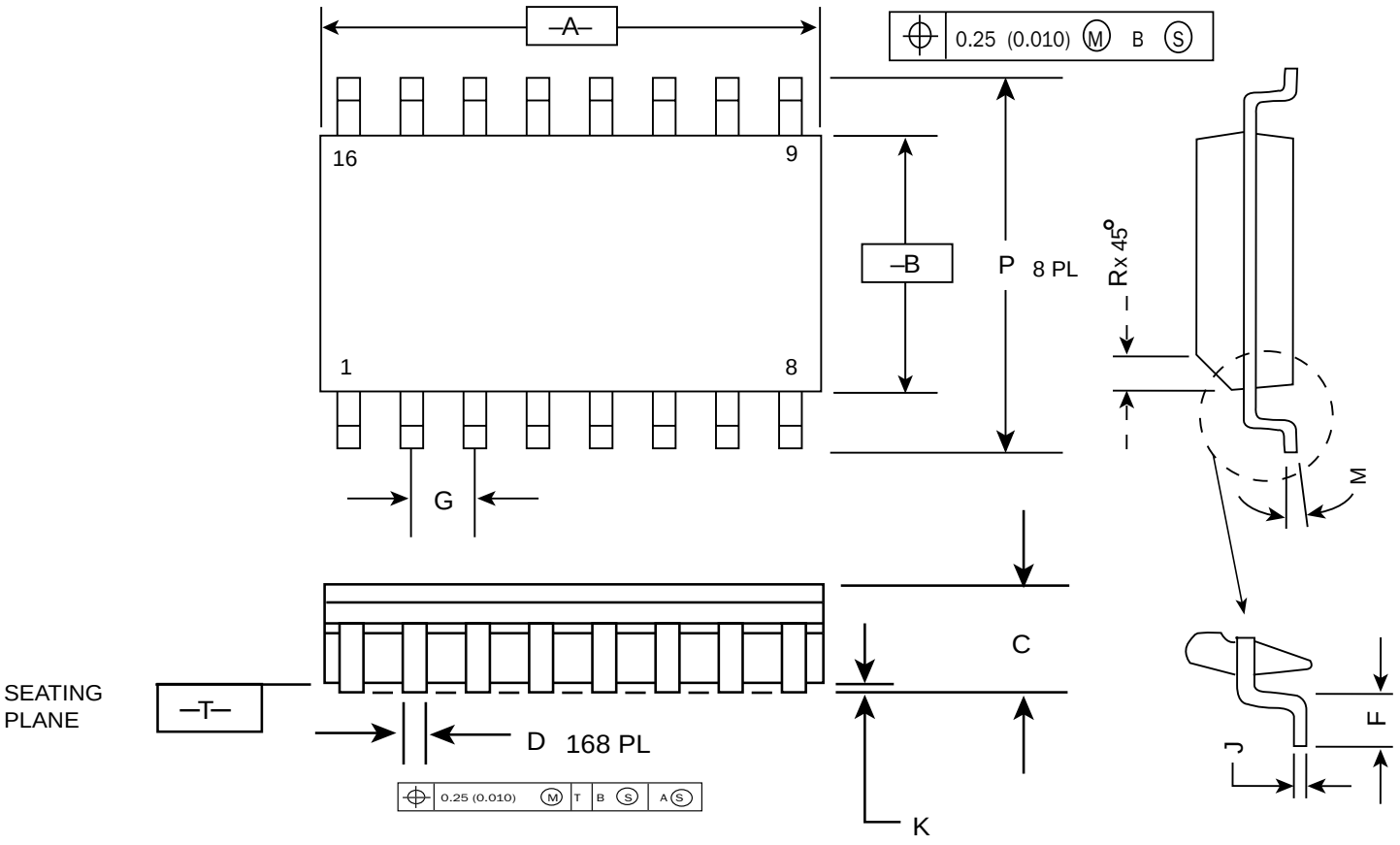
Pin Name	Function
CLK	Differential Clock Inputs
EN*	Synchronous Enable
MR	Master Reset
V_{BB}	Reference Output
Q0, Q0*	Differential ÷2 Outputs
Q1, Q1*	Differential ÷4 Outputs
Q2, Q2*	Differential ÷8 Outputs

CLK	EN*	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q0–2
X	X	H	Reset Q0–2

Z = Low-to-High transition
ZZ = High-to-Low transition

Truth Table

16 Pin SOIC Package



DIM	Millemeters		Inches	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Dimensions A and B do not include mold protrusion.
4. Maximum mold protrusion 0.150 (0.006) per side.
5. Dimension D does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.13 (0.005) total in excess of d dimension at maximum material condition.

DC Characteristics

SK10/100EL34W DC Electrical Characteristics (Notes 1, 2)

(V_{CC} – V_{EE} = +3.0V to +5.5V ; V_{OUT} loaded 50Ω to V_{CC} – 2.0V)

Symbol	Characteristic	TA = –40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{IN}	Input Current (Diff) (SE)	-150		150 150	-150		150 150	-150		150 150	-150		150 150	µA µA
I_{EE}	Power Supply Current 10EL 100EL	 26 26		 43 44	 27 27		 45 45	 27 27		 45 46	 27 29		 46 48	 mA mA
V_{BB}	Output Reference Voltage[5] 10EL 100EL	 –1.43 –1.38		 –1.3 –1.26	 –1.38 –1.38		 –1.27 –1.26	 –1.35 –1.38		 –1.25 –1.26	 –1.31 –1.38		 –1.19 –1.26	 mV mV
V_{CC} – V_{EE}	Power Supply Voltage	3.0		5.5	3.0		5.5	3.0		5.5	3.0		5.5	V

AC Characteristics

SK10/100EL34W AC Electrical Characteristics

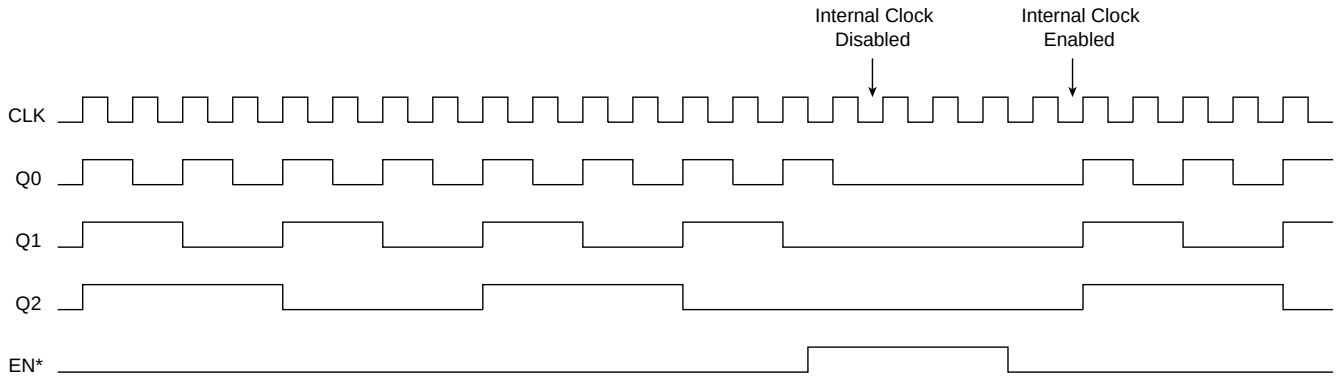
(V_{CC} – V_{EE} = +3.0V to +5.5V ; V_{OUT} loaded 50Ω to V_{CC} – 2.0V)

Symbol	Characteristic	TA = –40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency	1100			1100			1100			1100			MHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK MR	 840 585		 1035 770	 875 635		 1070 830	 890 655		 1100 860	 935 695		 1170 955	 ps ps
t_S	Setup Time EN*	400			400			400			400			ps
t_H	Hold Time EN*	250			250			250			250			ps
V_{PP}	Minimum Input Swing CLK[3]	250		1000	250		1000	250		1000	250		1000	mV
V_{CMR}	Common Mode Range CLK[4]	VEE + 2.0		VCC _ 0.4	VEE + 2.0		VCC _ 0.4	VEE + 2.0		VCC _ 0.4	VEE + 2.0		VCC _ 0.4	V
t_r , t_f	Output Rise/Fall Times Q (20% to 80%)	205		335	215		350	220		355	235		375	ps

AC Characteristics *(continued)*

Notes:

1. 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to VCC – 2.0V.
2. 100K circuits are designed to meet the DC specification shown in the table where transverse airflow greater than 500 lfpm is maintained.
3. Minimum input swing for which AC parameters guaranteed.
4. CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between $VPP_{(min)}$ and 1V. The lower end of the CMR range varies 1:1 with VEE and is equal to VEE + 2.0V.
5. Voltages referenced to VCC = 0V, ECL configuration.
6. For standard ECL DC specifications, refer to the ECL Logic Family Standard DC Specifications Data Sheet.
7. For part ordering description, see HPP Part Ordering Information Data Sheet.



Timing Diagram

The EN* signal will freeze the internal clocks to the flip-flops on the first falling edge of CLK after its assertion. The internal dividers will maintain their state during the internal clock freeze and will return to clocking once the internal clocks are unfrozen. The outputs will transition to their next states in the same manner, time, and relationship as they would have had the EN* signal not been asserted.

Ordering Information

Ordering Code	Package ID	Temperature Range
SK10EL34WD	16-SOIC	Industrial
SK10EL34WDT	16-SOIC	Industrial
SK100EL34WD	16-SOIC	Industrial
SK100EL34WDT	16-SOIC	Industrial
SK10EL34WU	Die	
SK100EL34WU	Die	

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