

Document Title**128K x16 bit Low Power and Low Voltage CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial Draft	October 1, 1997	Preliminary
1.0	Finalize - Change operation voltage: Vcc=2.3~3.3V → Vcc=2.3~2.7V - Release operating current Icc=2mA → 5mA Icc1 Read/Write=3/15mA → 5/20mA	August 27, 1998	Final

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128K x16 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology: TFT
- Organization: 128Kx16
- Power Supply Voltage
K6T2016S3M Family: 2.3~2.7V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type: 44-TSOP2 -400F

GENERAL DESCRIPTION

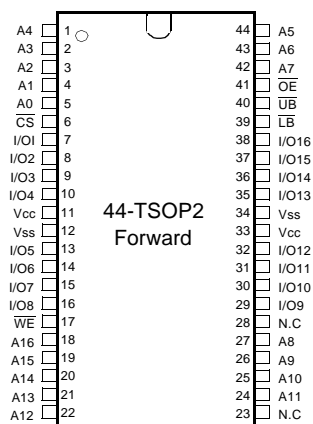
The K6T2016S3M families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and small package for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Produc Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I _{SB1} , Max)	Operating (I _{CC2} ,Max)	
K6T2016S3M-B	Commercial(0~70°C)	2.3~2.7V	120 ¹⁾ /150ns	10μA	45mA	44-TSOP2-F
K6T2016S3M-F	Industrial(-40~85°C)			15μA		

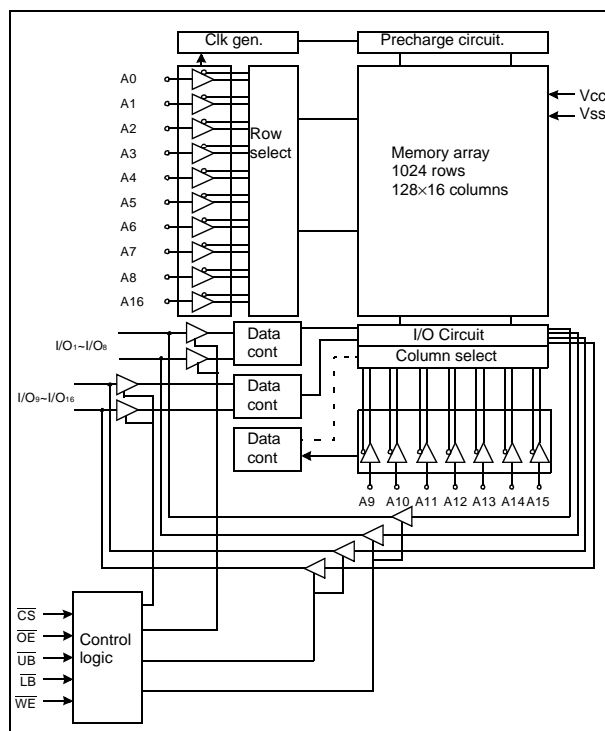
1. The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
CS	Chip Select Input	I/O ₁ ~I/O ₁₆	Data Inputs/Outputs
OE	Output Enable Input	A ₀ ~A ₁₆	Address Inputs
WE	Write Enable Input	Vcc	Power
UB	Upper Block Select Input	Vss	Ground
LB	Lower Block Select Input	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temperature Product(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
K6T2016S3M-TB12	44-TSOP2, 120ns, 2.3~2.7V, LL	K6T2016S3M-TF12	44-TSOP2, 120ns, 2.3~2.7V, LL
K6T2016S3M-TB15	44-TSOP2, 150ns, 2.3~2.7V, LL	K6T2016S3M-TF15	44-TSOP2, 150ns, 2.3~2.7V, LL

Note : LL - Low Low Standby Current

FUNCTIONAL DESCRIPTION

\overline{CS}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O ₁₋₈	I/O ₉₋₁₆	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
L	H	H	X ¹⁾	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	Word Read	Active
L	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	X ¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be in low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to V _{ss}	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5	V	-
Voltage on V _{CC} supply relative to V _{ss}	V _{CC}	-0.3 to 4.6	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	K6T2016S3M-L
		-40 to 85	°C	K6T2016S3M-P
Soldering temperature and time	T _{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	K6T2016S3M Family	2.3	2.5	2.7	V
Ground	V _{SS}	All Family	0	0	0	V
Input high voltage	V _{IH}	K6T2016S3M Family	2.0	-	V _{CC} +0.3 ²⁾	V
Input low voltage	V _{IL}	K6T2016S3M Family	-0.3 ³⁾	-	0.6	V

Note:

- Commercial Product : T_A=0 to 70°C, otherwise specified
Industrial Product : T_A=-40 to 85°C, otherwise specified
- Overshoot : V_{CC}+1.0V in case of pulse width ≤ 20ns
- Undershoot : -1.0V in case of pulse width ≤ 20ns
- Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

- Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

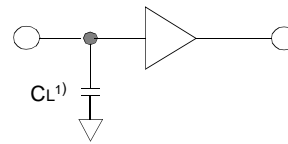
Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IL} or V _{IH} , Read	-	-	5	mA	
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty I _{IO} =0mA, $\overline{CS} \leq 0.2V$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	Read	-	-	5	mA
			Write	-	-	20	
	I _{CC2}	Cycle time=Min, 100% duty	-	-	45	mA	
Output low voltage	V _{OL}	I _{OL} =0.5mA at 2.3~2.7V	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} =-0.5mA	2.0	-	-	V	
Standby Current(TTL)	I _{SB}	$\overline{CS}=V_{IH}$, Other inputs=V _{IL} or V _{IH}	-	-	0.3	mA	
Standby Current (CMOS)	I _{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, Other inputs=0~V _{CC}	-	-	10 ¹⁾	μA	

- K6T2016S3M-I Family =15μA

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.4 to 2.2V
 Input rising and falling time : 5ns
 Input and output reference voltage : 1.5V
 Output load (See right) : $C_L = 100\text{pF} + 1\text{TTL}$
 $C_L^1 = 30\text{pF} + 1\text{TTL}$



1. Including scope and jig capacitance

1. Refer to AC CHARACTERISTICS

AC CHARACTERISTICS ($V_{CC} = 2.3 \sim 2.7\text{V}$, K6T2016S3M-L Family : $T_A = 0$ to 70°C , K6T2016S3M-I Family : $T_A = -40$ to 85°C)

Parameter List		Symbol	Speed Bins				Units
			120 ¹ ns		150ns		
			Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	120	-	150	-	ns
	Address access time	t _{AA}	-	120	-	150	ns
	Chip select to output	t _{CO}	-	120	-	150	ns
	Output enable to valid output	t _{OE}	-	60	-	75	ns
	Byte enable to valid output	t _{BA}	-	60	-	75	ns
	Chip select to low-Z output	t _{LZ}	20	-	20	-	ns
	Output enable to low-Z output	t _{OLZ}	10	-	10	-	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ enable to low-Z output	t _{BLZ}	10	-	10	-	ns
	Output hold from address change	t _{OH}	15	-	15	-	ns
	Chip disable to high-Z output	t _{HZ}	-	35	0	40	ns
	Output disable to high-Z output	t _{OHZ}	-	35	0	40	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ disable to high-Z output	t _{BHZ}	-	35	0	40	ns
Write	Write cycle time	t _{WC}	120	-	150	-	ns
	Chip select to end of write	t _{CW}	100	-	120	-	ns
	Address set-up time	t _{AS}	0	-	0	-	ns
	Address valid to end of write	t _{AW}	100	-	120	-	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ valid to end of write	t _{BW}	100	-	120	-	ns
	Write pulse width	t _{WP}	80	-	100	-	ns
	Write recovery time	t _{WR}	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	30	0	40	ns
	Data to write time overlap	t _{DW}	50	-	60	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	ns

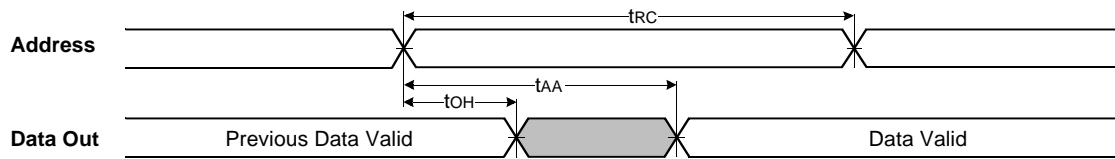
1. The parameter is measured with 30pF test load.

DATA RETENTION CHARACTERISTICS

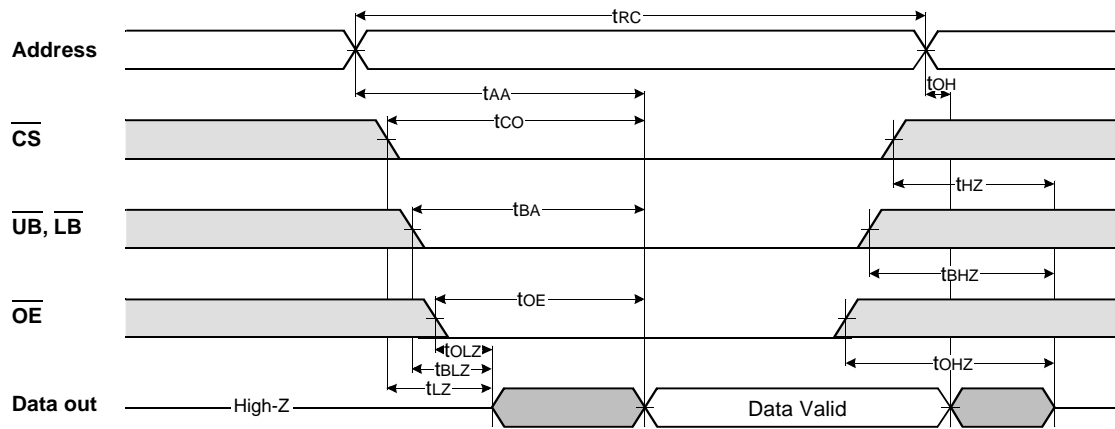
Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{\text{CS}} \geq V_{CC} - 0.2\text{V}$	2.0	-	2.7	V
Data retention current	I _{DR}	$V_{CC} = 2.0\text{V}$, $\overline{\text{CS}} \geq V_{CC} - 0.2\text{V}$	-	-	10	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, \overline{UB} or/and $\overline{LB}=V_{IL}$)



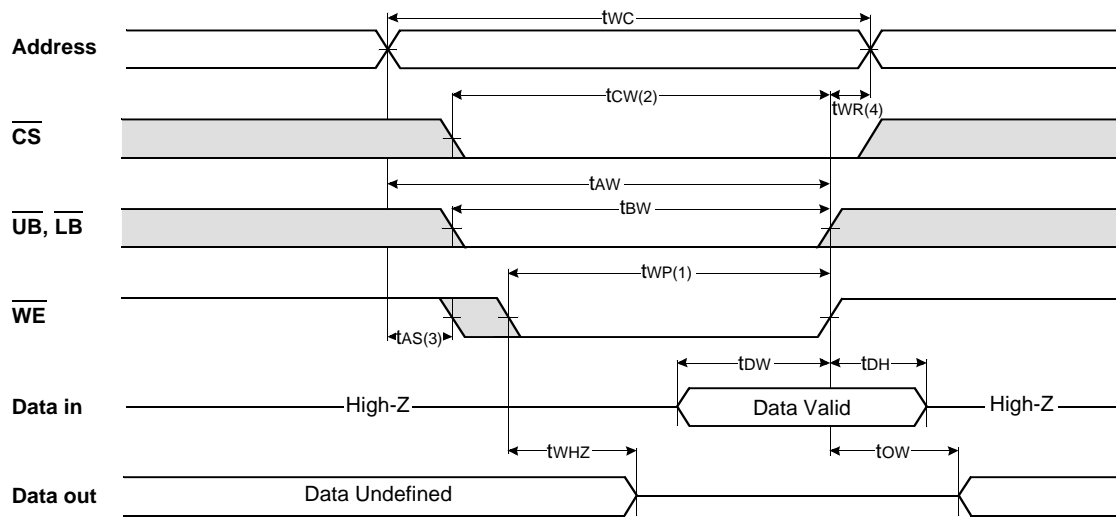
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



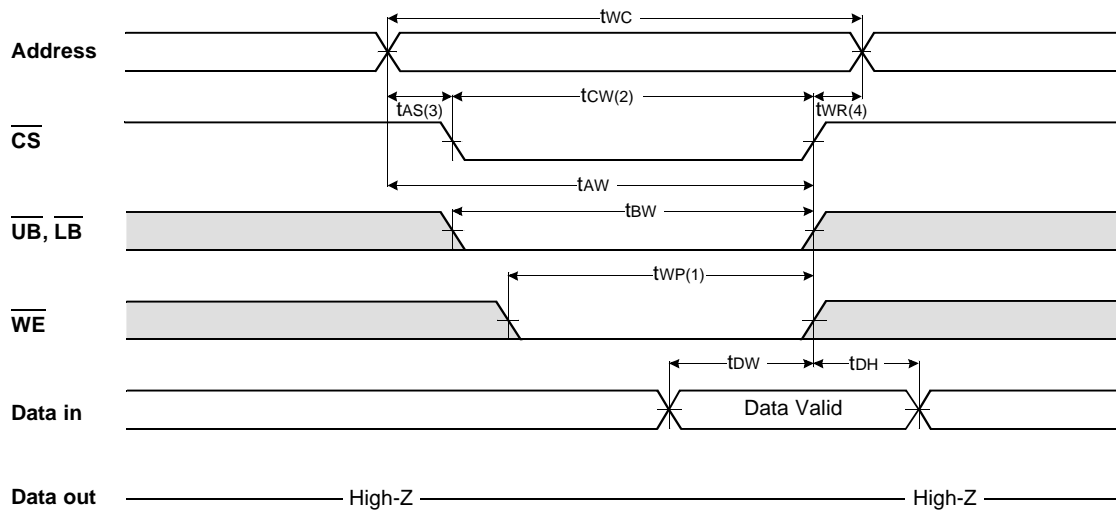
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

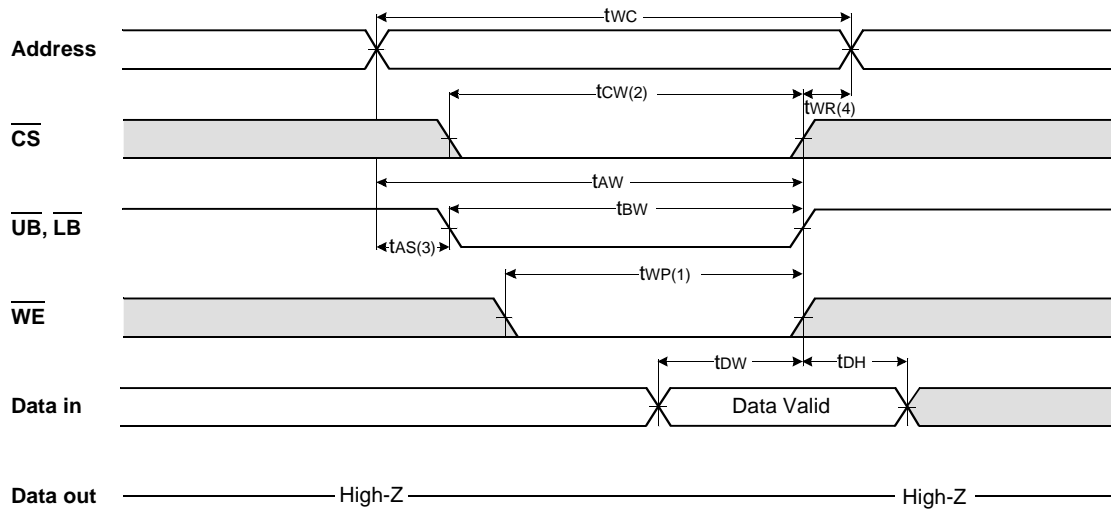
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{CS} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{UB} , \overline{LB} Controlled)

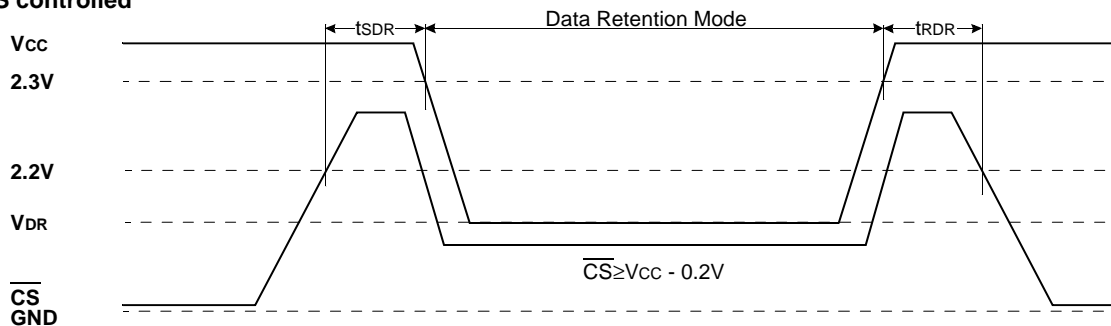


NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.

DATA RETENTION WAVE FORM

\overline{CS} controlled



PACKAGE DIMENSIONS

Unit : millimeter(inch)

44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)

