Document Title

128Kx8 Super Low Power and Low Voltage Full CMOS SRAM Data Sheets for 48-CSP

Revision History

Rev.No.	History	Draft Data	Remark
Rev. 0.0	- 1′st edition - Package Dimension Finalized	Feb. 6′th, 1997	Preliminary
Rev. 0.1	- 2′nd edition - Change speed marking method Marking was indicate speed at high power, that change to speed at low power	Apr. 18′th, 1997	Preliminary

128Kx8 bit Super Low Power and Low Voltage Full CMOS SRAM with 48-CSP(Chip Scale Package)

FEATURES SUMMARY

- Process Technology : 0.4µm Full CMOS
- Organization : 128Kx8
- Power Supply Voltage
  KM68FS1000Z Family : 2.3V(Min) ~ 3.3V(Max)
  KM68FR1000Z Family : 1.8V(Min) ~ 2.7V(Max)
- Low Data Retention Voltage : 1.5V(Min)
- Three state output and TTL Compatible
- Package Type : 48-CSP with 0.75mm ball pitch

GENERAL DESCRIPTION

The KM68FS1000Z and KM68FR1000Z family are fabricated by SAMSUNG's advanced Full CMOS process technology. The family can support various operating temperature ranges and has very small size with 0.75 ball pitch and 6 x 8 ball array. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

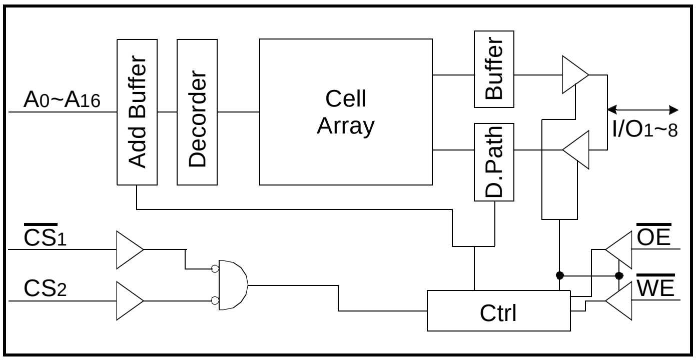
Product Family	Operating Temp.Range	Vcc Range	Speed (ns)	Power Dissipation		PKG Type
				Standby (ISB1)	Operating (ICC2)	
KM68FS1000Z	Commercial (0~70°C)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	10µA (Max)	55mA(Max) 30mA(Max)	48-CSP (6x8 ball area with 0.75mm ball pitch)
KM68FR1000Z		1.8~2.7V	300*@Vcc=2.0±0.2V		15mA(Max)	
KM68FS1000ZI	Industrial (-40~85°C)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	10µA (Max)	55mA(Max) 30mA(Max)	
KM68FR1000ZI		1.8~2.7V	300*@Vcc=2.0±0.2V		15mA(Max)	

48-CSP PIN TOP VIEW

	1	2	3	4	5	6
A	A0	A1	CS2	A3	A6	A8
B	I/O5	A2	$\overline{\text{WE}}$	A4	A7	I/O1
C	I/O6		NC	A5		I/O2
D	Vss					Vcc
E	Vcc					Vss
F	I/O7		NC	NC		I/O3
G	I/O8	$\overline{\text{OE}}$	$\overline{\text{CS}}$1	A16	A15	I/O4
H	A9	A10	A11	A12	A13	A14

* See last page for package dimension.

FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
A0~A16	Address Inputs	Vcc	Power
$\overline{\text{WE}}$	Write Enable Input	Vss	Ground
$\overline{\text{CS}}$1,CS2	Chip Select Input	I/O1~I/O8	Data Inputs/Outputs
$\overline{\text{OE}}$	Output Enable	N.C.	No Connection

SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70°C)		Industrial Temp Product (-40~85°C)	
Part Name	**Function**	**Part Name**	**Function**
KM68FS1000Z-15	48-CSP, 2.5V/3.0V, 150/100ns	KM68FS1000Z-15	48-CSP, 2.5V/3.0V, 150/100ns
KM68FR1000Z-30	48-CSP, 1.8V/2.5V, 300ns	KM68FR1000Z-30	48-CSP, 1.8V/2.5V, 300ns

* The meaning of 2.5V/3.0V, 150/100ns is that the operating V_{CC} is ranged from 2.3V(Min) to 3.3V(Max) with speed 150ns @2.5V±0.2 and 100ns @3.0V±0.3. This type of meaning is applied to other notations like the example.

** But in case of KM68FR1000Z-30, there is only one speed bin, 300ns though it supports wide range operating V_{CC}.

ORDERING INFORMATION

KM6 8 X X 1000 X X X - X X

Blank : Low Low Power
Access Time : 7=70ns, 8=85ns, 10=100ns, 12=120ns, 15=150ns, 30=300ns
Operating Temperature : Blank=Commercial, E=Extended, I=Industrial
Package Type : G=SOP, T=TSOP Forward, R=TSOP Reverse Z=48-CSP with 0.75mm pitch
Die Version : Blank=1′st generation
Density : 1000=1Mbit
S=2.3~3.3V, R=1.8~2.7V
Process Technology : F-Full CMOS(6-Tr Cell)
Organization : 8= x8
SEC Standard SRAM

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.2 to 3.6V	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0V	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-55 to 150	°C	-
Operating Temperature	T_A	0 to 70	°C	KM68FS1000Z KM68FR1000Z
		-40 to 85	°C	KM68FS1000ZI KM68FR1000ZI
Soldering temperature and time	T_{SOLDER}	260°C, 5sec(Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product		Min	Typ**	Max	Unit
Supply voltage	Vcc	KM68FS1000Z Family		2.3	2.5/3.0	3.3	V
		KM68FR1000Z Family		1.8	2.0/2.5	2.7	V
Ground	Vss	All Family		0	0	0	V
Input high voltage	V_{IH}	KM68FS1000Z Family	Vcc=3.0¡¾0.2V	2.2	-	Vcc+0.2	V
			Vcc=2.5¡¾0.2V	2.0	-	Vcc+0.2	V
		KM68FR1000Z Family	Vcc=2.5¡¾0.2V	2.0	-	Vcc+0.2	V
			Vcc=2.0¡¾0.2V	1.6	-	Vcc+0.2	V
Input low voltage	V_{IL}	All Family		-0.2***	-	0.4	V

* 1) Commercial Product : T_A=0 to 70°C, unless otherwise specified
2) Industrial Product : T_A=-40 to 85°C, unless otherwise specified

** T_A=25°C

*** V_{IL}(Min)=-1.5V for≤30ns pulse width

CAPACITANCE* (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

* Capacitance is sampled not, 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions$^{1)}$			Min	Typ**	Max	Unit
Input leakage current	ILI	VIN=Vss to Vcc			-1	-	1	µA
Output leakage current	ILO	$\overline{\text{CS}}$1=VIH or CS2=VIL or WE=VIL, VIO=Vss to Vcc			-1	-	1	µA
Operating power supply current	ICC	$\overline{\text{CS}}$1=VIL, CS2=VIH VIN=VIH or VIL, IIO=0mA		Read	-	-	$5^{5)}$	mA
				Write	-	-	$15^{5)}$	
Average operating current	ICC1	Cycle time=1§Á100% duty, $\overline{\text{CS}}$1≤0.2V, CS2≥VIN≥VCC-0.2V		Read	-	-	$5^{5)}$	mA
				Write	-	-	$15^{5)}$	
	ICC2	Min cycle, 100% duty, IIO=0mA, $\overline{\text{CS}}$1=VIL, or CS2=VIH	Vcc=3.3V@100ns		-	-	$55^{4)}$	mA
			Vcc=2.7V@150ns		-	-	30	
			Vcc=2.2V@300ns		-	-	15	
Output low voltage	VOL	IOL	Vcc=3.0V	2.1mA	-	-	0.4	V
			Vcc=2.5V	0.5mA	-	-	0.4	
			Vcc=2.0V	0.33mA	-	-	0.4	
Output high voltage	VOH	IOH	Vcc=3.0V	-1.0mA	2.4	-	-	V
			Vcc=2.5V	-0.5mA	2.0	-	-	
			Vcc=2.0V	-0.44mA	1.6	-	-	
Standby Current(TTL)	ISB	$\overline{\text{CS}}$1=VIH, or CS2=VIL			-	-	0.3	mA
Standby Current (CMOS) KM68FS1000Z KM68FR1000Z	ISB1	$\overline{\text{CS}}$1≥Vcc-0.2V CS2≥Vcc-0.2V or CS2≤0.2V, Other input =0~Vcc	Low Low Power		-	0.05	$5^{2)}$	µA
KM68FS1000ZI KM68FR1000ZI			Low Low Power		-	0.05	$5^{2)}$	µA

1) - Commercial Product
TA=0 to 70°C, Vcc=2.3V(Min) ~ 3.3V(Max) for 68FS1000Z Family, Vcc=1.8V(Min) ~ 2.7V(Max)V for 68FR1000Z Family
- Industrial Product
TA=-40 to 85°C, Vcc=2.3V(Min) ~ 3.3V(Max) for 68FS1000ZI Family, Vcc=1.8V(Min)~2.7V(Max) for 68FR1000ZI Family.

2) The value has difference by ±1µA.
Measured at Vcc=3.3V(Max)

3) The value is not 100% tested but obtained statistically at Temp=25°C

4) - The value is measured at Vcc=3.0V±0.3V
- ICC2=30mA with 120ns cycle at Vcc=2.5V±0.2V, but this value is not 100% tested but obtained statistically.
- ICC2=15mA with 300ns cycle at Vcc=2.0V±0.2V, but this value is not 100% tested but obtained statistically.

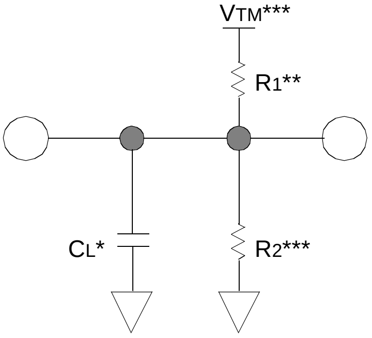
5) The value is measured at Vcc=3.0V±0.3V

AC OPERATING CONDITIONS

TEST CONDITIONS(1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	V_{CC}=3.0V, 2.5V
	0.4 to 1.8V	V_{CC}=2.0V
Input rising and falling time	5ns	-
input and output reference voltage	1.5V	V_{CC}=3.0V
	1.1V	V_{CC}=2.5V
	0.9V	V_{CC}=2.0V,
Output load (See right)	C_L=100pF	See Test Condition #2
	C_L=30pF	

* See test condition of DC and Operating characteristics



* Including scope and jig capacitance
**R_1=3070Ω, R_2=3150Ω
***V_{TM}=2.8V for Vcc = 3.0V/3.3V
2.3V for Vcc = 2.5V
1.8V for Vcc = 2.0V

TEST CONDITIONS(2. Temperature and Vcc Conditions)

Product Family	Temperature	Vcc Range	Typical Supply Vcc	Speed	Comments
KM68FR1000Z	0~70°C	1.8(Min)~2.7(Max)	2.0V±0.2 Operation	300*ns	Commercial
KM68FS1000Z	0~70°C	2.3(Min)~3.3(Max)	2.5V±0.2 Operation	150*ns	
			3.0V±0.3 Operation	100*ns	
KM68FR1000ZI	-40~85°C	1.8(Min)~2.7(Max)	2.0V±0.2 Operation	300*ns	Industrial
KM68FS1000ZI	-40~85°C	2.3(Min)~3.3(Max)	2.5V±0.2 Operation	150*ns	
			3.0V±0.3 Operation	100*ns	

* All the parameters are measured with 30pF test load

AC CHARACTERISTICS

Parameter List		Symbol	Speed Bins						Units
			100ns		150ns		300ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t_{RC}	100	-	150	-	300	-	ns
	Address access time	t_{AA}	-	100	-	150	-	300	ns
	Chip select to output	t_{CO1}	-	100	-	150	-	300	ns
	Output enable to valid output	t_{OE}	-	50	-	75	-	150	ns
	Chip select to low-Z output	t_{LZ1},t_{LZ2}	10	-	20	-	50	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	20	-	30	-	ns
	Chip disable to high-Z output	t_{HZ1},t_{HZ2}	0	30	0	40	0	60	ns
	Output disable to high-Z output	t_{OHZ}	0	30	0	40	0	60	ns
	Output hold from address change	t_{OH}	15	-	15	-	30	-	ns
Write	Write cycle time	t_{WC}	100	-	150	-	300	-	ns
	Chip select to end of write	t_{CW}	80	-	120	-	300	-	ns
	Address set-up time	t_{AS}	0	-	0	-	0	-	ns
	Address valid to end of write	t_{AW}	80	-	120	-	300	-	ns
	Write pulse width	t_{WP}	70	-	100	-	200	-	ns
	Write recovery	t_{WR}	0	-	0	-	0	-	ns
	Write to output high-Z	t_{WHZ}	0	30	0	40	0	60	ns
	Data to write time overlap	t_{DW}	40	-	60	-	120	-	ns
	Data hold from write time	t_{DH}	0	-	0	-	0	-	ns
	End write to output low-Z	t_{OW}	5	-	5	-	20	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}	$\overline{\text{CS}}_1$***≥Vcc-0.2V		1.5	-	3.6	V
Data retention current	I_{DR}	Vcc=3.0V $\overline{\text{CS}}_1$≥Vcc-0.2V	Low Low Power	-	0.05	5	µA
Data retention set-up time	t_{SDR}	See data retention waveform		0	-	-	ns
Recovery time	t_{RDR}			t_{RC}	-	-	

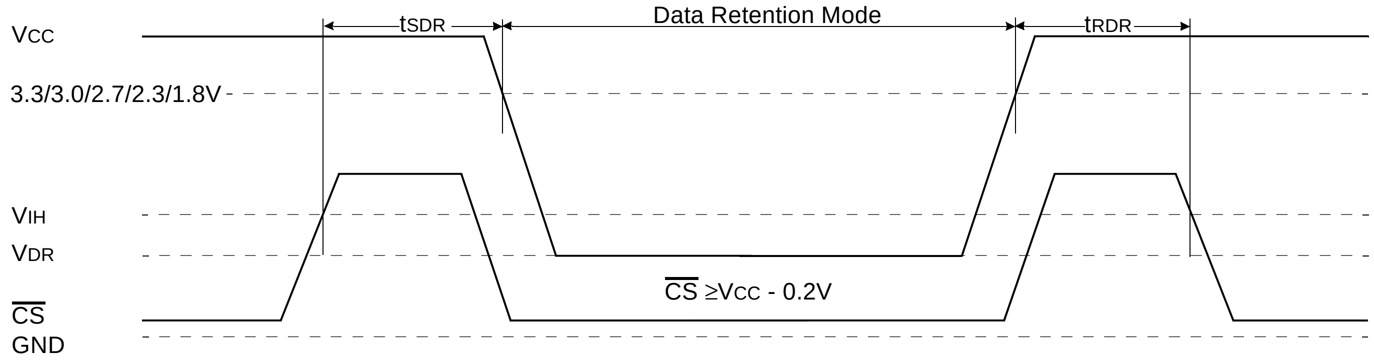
* 1) Commercial Product : T_A=0 to 70°C, unless otherwise specified
2) Industrial Product : T_A=-40 to 85°C, unless otherwise specified

** T_A=25°C, the value is too small to detect by test machine, 0.01µA statistically

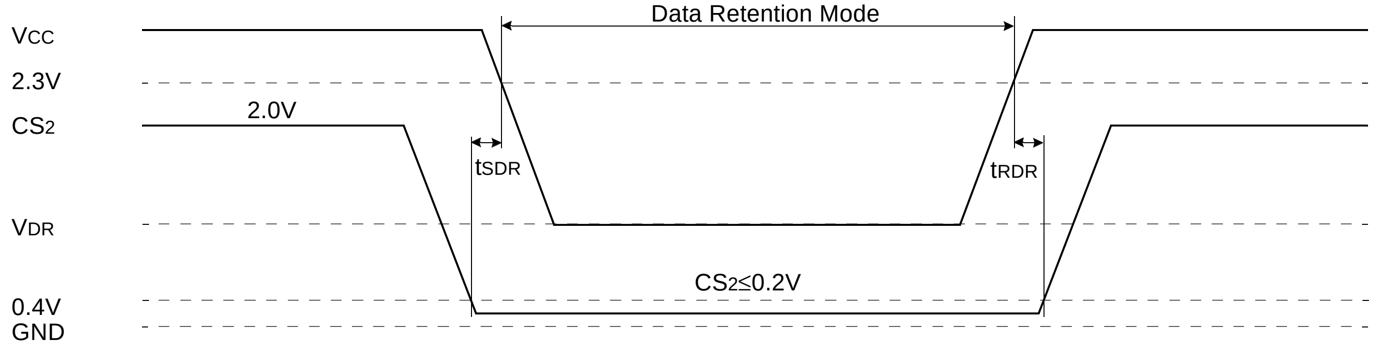
*** $\overline{\text{CS}}_1$≥Vcc-2.0V, CS_2≥Vcc-2.0V($\overline{\text{CS}}_1$ controlled) or CS_2≤2.0V(CS_2 controlled)

DATA RETENTION TIMING DIAGRAM

1) $\overline{\text{CS}}_1$ controlled



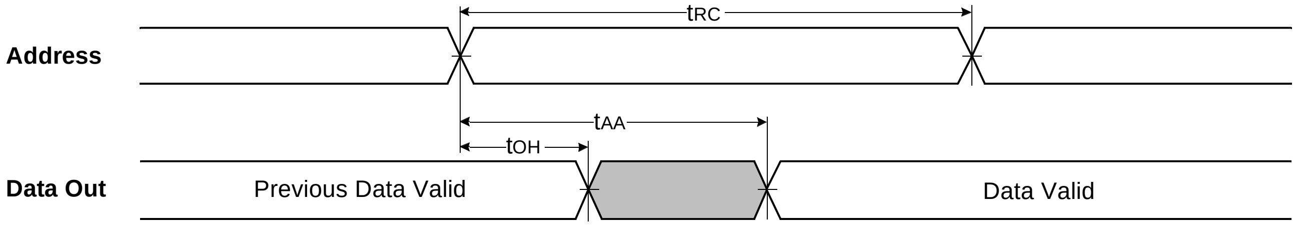
2) CS_2 controlled



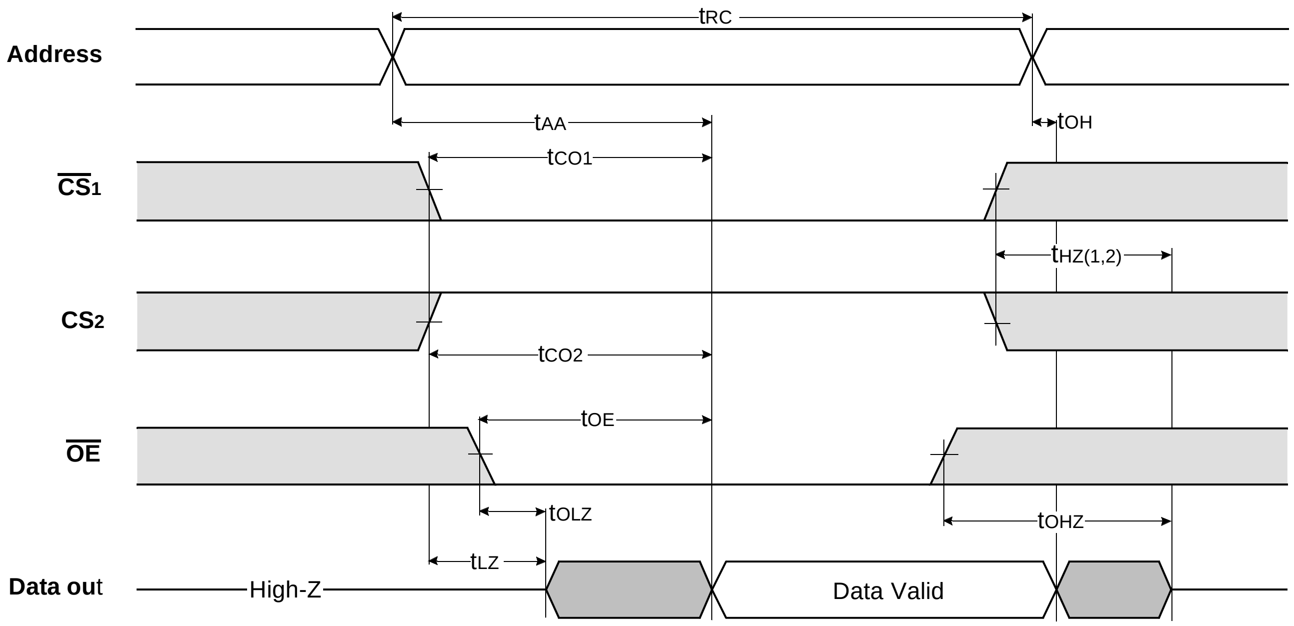
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1)(Address Controlled)

($\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, $\overline{UB}$ or, and $\overline{LB}=V_{IL}$)



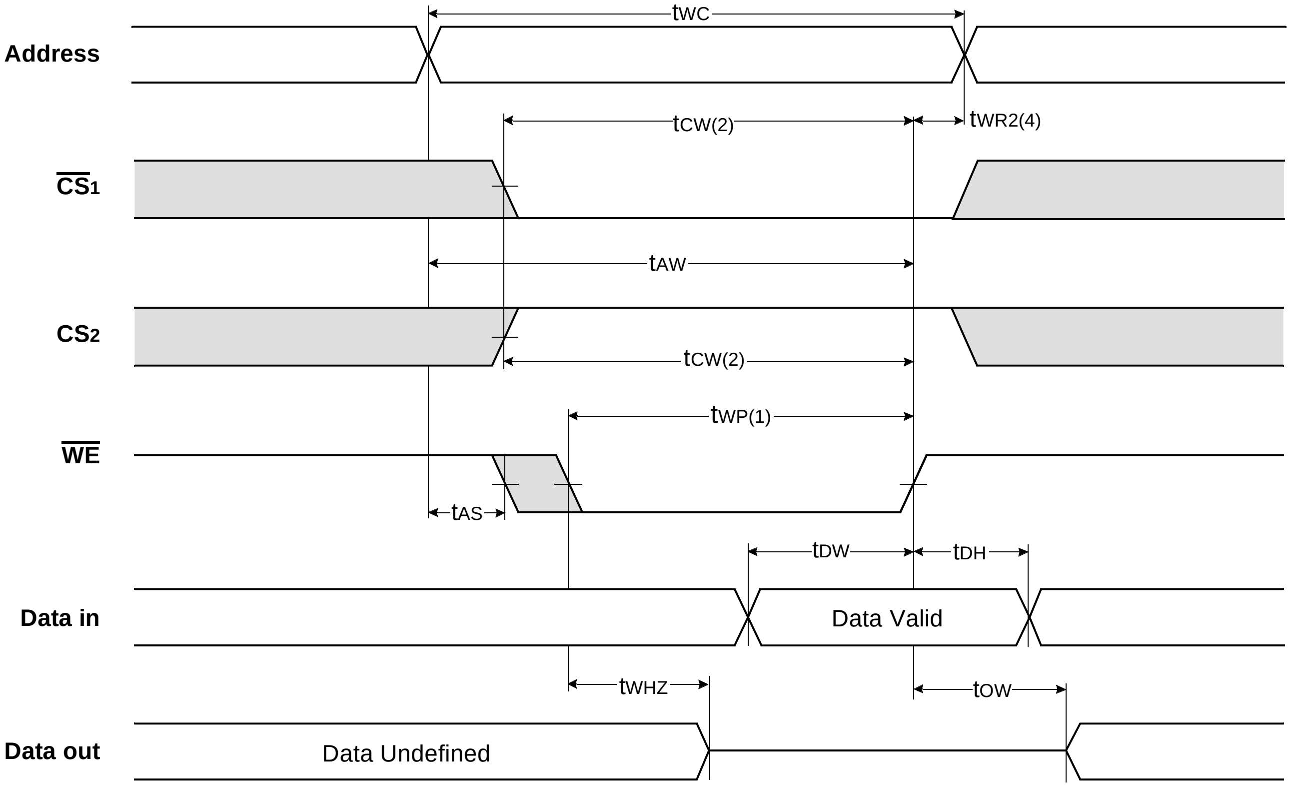
TIMING WAVEFORM OF READ CYCLE(2)($\overline{WE}=V_{IH}$)



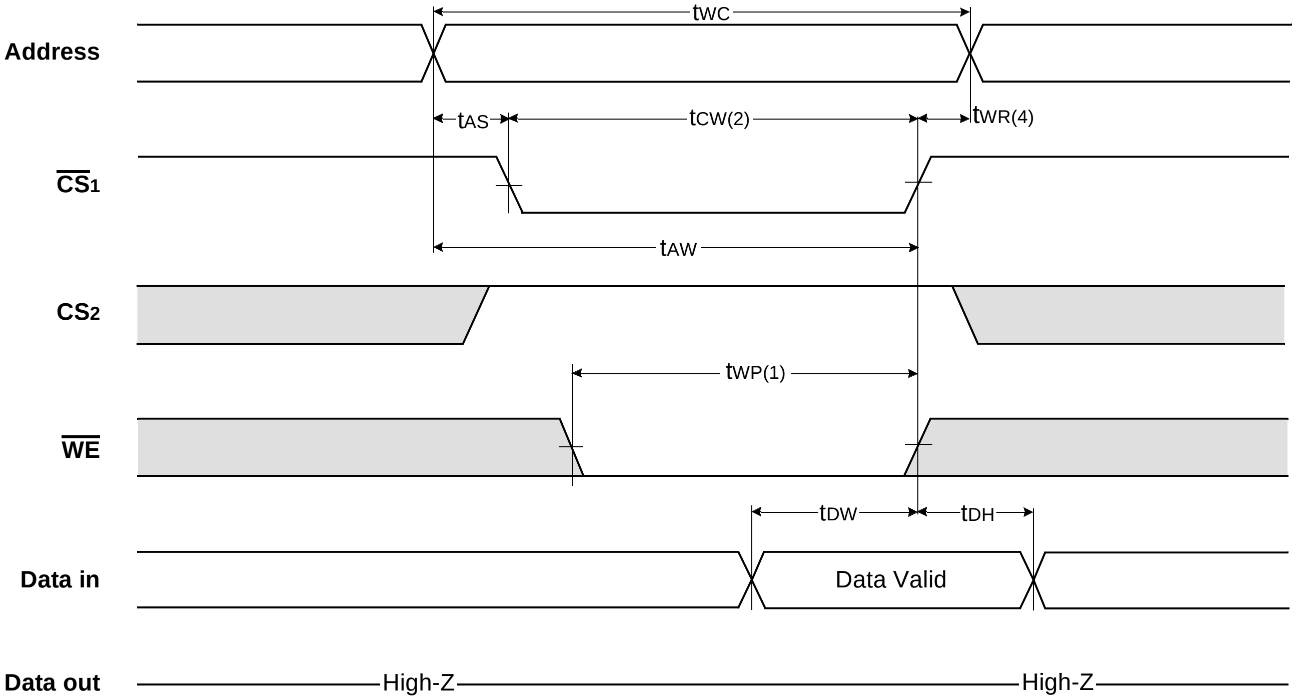
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

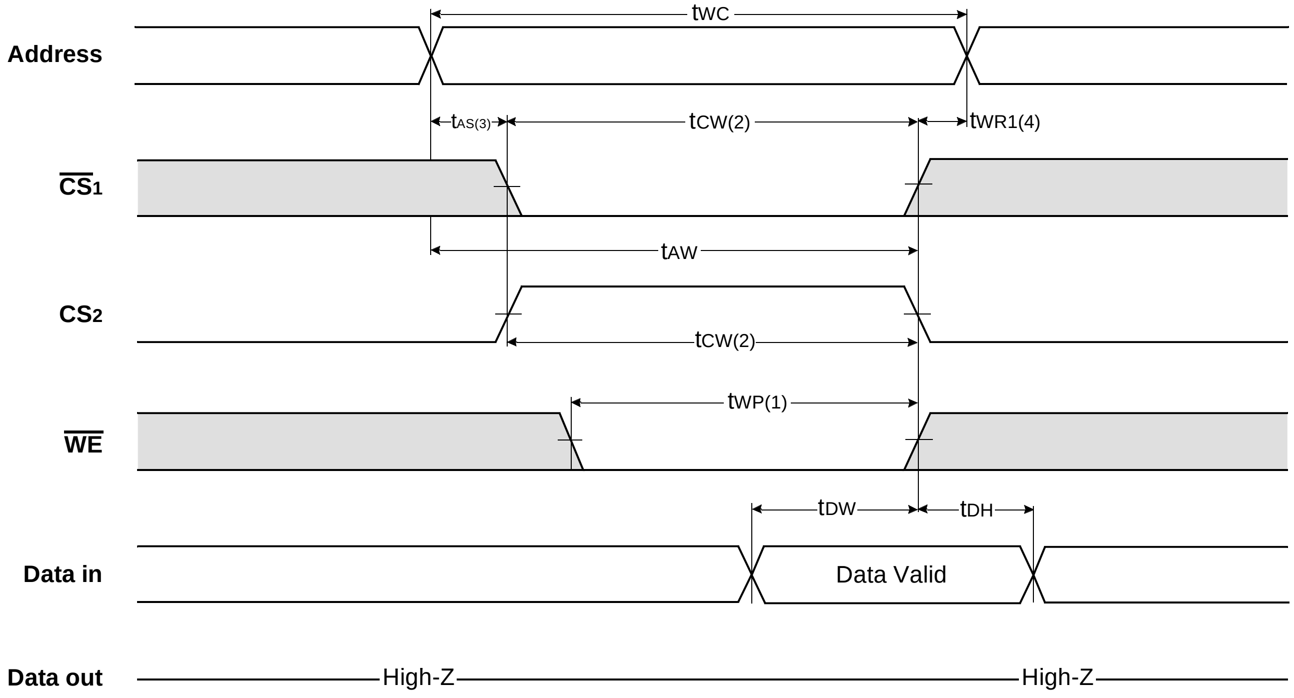
TIMING WAVEFORM OF WRITE CYCLE(1)(WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2)(CS1 Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



NOTES (WRITE CYCLE)

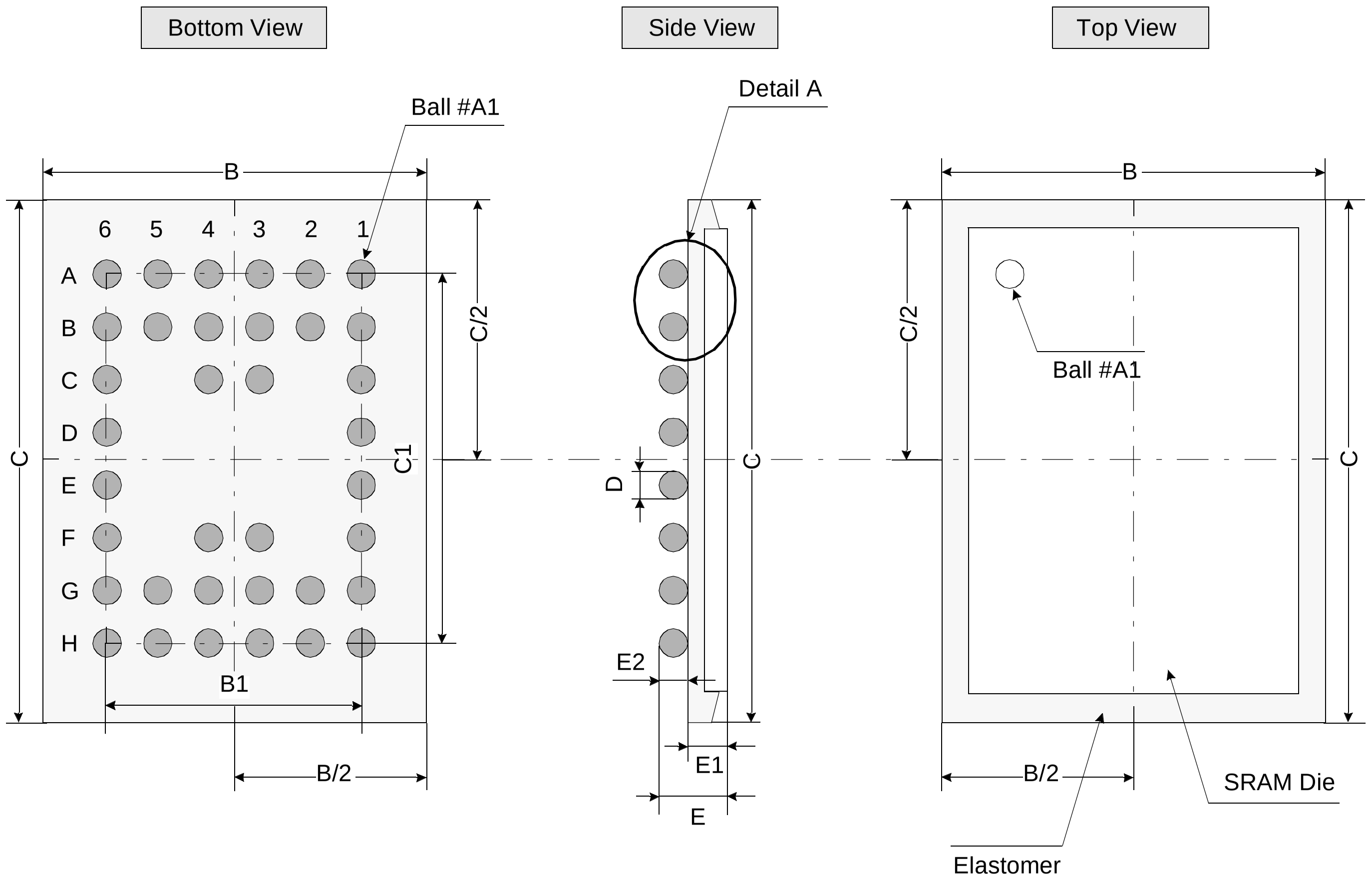
1. A write occurs during the overlap of a low $\overline{\text{CS}}_1$ and a high CS_2 low $\overline{\text{WE}}$. A write begins at the latest transition among $\overline{\text{CS}}_1$ going low CS_2 going high and $\overline{\text{WE}}$ goes low. A write ends at the earliest transition among $\overline{\text{CS}}1$ going high ,CS_2 going low and $\overline{\text{WE}}$ going high tWP is measured from the beginning of write to the end write.
2. t_{CW} is measured from the later of $\overline{\text{CS}}_1$ going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR1} applied in case a write ends at $\overline{\text{CS}}_1$ or $\overline{\text{WE}}$ going high, t_{WR2} applied in case a write ends at CS_2 going to low.

FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}_1$	CS_2	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Mode	$I/O_{1\sim8}$	Current Mode
H	X*	X	X	Power Down	High-Z	I_{SB}
X	L	X	X	Power Down	High-Z	I_{SB},I_{SB1}
L	H	H	H	Output Disable	High-Z	Icc
L	H	H	L	Read	Dout	Icc
L	H	L	X	Write	Din	Icc

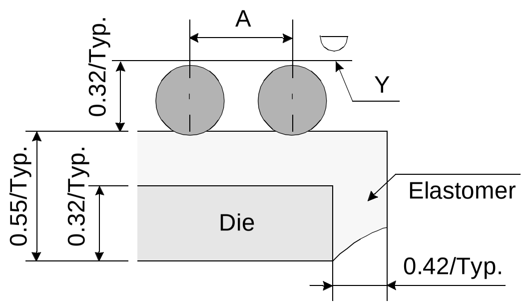
* X means do care (high or low)

PACKAGE DIMENSIONS (Units : mm)



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	0.80	0.81
E1	-	0.55	-
E2	-	0.25	-
Y	-	-	0.08

Detail A



Notes.

1. Bump counts : 48(8row x 6row)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are +/-0.050 unless
   otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)