Preliminary
GS8150Z18/36T-225/200/180/166/150/133

100-Pin TQFP
Commercial Temp
Industrial Temp

16Mb Pipelined and Flow Through Synchronous NBT SRAM

225 MHz–133 MHz
3.3 V V_{DD}
2.5 V or 3.3 V I/O

Features

- User-configurable Pipeline and Flow Through mode
- NBT (No Bus Turn Around) functionality allows zero wait read-write-read bus utilization; Fully pin-compatible with both pipelined and flow through NtRAM™, NoBL™ and ZBT™ SRAMs
- 3.3 V +10%/–5% core power supply
- 2.5 V or 3.3 V I/O supply
- $\overline{\text{LBO}}$ pin for Linear or Interleave Burst mode
- Pin compatible with 2M, 4M, and 8M devices
- Byte write operation (9-bit Bytes)
- 3 chip enable signals for easy depth expansion
- ZZ Pin for automatic power-down
- JEDEC-standard 100-lead TQFP package

		-225	-200	-180	-166	-150	-133	Unit
Pipeline 3-1-1-1	t_{KQ}	2.5	3.0	3.2	3.5	3.8	4.0	ns
	tCycle	4.4	5.0	5.5	6.0	6.6	7.5	ns
	Curr (x18)	350	315	290	270	250	230	mA
	Curr (x36)	410	370	340	315	290	260	mA
Flow Through 2-1-1-1	t_{KQ}	7.0	7.5	8	8.5	10	11	ns
	tCycle	8.5	10	10	10	10	15	ns
	Curr (x18)	205	185	185	185	185	140	mA
	Curr (x36)	240	210	210	210	210	160	mA

Functional Description

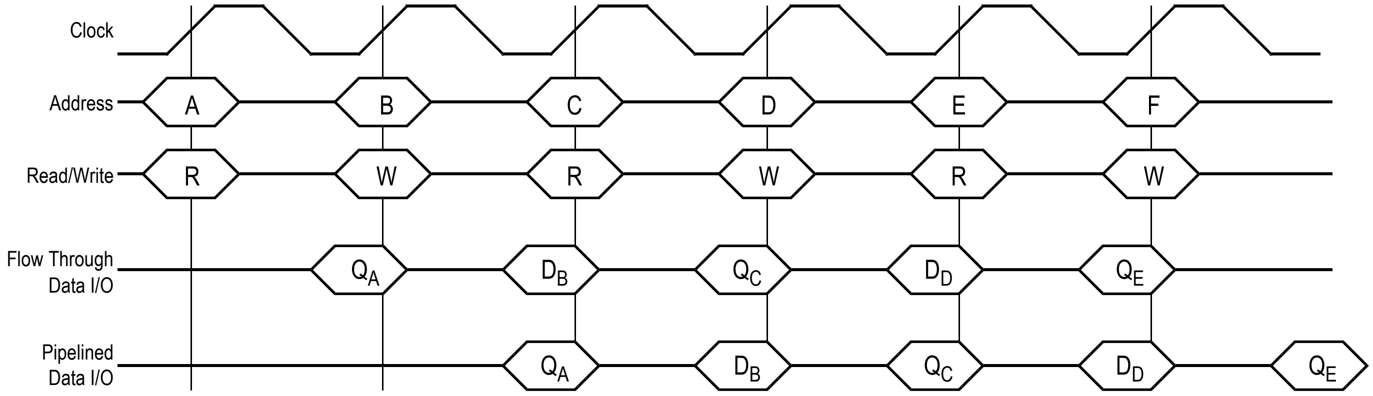
The GS8150Z18/36T is a 16Mbit Synchronous Static SRAM. GSI's NBT SRAMs, like ZBT, NtRAM, NoBL or other pipelined read/double late write or flow through read/single late write SRAMs, allow utilization of all available bus bandwidth by eliminating the need to insert deselect cycles when the device is switched from read to write cycles.

Because it is a synchronous device, address, data inputs, and read/ write control inputs are captured on the rising edge of the input clock. Burst order control ($\overline{\text{LBO}}$) must be tied to a power rail for proper operation. Asynchronous inputs include the Sleep mode enable (ZZ) and Output Enable. Output Enable can be used to override the synchronous control of the output drivers and turn the RAM's output drivers off at any time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation required by asynchronous SRAMs and simplifies input signal timing.

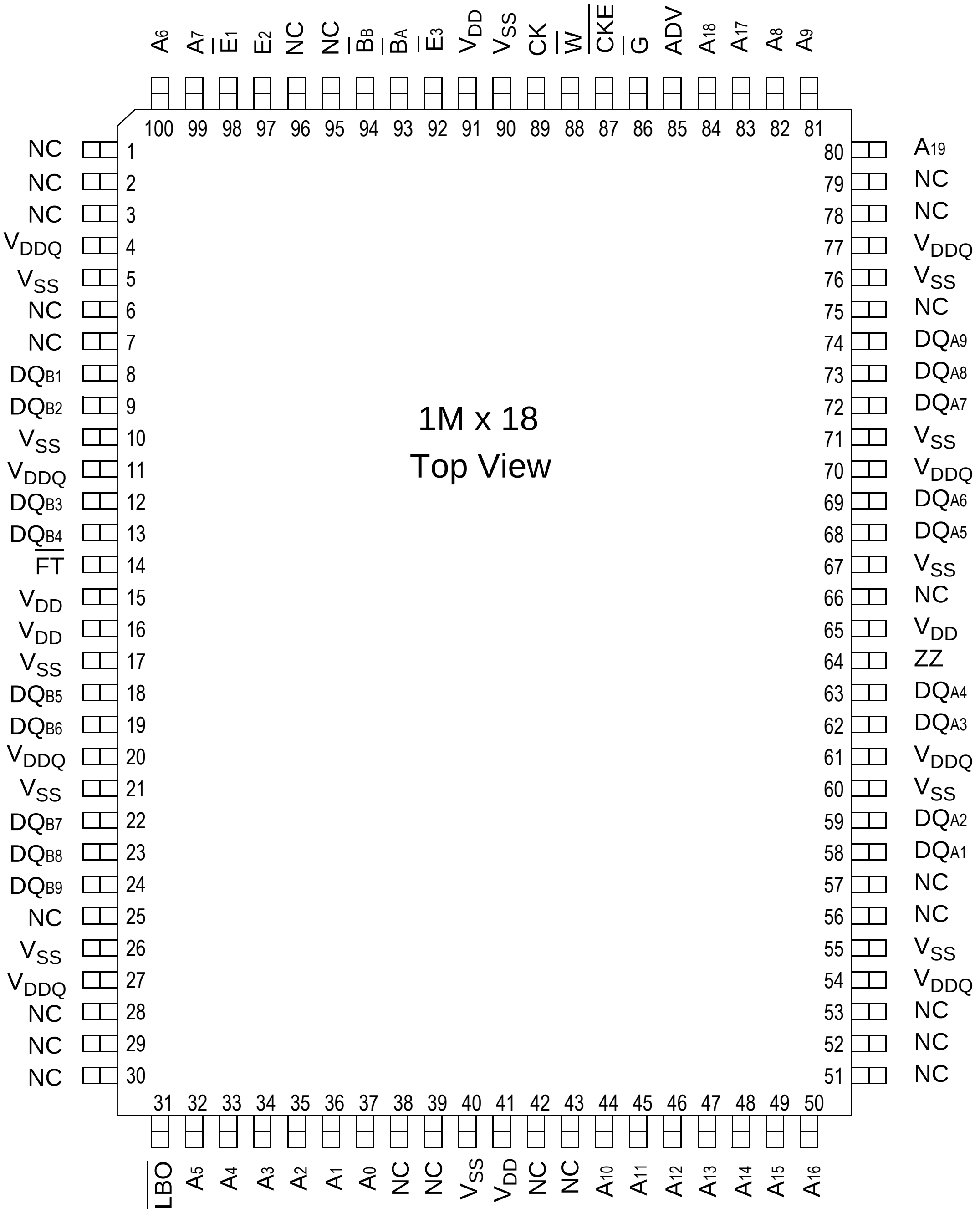
The GS8150Z18/36T may be configured by the user to operate in Pipeline or Flow Through mode. Operating as a pipelined synchronous device, meaning that in addition to the rising edge triggered registers that capture input signals, the device incorporates a rising-edge-triggered output register. For read cycles, pipelined SRAM output data is temporarily stored by the edge triggered output register during the access cycle and then released to the output drivers at the next rising edge of clock.

The GS8150Z18/36T is implemented with GSI's high performance CMOS technology and is available in a JEDEC-Standard 100-pin TQFP package.

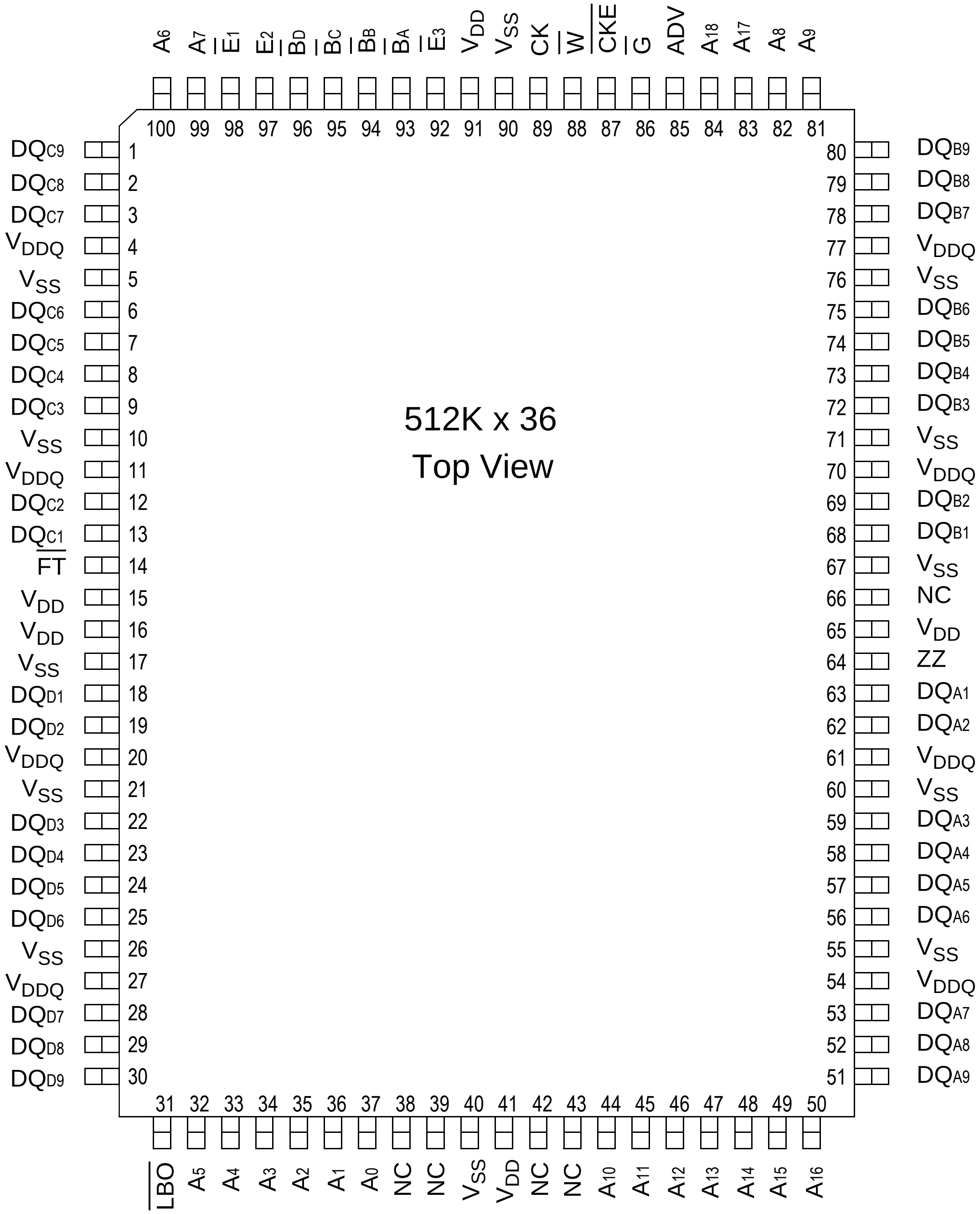
Flow Through and Pipelined NBT SRAM Back-to-Back Read/Write Cycles



GS8150Z18T Pinout



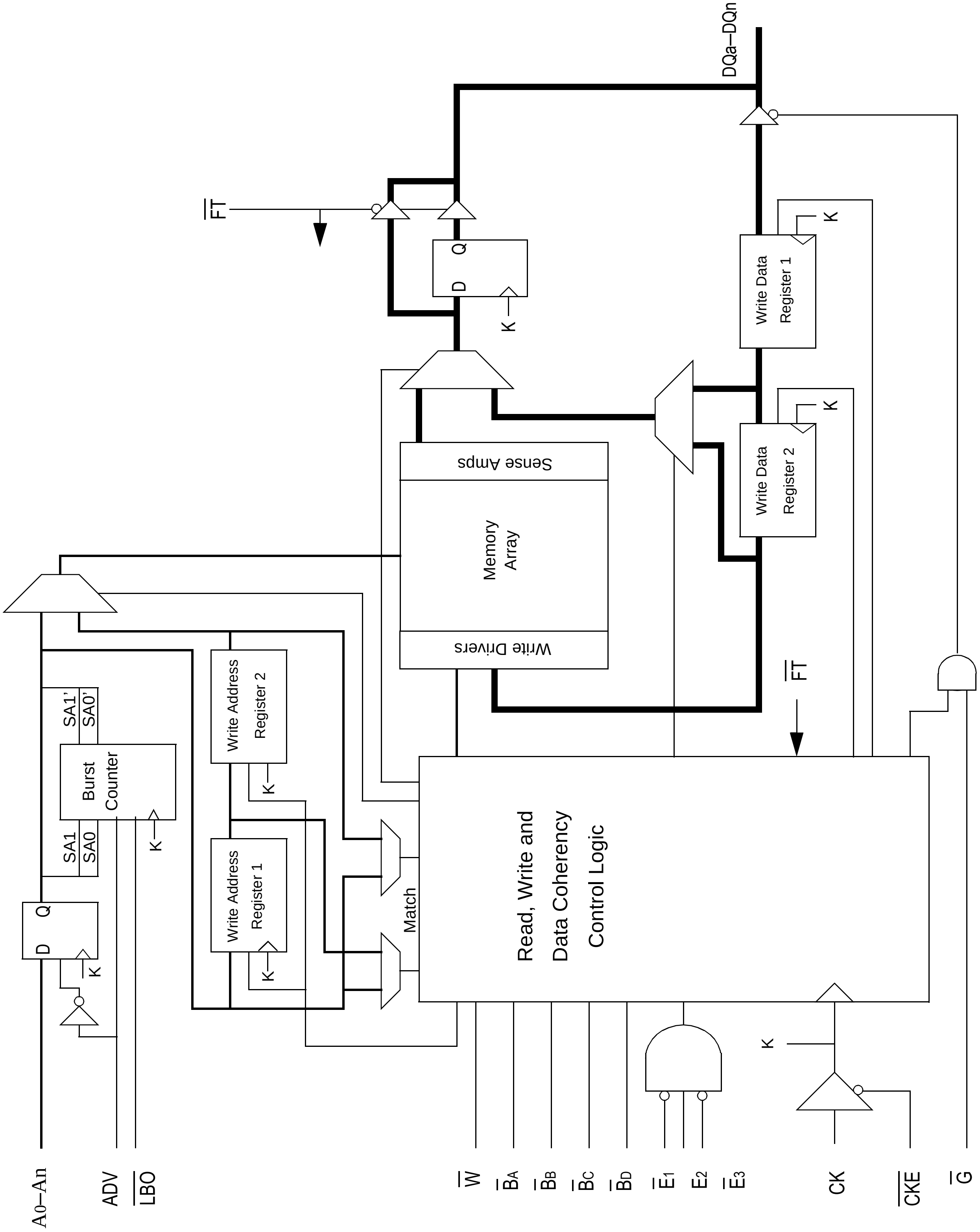
GS8150Z36T Pinout



100-Pin TQFP Pin Descriptions

Pin Location	Symbol	Type	Description
37, 36	A_0, A_1	In	Burst Address Inputs; Preload the burst counter
35, 34, 33, 32, 100, 99, 84, 83, 82, 81, 44, 45, 46,47, 48, 49, 50	A_2–A_{18}	In	Address Inputs
80	A_{19}	In	Address Input (x18 Version Only)
89	CK	In	Clock Input Signal
93	$\overline{B}_A$	In	Byte Write signal for data inputs DQ_{A1}-DQ_{A9}; active low
94	$\overline{B}_B$	In	Byte Write signal for data inputs DQ_{B1}-DQ_{B9}; active low
95	$\overline{B}_C$	In	Byte Write signal for data inputs DQ_{C1}-DQ_{C9}; active low (x36 Versions Only)
96	$\overline{B}_D$	In	Byte Write signal for data inputs DQ_{D1}-DQ_{D9}; active low (x36 Versions Only)
88	$\overline{W}$	In	Write Enable; active low
98	$\overline{E}_1$	In	Chip Enable; active low
97	E_2	In	Chip Enable; Active High. For self decoded depth expansion
92	$\overline{E}_3$	In	Chip Enable; Active Low. For self decoded depth expansion
86	$\overline{G}$	In	Output Enable; active low
85	ADV	In	Advance/$\overline{\text{Load}}$; Burst address counter control pin
87	$\overline{\text{CKE}}$	In	Clock Input Buffer Enable; active low
58, 59, 62,63, 68, 69, 72, 73, 74	DQ_{A1}–DQ_{A9}	I/O	Byte A Data Input and Output pins (x18 Version Only)
8, 9, 12, 13, 18, 19, 22, 23, 24	DQ_{B1}–DQ_{B9}	I/O	Byte B Data Input and Output pins (x18 Version Only)
51, 52, 53, 56, 57, 75, 78, 79, 1, 2, 3, 6, 7, 25, 28, 29, 30	NC	—	No Connect (x18 Version Only)
51, 52, 53, 56, 57, 58, 59, 62,63	DQ_{A1}–DQ_{A9}	I/O	Byte A Data Input and Output pins (x36 Versions Only)
68, 69, 72, 73, 74, 75, 78, 79, 80	DQ_{B1}–DQ_{B9}	I/O	Byte B Data Input and Output pins (x36 Versions Only)
1, 2, 3, 6, 7, 8, 9, 12, 13	DQ_{C1}–DQ_{C9}	I/O	Byte C Data Input and Output pins (x36 Versions Only)
18, 19, 22, 23, 24, 25, 28, 29, 30	DQ_{D1}–DQ_{D9}	I/O	Byte D Data Input and Output pins (x36 Versions Only)
64	ZZ	In	Power down control; active high
14	$\overline{\text{FT}}$	In	Pipeline/Flow Through Mode Control; active low
31	$\overline{\text{LBO}}$	In	Linear Burst Order; active low
15, 16, 41, 65, 91	V_{DD}	In	3.3 V power supply
5,10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	In	Ground
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	In	3.3 V output power supply for noise reduction
38, 39, 42, 43, 66	NC	—	No Connect

GS8150Z18/36 NBT SRAM Functional Block Diagram



Functional Details

Clocking

Deassertion of the Clock Enable ($\overline{\text{CKE}}$) input blocks the Clock input from reaching the RAM's internal circuits. It may be used to suspend RAM operations. Failure to observe Clock Enable set-up or hold requirements will result in erratic operation.

Pipeline Mode Read and Write Operations

All inputs (with the exception of Output Enable, Linear Burst Order and Sleep) are synchronized to rising clock edges. Single cycle read and write operations must be initiated with the Advance/Load pin (ADV) held low, in order to load the new address. Device activation is accomplished by asserting all three of the Chip Enable inputs ($\overline{E}_1$, E_2 and $\overline{E}_3$). Deassertion of any one of the Enable inputs will deactivate the device.

Function	$\overline{W}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$
Read	H	X	X	X	X
Write Byte a	L	L	H	H	H
Write Byte b	L	H	L	H	H
Write Byte c	L	H	H	L	H
Write Byte d	L	H	H	H	L
Write all Bytes	L	L	L	L	L
Write Abort/NOP	L	H	H	H	H

Read operation is initiated when the following conditions are satisfied at the rising edge of clock: $\overline{\text{CKE}}$ is asserted Low, all three chip enables ($\overline{E}_1$, E_2, and $\overline{E}_3$) are active, the write enable input signals $\overline{W}$ is deasserted high, and ADV is asserted low. The address presented to the address inputs is latched in to address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the next rising edge of clock the read data is allowed to propagate through the output register and onto the output pins.

Write operation occurs when the RAM is selected, CKE is active, and the Write input is sampled low at the rising edge of clock. The Byte Write Enable inputs ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, & $\overline{B}_D$) determine which bytes will be written. All or none may be activated. A write cycle with no Byte Write inputs active is a no-op cycle. The pipelined NBT SRAM provides double late write functionality, matching the write command versus data pipeline length (2 cycles) to the read command versus data pipeline length (2 cycles). At the first rising edge of clock, Enable, Write, Byte Write(s), and Address are registered. The Data In associated with that address is required at the third rising edge of clock.

Flow Through Mode Read and Write Operations

Operation of the RAM in Flow Through mode is very similar to operations in Pipeline mode. Activation of a Read Cycle and the use of the Burst Address Counter is identical. In Flow Through mode the device may begin driving out new data immediately after new address are clocked into the RAM, rather than holding new data until the following (second) clock edge. Therefore, in Flow Through mode the read pipeline is one cycle shorter than in Pipeline mode.

Write operations are initiated in the same way, but differ in that the write pipeline is one cycle shorter as well, preserving the ability to turn the bus from reads to writes without inserting any dead cycles. While the pipelined NBT RAMs implement a double late write protocol, in Flow Through mode a single late write protocol mode is observed. Therefore, in Flow Through mode, address and control are registered on the first rising edge of clock and data in is required at the data input pins at the second rising edge of clock.

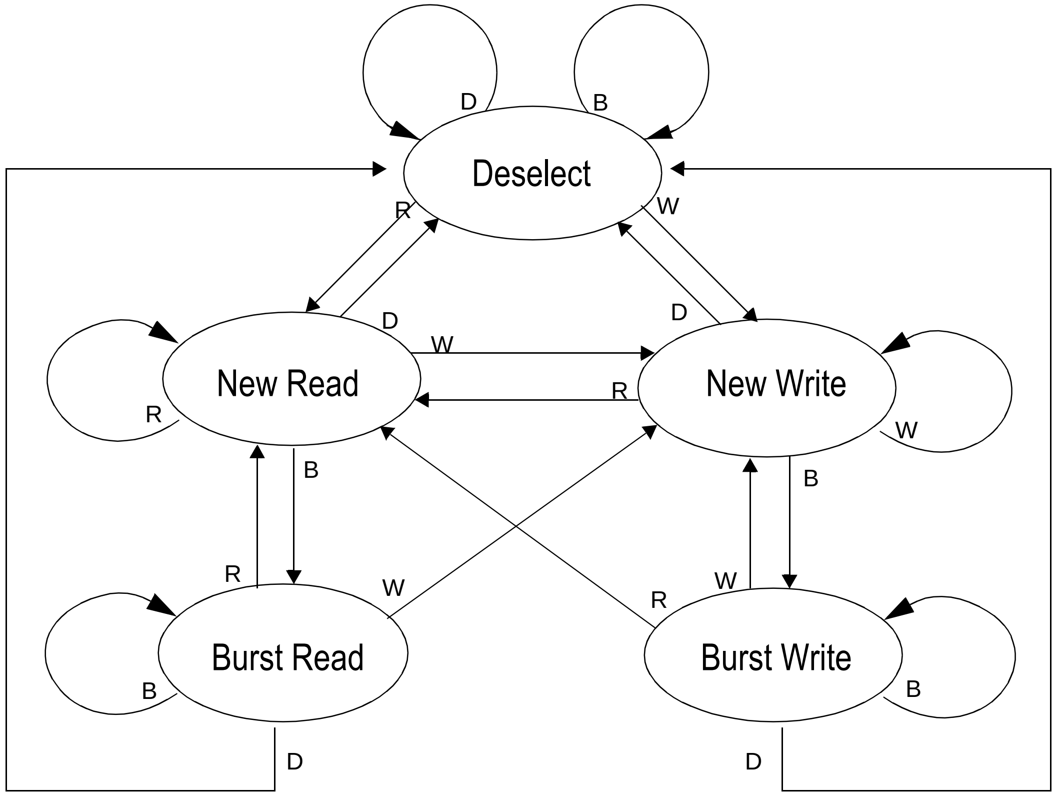
Synchronous Truth Table

Operation	Type	Address	$\overline{E}_1$	E_2	$\overline{E}_3$	ZZ	ADV	$\overline{W}$	$\overline{Bx}$	$\overline{G}$	$\overline{CKE}$	CK	DQ	Notes
Deselect Cycle, Power Down	D	None	H	X	X	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Power Down	D	None	X	X	H	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Power Down	D	None	X	L	X	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Continue	D	None	X	X	X	L	H	X	X	X	L	L-H	High-Z	1
Read Cycle, Begin Burst	R	External	L	H	L	L	L	H	X	L	L	L-H	Q	
Read Cycle, Continue Burst	B	Next	X	X	X	L	H	X	X	L	L	L-H	Q	1,10
NOP/Read, Begin Burst	R	External	L	H	L	L	L	H	X	H	L	L-H	High-Z	2
Dummy Read, Continue Burst	B	Next	X	X	X	L	H	X	X	H	L	L-H	High-Z	1,2,10
Write Cycle, Begin Burst	W	External	L	H	L	L	L	L	L	X	L	L-H	D	3
Write Cycle, Continue Burst	B	Next	X	X	X	L	H	X	L	X	L	L-H	D	1,3,10
NOP/Write Abort, Begin Burst	W	None	L	H	L	L	L	L	H	X	L	L-H	High-Z	2,3
Write Abort, Continue Burst	B	Next	X	X	X	L	H	X	H	X	L	L-H	High-Z	1,2,3,10
Clock Edge Ignore, Stall		Current	X	X	X	L	X	X	X	X	H	L-H	-	4
Sleep Mode		None	X	X	X	H	X	X	X	X	X	X	High-Z	

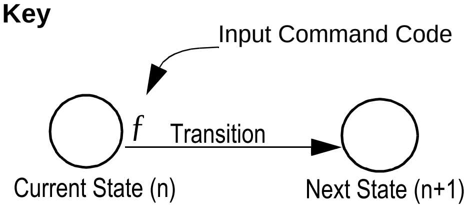
Notes:

1. Continue Burst cycles, whether read or write, use the same control inputs. A Deselect continue cycle can only be entered into if a Deselect cycle is executed first.
2. Dummy Read and Write abort can be considered NOPs because the SRAM performs no operation. A Write abort occurs when the $\overline{W}$ pin is sampled low but no Byte Write pins are active so no write operation is performed.
3. $\overline{G}$ can be wired low to minimize the number of control signals provided to the SRAM. Output drivers will automatically turn off during write cycles.
4. If $\overline{CKE}$ High occurs during a pipelined read cycle, the DQ bus will remain active (Low Z). If $\overline{CKE}$ High occurs during a write cycle, the bus will remain in High Z.
5. X = Don t Care; H = Logic High; L = Logic Low; $\overline{Bx}$ = High = All Byte Write signals are high; $\overline{Bx}$ = Low = One or more Byte/Write signals are Low
6. All inputs, except $\overline{G}$ and ZZ must meet setup and hold times of rising clock edge.
7. Wait states can be inserted by setting $\overline{CKE}$ high.
8. This device contains circuitry that ensures all outputs are in High Z during power-up.
9. A 2-bit burst counter is incorporated.
10. The address counter is incriminated for all Burst continue cycles.

Pipeline and Flow Through Read Write Control State Diagram

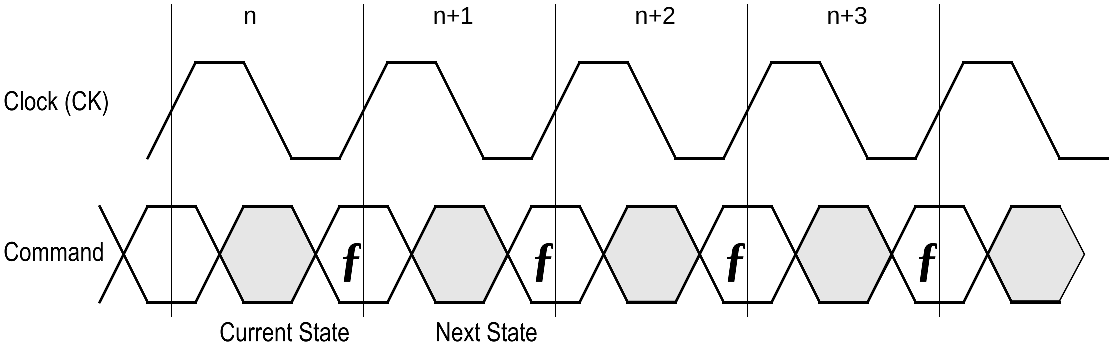


Key



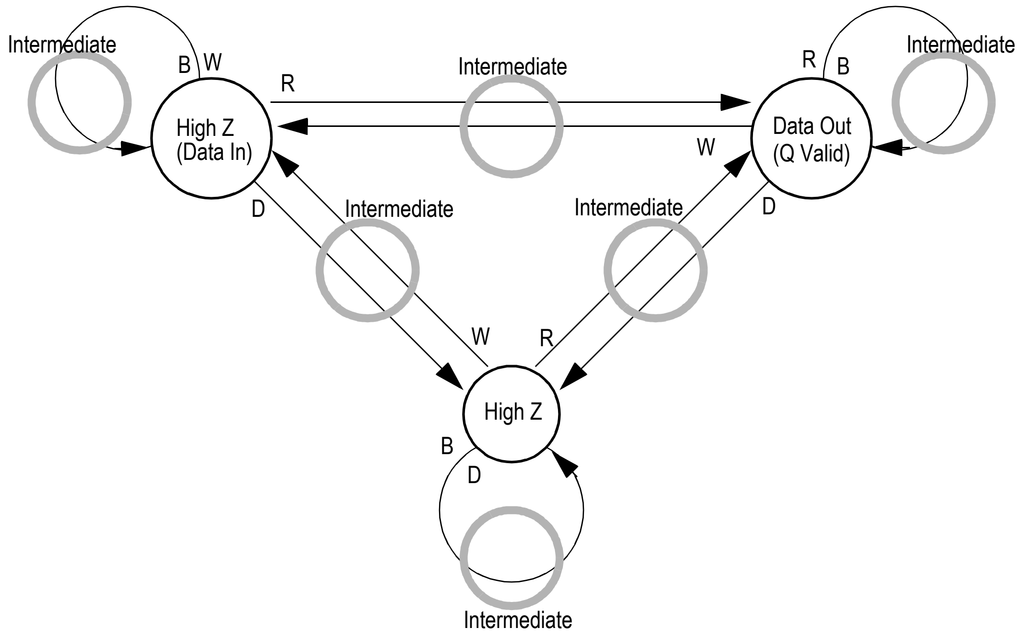
Notes:

1. The Hold command ($\overline{\text{CKE}}$ Low) is not shown because it prevents any state change.
2. W, R, B and D represent input command codes ,as indicated in the Synchronous Truth Table.



Current State and Next State Definition for Pipeline and Flow Through Read/Write Control State Diagram

Pipeline Mode Data I/O State Diagram



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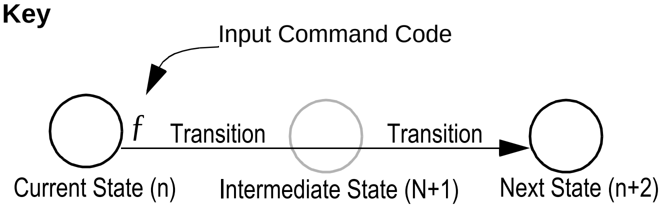
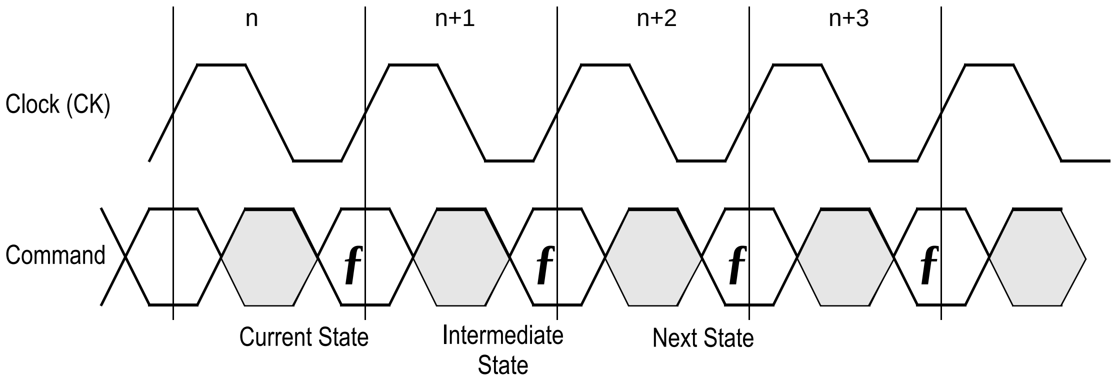


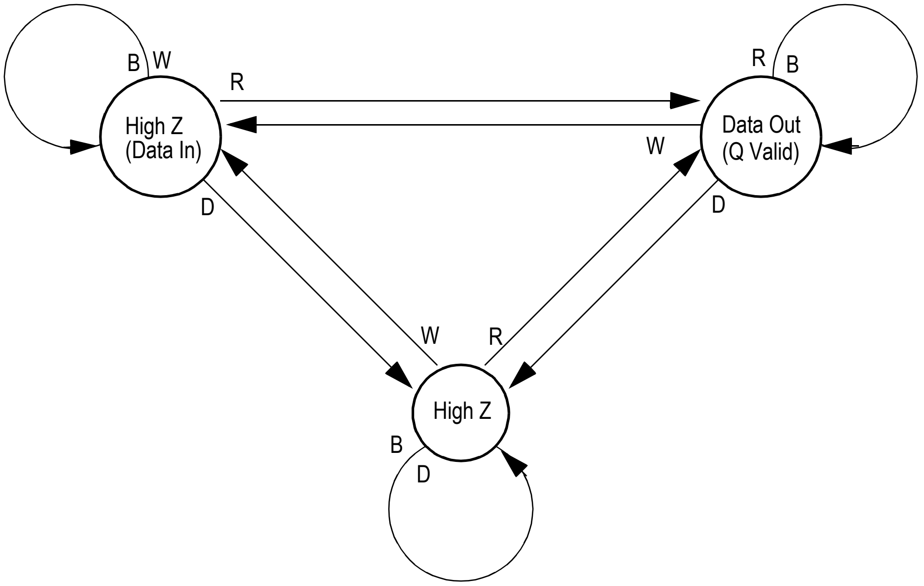
Notes:

1. The Hold command ($\overline{\text{CKE}}$ Low) is not shown because it prevents any state change.
2. W, R, B, and D represent input command codes as indicated in the Truth Tables.

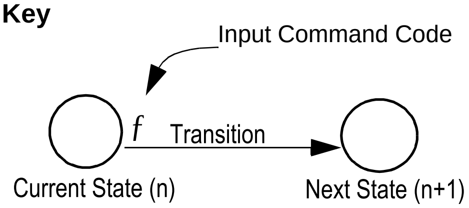


Current State and Next State Definition for Pipeline Mode Data I/O State Diagram

Flow Through Mode Data I/O State Diagram



Key



Notes

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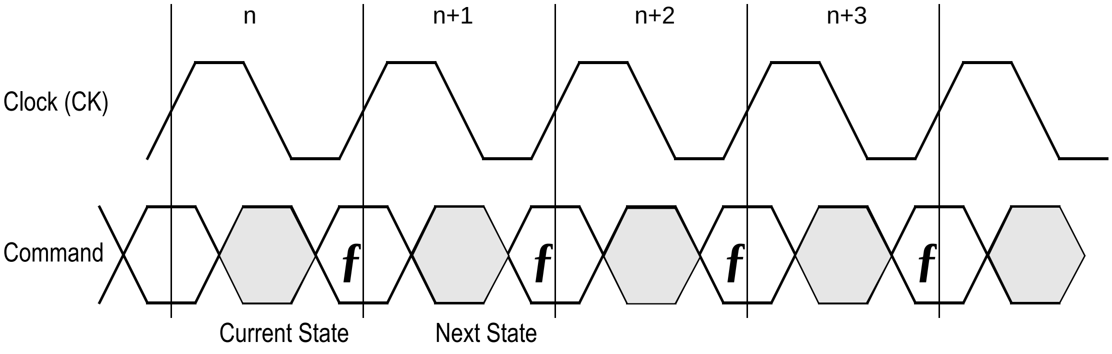

Current State and Next State Definition for: Pipeline and Flow Through Read Write Control State Diagram

Burst Cycles

Although NBT RAMs are designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from read to write, multiple back-to-back reads or writes may also be performed. NBT SRAMs provide an on-chip burst address generator that can be utilized, if desired, to further simplify burst read or write implementations. The ADV control pin, when driven high, commands the SRAM to advance the internal address counter and use the counter generated address to read or write the SRAM. The starting address for the first cycle in a burst cycle series is loaded into the SRAM by driving the ADV pin low, into Load mode.

Burst Order

The burst address counter wraps around to its initial state after four addresses (the loaded address and three more) have been accessed. The burst sequence is determined by the state of the Linear Burst Order pin ($\overline{\text{LBO}}$). When this pin is low, a linear burst sequence is selected. When the RAM is installed with the LBO pin tied high, Interleaved burst sequence is selected. See the tables below for details.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{\text{LBO}}$	L	Linear Burst
		H	Interleaved Burst
Output Register Control	$\overline{\text{FT}}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:
There is a pull-up device on the and $\overline{\text{FT}}$ pin and a pull-down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note: The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note: The burst counter wraps to initial state on the 5th clock.

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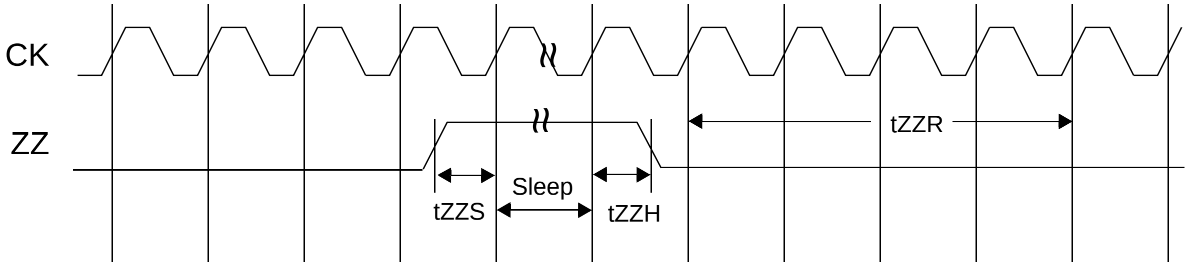
Sleep Mode

During normal operation, ZZ must be pulled low, either by the user or by it's internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after 2 cycles of wake up time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to $I_{SB}2$. The duration of Sleep mode is dictated by the length of time the ZZ is in a high state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, $I_{SB}2$ is guaranteed after the time tZZI is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during tZZR, only a deselect or read commands may be applied while the SRAM is recovering from Sleep mode.

Sleep Mode Timing Diagram



Designing for Compatibility

The GSI NBT SRAMs offer users a configurable selection between Flow Through mode and Pipeline mode via the $\overline{FT}$ signal found on Pin 14. Not all vendors offer this option, however most mark Pin 14 as V_{DD} or V_{DDQ} on pipelined parts and V_{SS} on flow through parts. GSI NBT SRAMs are fully compatible with these sockets.

Pin 66, a No Connect (NC) on GSI’s GS8160Z18/36 NBT SRAM, the Parity Error open drain output on GSI’s GS8161Z18/36 NBT SRAM, is often marked as a power pin on other vendor’s NBT compatible SRAMs. Specifically, it is marked V_{DD} or V_{DDQ} on pipelined parts and V_{SS} on flow through parts. Users of GSI NBT devices who are not actually using the ByteSafe™ parity feature may want to design the board site for the RAM with Pin 66 tied high through a 1k ohm resistor in Pipeline mode applications or tied low in Flow Through mode applications in order to keep the option to use non-configurable devices open. By using the pull-up resistor, rather than tying the pin to one of the power rails, users interested in upgrading to GSI’s ByteSafe NBT SRAMs (GS8161Z18/36), featuring Parity Error detection and JTAG Boundary Scan, will be ready for connection to the active low, open drain Parity Error output driver at Pin 66 on GSI’s TQFP ByteSafe RAMs.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	0.5 to V_{DD}	V
V_{CK}	Voltage on Clock Input Pin	0.5 to 6	V
$V_{I/O}$	Voltage on I/O Pins	0.5 to V_{DDQ} +0.5 ($\leq$ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	0.5 to V_{DD} +0.5 ($\leq$ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/ 20	mA
I_{OUT}	Output Current on Any I/O Pin	+/ 20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	55 to 125	°C
T_{BIAS}	Temperature Under Bias	55 to 125	°C

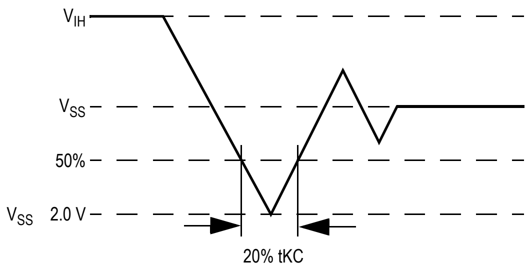
Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

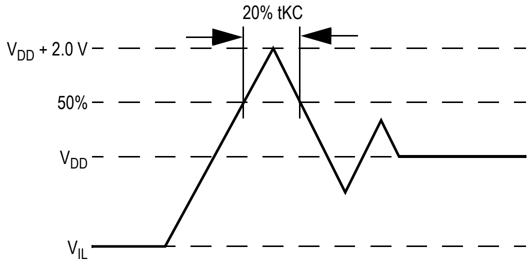
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V_{DD}	3.135	3.3	3.6	V	
I/O Supply Voltage	V_{DDQ}	2.375	2.5	V_{DD}	V	1
Input High Voltage	V_{IH}	1.7		V_{DD} +0.3	V	2
Input Low Voltage	V_{IL}	0.3		0.8	V	2
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	3
Ambient Temperature (Industrial Range Versions)	T_A	40	25	85	°C	3

Notes:
1. Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both 2.75 V $\leq V_{DDQ} \leq$ 2.375 V (i.e., 2.5 V I/O) and 3.6 V $\leq V_{DDQ} \leq$ 3.135 V (i.e., 3.3 V I/O), and quoted at whichever condition is worst case.
2. This device features input buffers compatible with both 3.3 V and 2.5 V I/O drivers.
3. Most speed grades and configurations of this device are offered in both Commercial and Industrial Temperature ranges. The part number of Industrial Temperature Range versions end the character I . Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
4. Input Under/overshoot voltage must be 2 V > Vi < V_{DD} +2 V with a pulse width not to exceed 20% tKC.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

($T_A = 25^oC$, f = 1 MHz, V_{DD} = 3.3 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0 V	6 (x36) 12 (x18)	7 (x36) 12 (x18)	pF

Note: These parameters are sample tested.

Package Thermal Characteristics

Rating	Layer Board	Symbol	Max	Unit	Notes
Junction to Ambient (at 200 lfm)	single	$R_{\Theta JA}$	40	°C/W	1,2
Junction to Ambient (at 200 lfm)	four	$R_{\Theta JA}$	24	°C/W	1,2
Junction to Case (TOP)		$R_{\Theta JC}$	9	°C/W	3

Notes:

1. Junction temperature is a function of SRAM power dissipation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
2. SCMI G-38-87
3. Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1

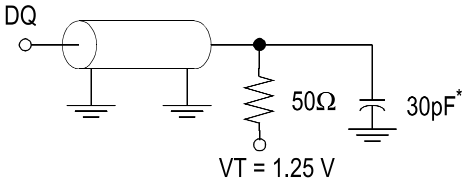
AC Test Conditions

Parameter	Conditions
Input high level	2.3 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	1.25 V
Output reference level	1.25 V
Output load	**Fig. 1& 2**

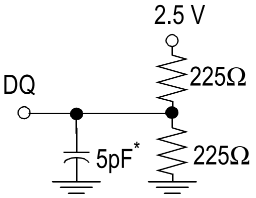
Notes:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output Load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}
4. Device is deselected as defined by the Truth Table.

Output Load 1



Output Load 2



* Distributed Test Jig Capacitance

DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	1 uA	1 uA
ZZ Input Current	I_{INZZ}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0\ V \leq V_{IN} \leq V_{IH}$	1 uA 1 uA	1 uA 300 uA
Mode Pin Input Current	I_{INM}	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0\ V \leq V_{IN} \leq V_{IL}$	300 uA 1 uA	1 uA 1 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	1 uA	1 uA
Output High Voltage	V_{OH}	I_{OH} = 4 mA, V_{DDQ} = 2.375 V	1.7 V	
Output High Voltage	V_{OH}	I_{OH} = 4 mA, V_{DDQ} = 3.135 V	2.4 V	
Output Low Voltage	V_{OL}	I_{OL} = 4 mA		0.4 V

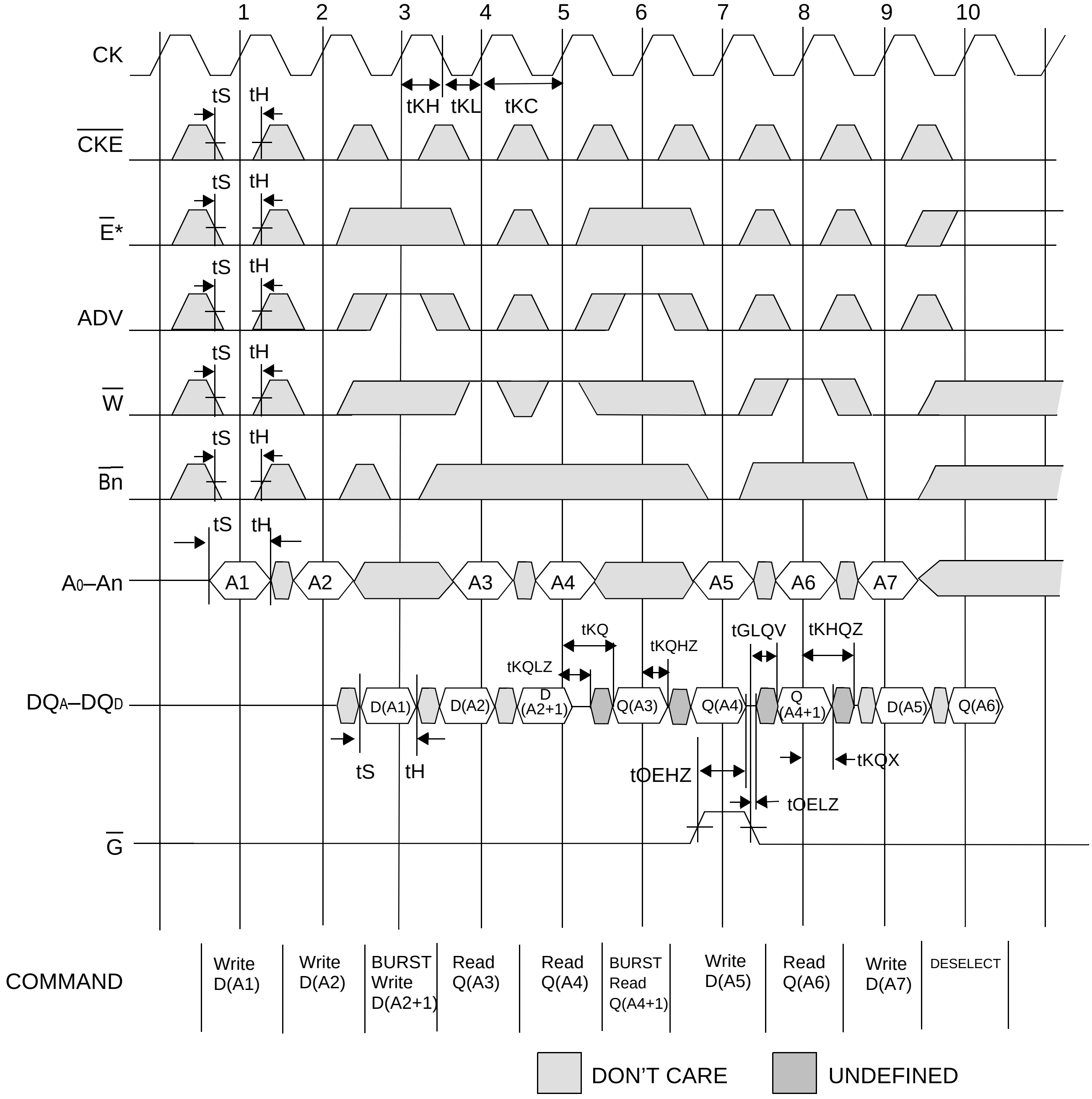
Operating Currents

Parameter	Test Conditions	Mode		Symbol	-225		-200		-180		-166		-150		-133		Unit
					0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	
Operating Current	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	(x36)	Pipeline	I_{DD} I_{DDQ}	335 74	345 84	303 66	313 76	278 59	288 69	260 55	270 65	240 50	250 60	218 44	228 54	mA
			Flow Through	I_{DD} I_{DDQ}	199 39	209 49	177 33	187 43	177 33	187 43	177 33	187 43	177 33	187 43	134 22	144 32	mA
		(x18)	Pipeline	I_{DD} I_{DDQ}	310 37	320 47	281 33	291 43	258 30	268 40	242 27	252 37	223 25	233 35	204 22	214 32	mA
			Flow Through	I_{DD} I_{DDQ}	186 19	196 29	166 17	176 27	166 17	176 27	166 17	176 27	166 17	176 27	127 11	137 21	mA
Standby Current	$ZZ \geq V_{DD} - 0.2$ V	—	Pipeline	I_{SB}	10	20	10	20	10	20	10	20	10	20	10	20	mA
			Flow Through	I_{SB}	10	20	10	20	10	20	10	20	10	20	10	20	mA
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	—	Pipeline	I_{DD}	80	85	75	80	70	75	64	70	60	65	50	55	mA
			Flow Through	I_{DD}	60	65	50	55	50	55	50	55	50	55	45	50	mA

AC Electrical Characteristics

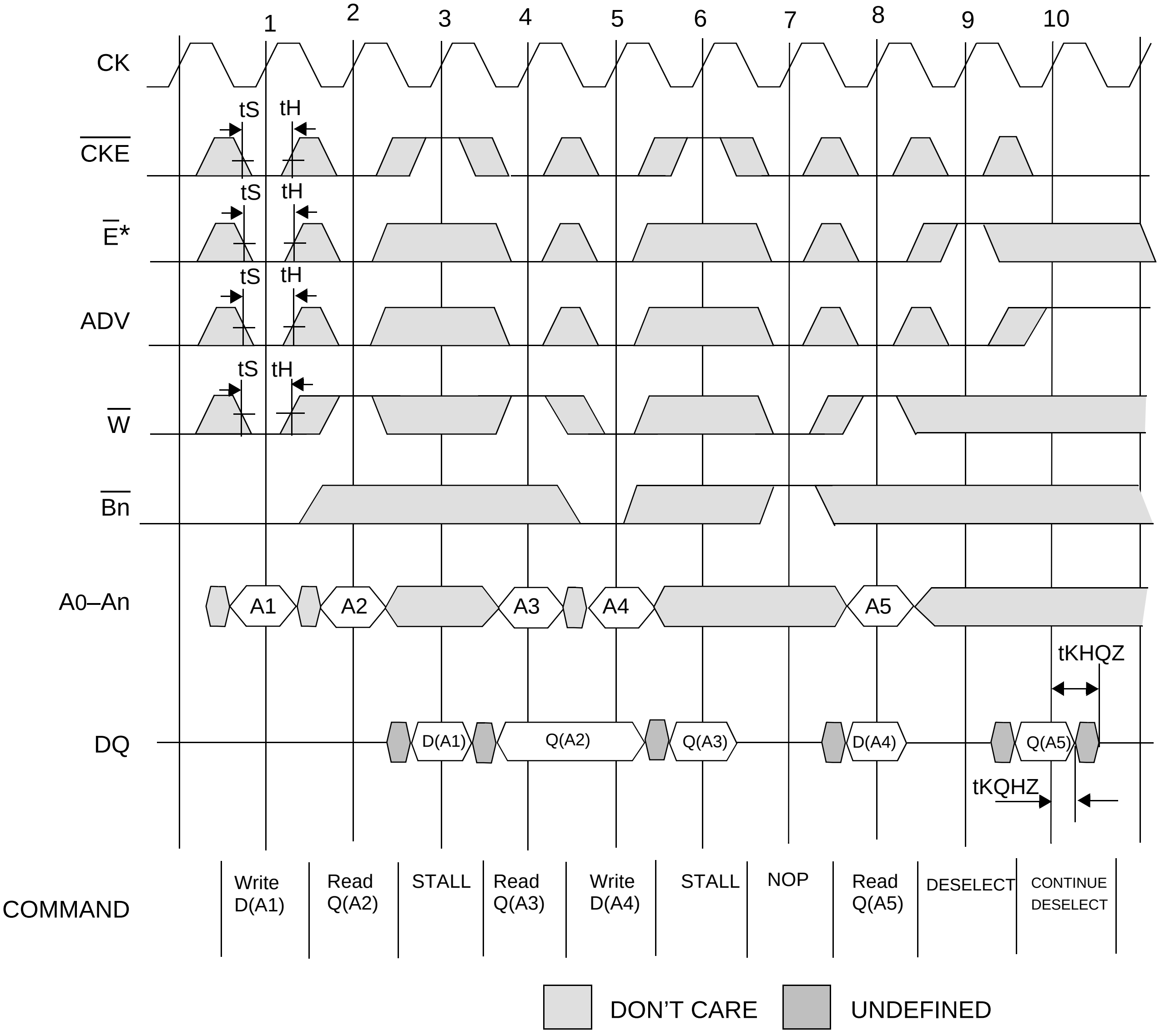
	Parameter	Symbol	-225		-200		-180		-166		-150		-133		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	tKC	4.4	—	5.0	—	5.5	—	6.0	—	6.7	—	7.5	—	ns
	Clock to Output Valid	tKQ	—	2.5	—	3.0	—	3.2	—	3.5	—	3.8	—	4.0	ns
	Clock to Output Invalid	tKQX	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	tLZ[1]	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
Flow Through	Clock Cycle Time	tKC	8.5	—	10.0	—	10.0	—	10.0	—	10.0	—	15.0	—	ns
	Clock to Output Valid	tKQ	—	7.0	—	7.5	—	8.0	—	8.5	—	10.0	—	11.0	ns
	Clock to Output Invalid	tKQX	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock HIGH Time	tKH	1.3	—	1.3	—	1.3	—	1.3	—	1.5	—	1.7	—	ns
	Clock LOW Time	tKL	1.5	—	1.5	—	1.5	—	1.5	—	1.7	—	2	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	2.5	1.5	3.0	1.5	3.2	1.5	3.5	1.5	3.8	1.5	4.0	ns
	$\overline{G}$ to Output Valid	tOE	—	2.5	—	3.2	—	3.2	—	3.5	—	3.8	—	4.0	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	0	—	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	2.5	—	3.0	—	3.2	—	3.5	—	3.8	—	4.0	ns
	Setup time	tS	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	tH	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
	ZZ setup time	tZZS[2]	5	—	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	tZZR	100	—	100	—	100	—	100	—	100	—	100	—	ns

Pipeline Mode Read/Write Cycle Timing



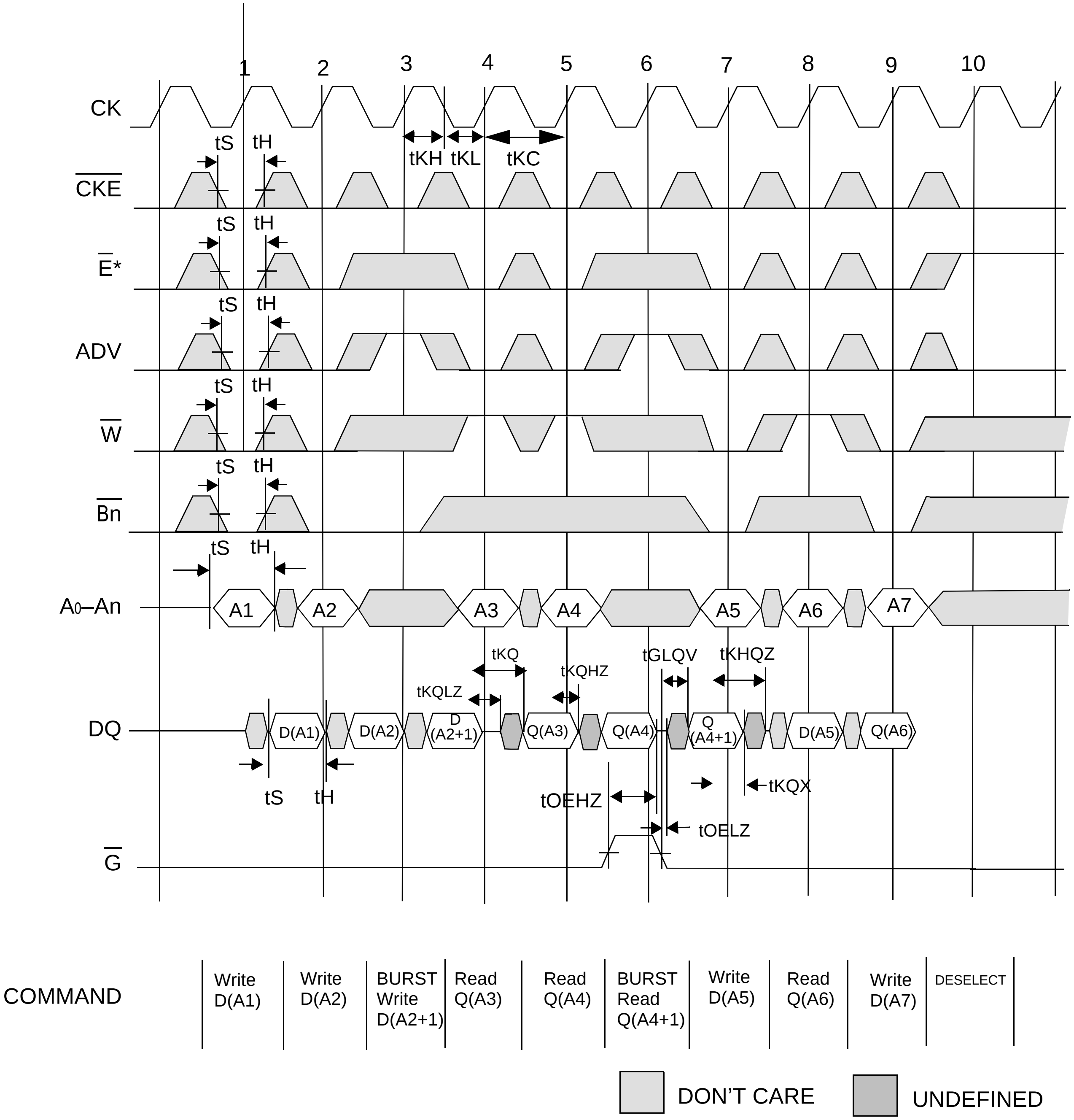
*Note: E = High (False) if $E_1 = 1$ or $E_2 = 0$ or $E_3 = 1$

Pipeline Mode No-Op, Stall and Deselect Timing



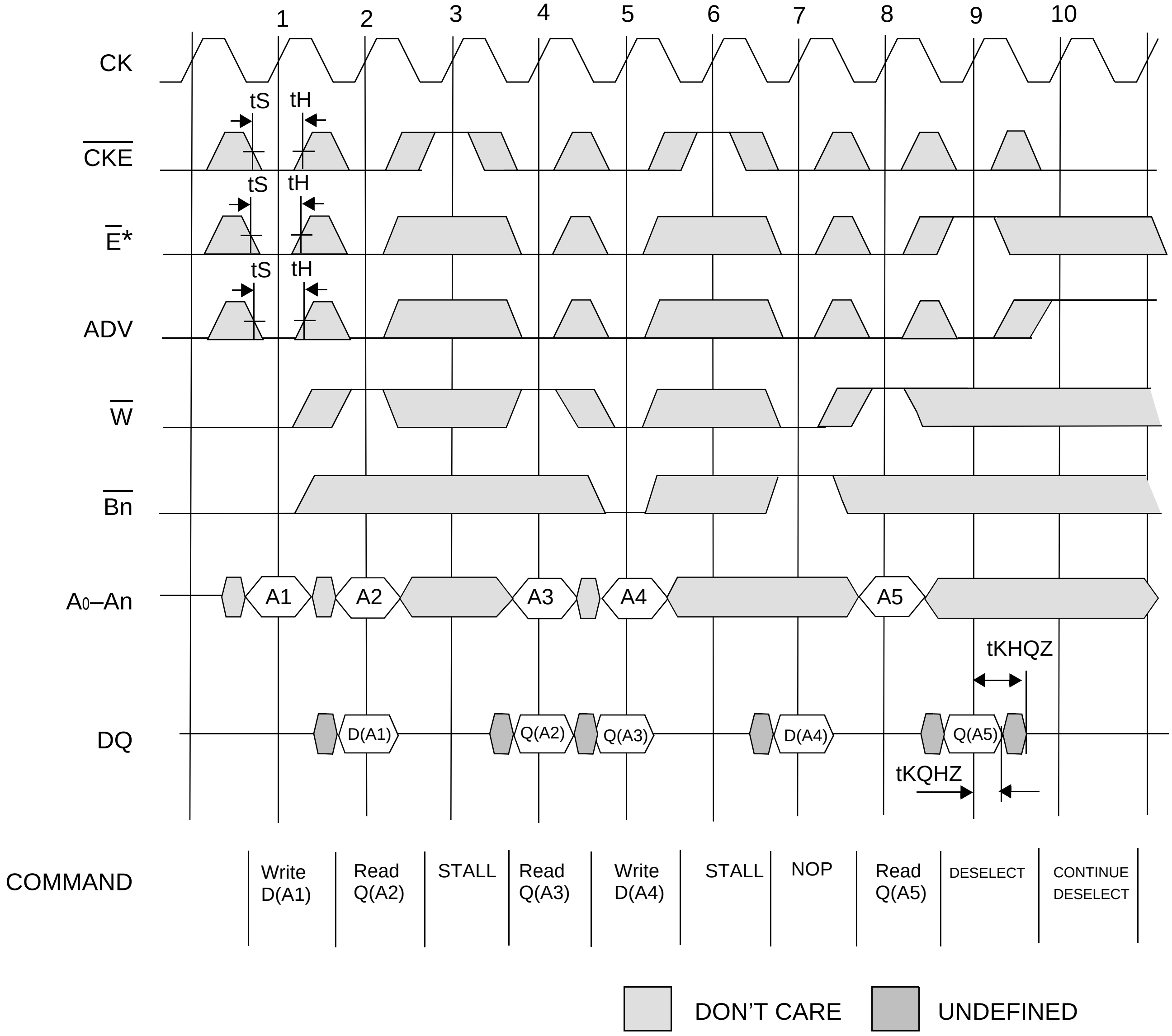
*Note: E = High (False) if $E_1 = 1$ or $E_2 = 0$ or $E_3 = 1$

Flow Through Mode Read/Write Cycle Timing



*Note: $\overline{E}$ = High (False) if $\overline{E}_1 = 1$ or $E_2 = 0$ or $\overline{E}_3 = 1$

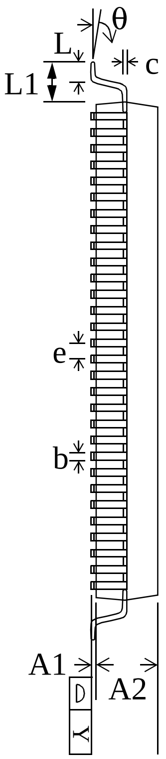
Flow Through Mode No-Op, Stall and Deselect Timing

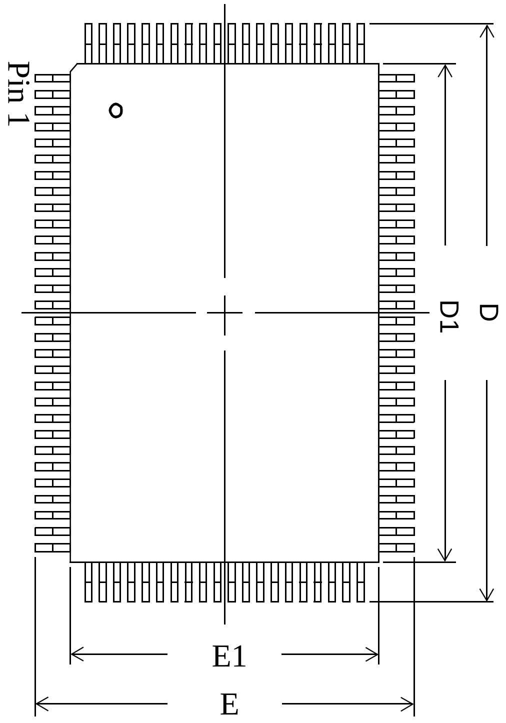


*Note: E = High (False) if E_1 = 1 or E_2 = 0 or E_3 = 1

TQFP Package Drawing

Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09	—	0.20
D	Terminal Dimension	21.9	22.0	20.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch	—	0.65	—
L	Foot Length	0.45	0.60	0.75
L1	Lead Length	—	1.00	—
Y	Coplanarity	—	—	0.10
θ	Lead Angle	0°	—	7°





Notes:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

BPR 1999.05.18

Ordering Information—GSI NBT Synchronous SRAM

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]	Status
1M x 18	GS8150Z18T-225	NBT Pipeline/Flow Through	TQFP	225/7	C	
1M x 18	GS8150Z18T-200	NBT Pipeline/Flow Through	TQFP	200/7.5	C	
1M x 18	GS8150Z18T-180	NBT Pipeline/Flow Through	TQFP	180/8	C	
1M x 18	GS8150Z18T-166	NBT Pipeline/Flow Through	TQFP	166/8.5	C	
1M x 18	GS8150Z18T-150	NBT Pipeline/Flow Through	TQFP	150/10	C	
1M x 18	GS8150Z18T-133	NBT Pipeline/Flow Through	TQFP	133/11	C	
512K x 36	GS8150Z36T-225	NBT Pipeline/Flow Through	TQFP	225/7	C	
512K x 36	GS8150Z36T-200	NBT Pipeline/Flow Through	TQFP	200/7.5	C	
512K x 36	GS8150Z36T-180	NBT Pipeline/Flow Through	TQFP	180/8	C	
512K x 36	GS8150Z36T-166	NBT Pipeline/Flow Through	TQFP	166/8.5	C	
512K x 36	GS8150Z36T-150	NBT Pipeline/Flow Through	TQFP	150/10	C	
512K x 36	GS8150Z36T-133	NBT Pipeline/Flow Through	TQFP	133/11	C	
1M x 18	GS8150Z18T-225I	NBT Pipeline/Flow Through	TQFP	225/7	I	Not Available
1M x 18	GS8150Z18T-200I	NBT Pipeline/Flow Through	TQFP	200/7.5	I	Not Available
1M x 18	GS8150Z18T-180I	NBT Pipeline/Flow Through	TQFP	180/8	I	
1M x 18	GS8150Z18T-166I	NBT Pipeline/Flow Through	TQFP	166/8.5	I	
1M x 18	GS8150Z18T-150I	NBT Pipeline/Flow Through	TQFP	150/10	I	
1M x 18	GS8150Z18T-133I	NBT Pipeline/Flow Through	TQFP	133/11	I	
512K x 36	GS8150Z36T-225I	NBT Pipeline/Flow Through	TQFP	225/7	I	Not Available
512K x 36	GS8150Z36T-200I	NBT Pipeline/Flow Through	TQFP	200/7.5	I	Not Available
512K x 36	GS8150Z36T-180I	NBT Pipeline/Flow Through	TQFP	180/8	I	
512K x 36	GS8150Z36T-166I	NBT Pipeline/Flow Through	TQFP	166/8.5	I	
512K x 36	GS8150Z36T-150I	NBT Pipeline/Flow Through	TQFP	150/10	I	
512K x 36	GS8150Z36T-133I	NBT Pipeline/Flow Through	TQFP	133/11	I	

Notes:

1. Customers requiring delivery in Tape and Reel should add the character T to the end of the part number. Example: GS8150Z36T-100IT.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
3. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings

0.18u 16M Sync SRAM Data Sheet Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
8150Z18_r1		• Creation of new datasheet
8150Z18_r1; 8150Z18_r1_01	Content	• Updated Features list on page 1 • Completely reworked table on page 1 • Updated Mode Pin Functions table on page 11