SED1633

LOW-POWER 100-BIT LCD COMMON DRIVER

■ DESCRIPTION

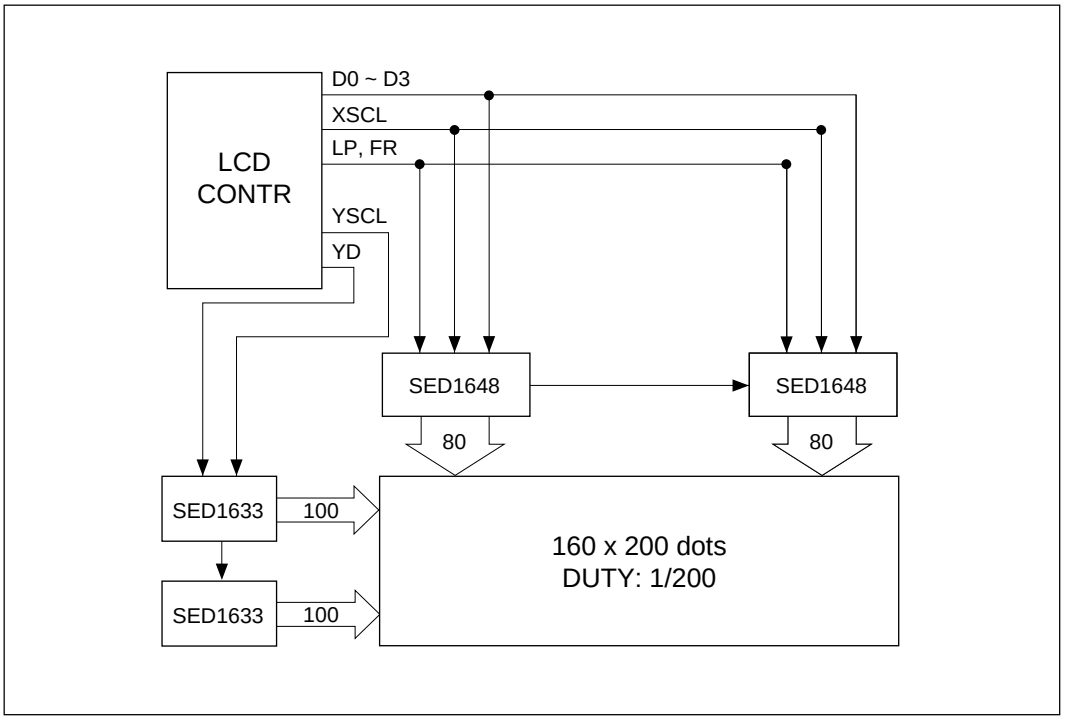
The SED1633 is a 100-output dot matrix LCD common (row) driver for driving high-capacity LCD panels at duty cycles higher than 1/64 (up to 1/300). The LSI has a wide range of LCD driving voltages, and has its maximum drive voltage, VO, isolated from V_{DD} for flexibility of bias voltage generation.

The SED1633 is used in conjunction with the SED1648 (80-output segment driver) or the SED1600 (80-bit segment driver) to drive a large-capacity dot matrix LCD panel).

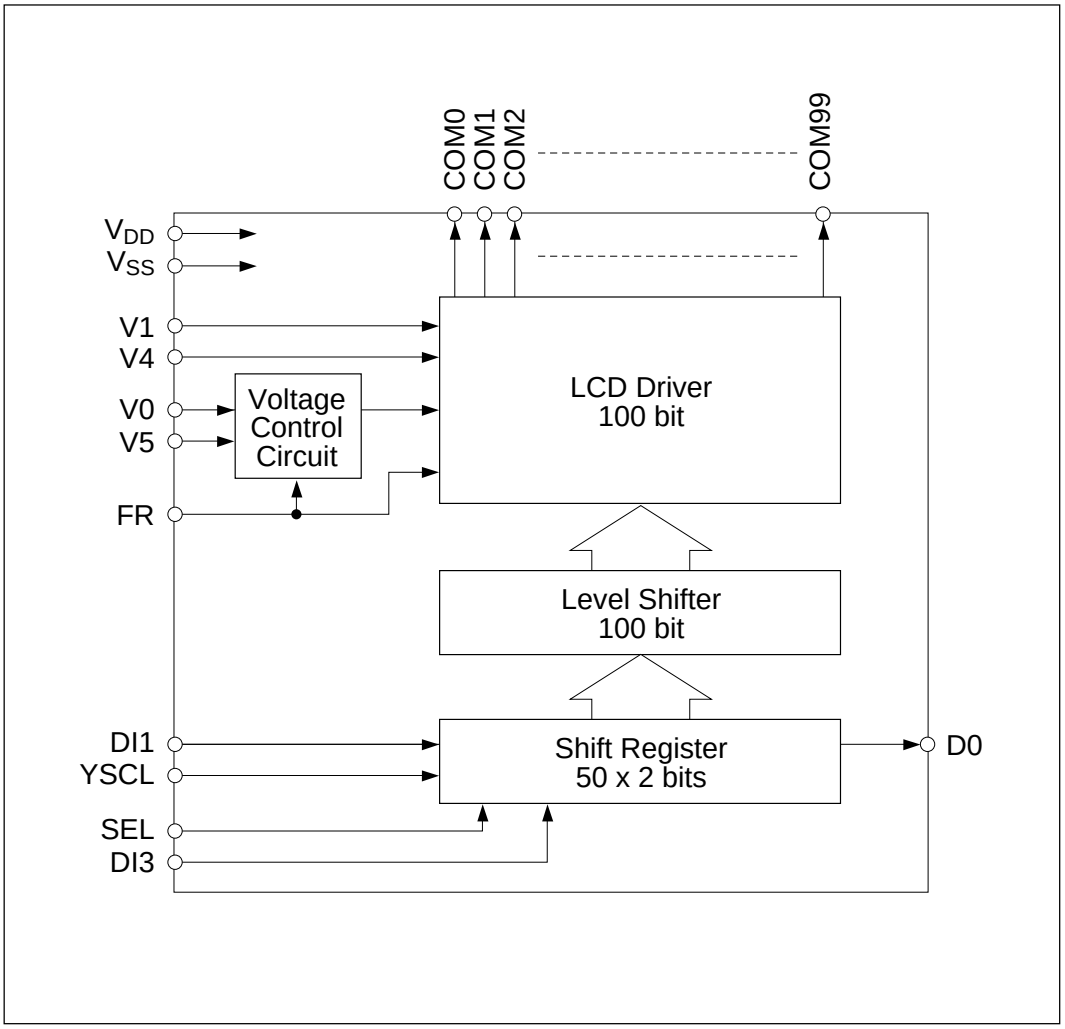
■ FEATURES

- Low-power CMOS technology
- 100-bit (50 × 2 structure) common (row) driver
- Duty cycle ..... 1/64 to 1/300
- Low output impedance 500Ω typ (V1, V4 level)
  700Ω typ (VO, V5 level)
- Duty cycle ..... 1/100 to 1/300
- Ability to adjust offset bias of the LCD relative to V_{DD}
- Non-biased display off function
- Pin selection of the output shift direction
- LCD voltage ..... –8 to –28V
- Supply voltage ..... 2.7 to 5.5V
- Package ..... Al pad (D_{1A})
  Au bump (D_{1B})

■ SYSTEM BLOCK DIAGRAM



■ **BLOCK DIAGRAM**



■ BLOCK DESCRIPTION

● Shift Register

This is a bidirectional shift register for common data transmission.

● Shift Direction

SED1633	COM 0 → COM 99	
SED1634	COM 99 → COM 0	Reference

● Level Shifter

This is a level interface circuit for shifting the signal voltage from the logic system level to the LCD driver system level.

● LCD Drivers and Voltage Controller Circuit

Outputs the LCD driver voltage.

The relationships between the content of the shift register, the alternating signal FR, and the common output voltage are as shown in the table below:

Contents of Shift Register	FR	COM Output Voltage	
H	H	V5	Select level
	L	V0	
L	H	V1	Non-select level
	L	V4	

■ PIN DESCRIPTION

Pin Name	I/O	Function	No. of Pins
COM0-COM99	O	LCD driver common (row) output Changes on the falling edge of the YSCL signal.	100
DI1, DI3	I	Serial data input for the 100 bit shift register. DI3 is the intermediate shift input. (When DI3 is unused, tie it to V_{DD} or V_{SS}.)	2
YSCL	I	Serial data shift clock input. Scanning data is shifted at the falling edge.	1
FR	I	LCD driver output AC signal input	1
V_{DD}, V_{SS}	Power	Power source for logic. V_{DD}: 0V (GND). V_{SS}: –5.0V	2
V0, V1, V4, V5	Power	Power source for LCD driver. V5: –12 to –28 V $V_{DD} \geq V0 \geq V1 > V4 \geq V5$	4
SEL	I	Shift Register Operating Configuration Selection: SEL: H → 50 × 2, Input SEL: L → 100 × 1, H/L	1
DO	O	Shift register data output. The output changes with the falling edge of the YSCL signal.	1

Total: 112

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Condition	Unit
Power voltage (1)	V_{SS}	–7.0 to +0.3	V
Power voltage (2)	V5	–30.0 to +0.3	V
Power voltage (3)	V0, V1, V4	V5 – 0.3 to + 0.3	V
Input voltage	VI	V_{SS} – 0.3 to + 0.3	V
Output voltage	VO	V_{SS} – 0.3 to + 0.3	V
Output current (1)	IO	20	mA
Output current (2)	IOCOM	20	mA
Operating temperature	Topr	–40 to +85	°C
Storage temperature	Tstg	–65 to +150	°C

Notes: *1. The voltages are all relative to V_{DD} = 0V.

*2. Ensure that the relationship between V0, V1, and V4 is always as follows: $V_{DD} \geq V0 \geq V1 \geq V4 \geq V5$.

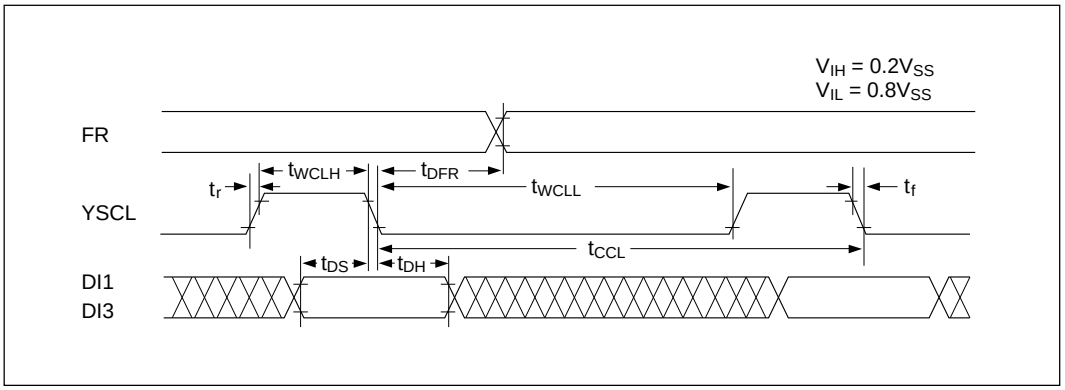
*3. The LSI may be permanently damaged if the logic system power is floating or V_{SS} is less than or equal to –2.6V when power is applied to the LC drive circuit system. Special caution must be paid to the power sequences when turning the power on and off.

● DC Electrical Characteristics

Unless otherwise specified, V_{DD} = V0 = 0V, V_{SS} = –5.0V ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Applicable Pins	Min	Typ	Max	Unit
Power voltage (1)	V_{SS}		V_{SS}	–5.5	–5.0	–2.7	V
Recommended operating voltage	V5		V5	–28.0	—	–12.0	V
Possible operating voltage	V5	Function	V5	—	—	–8.0	V
Power voltage (2)	V0	Recommended value	V0	–2.5	—	0	V
Power voltage (3) Power voltage (4)	V1 V4	Recommended value	V1 V4	2/9 × V5 V5	—	V_{DD} 7/9 × V5	V
High-level input voltage	V_{IH}	V_{SS} = –2.7 to –5.5V	DI1, YSCL, SEL, DI3, FR	0.2 × V_{SS}	—	—	V
Low-level input voltage	V_{IL}			—	—	0.8 × V_{SS}	V
High-level output voltage	V_{OH}	I_{OH} = –0.3mA I_{OH} = –0.2mA (V_{SS} = –2.7 to –4.5V)	DO	–0.4	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 0.3mA I_{OL} = 0.2mA (V_{SS} = –2.7 to –4.5V)		—	—	V_{SS} + 0.4	V
Input leakage current	I_{LI}	$V_{SS} \le V_{IN} \le 0V$	YSCL, SEL, DI3, FR	—	—	2.0	µA
I/O leakage current	I_{LO}	$V_{SS} \le V_{IN} \le 0V$	DI1, DO	—	—	5.0	µA
Static current	I_{DDS}	V5 = –12.0 to –28.0V V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{DD}	—	—	25	µA
Output resistance	R_{COM}	Δ|V_{ON}| = 0.5V; V5 = –20.0V, V5 = –14.0V, *(V5 = –8.0V); When outputting the V1, V4 levels; COM0 ~ COM99		—	0.40 0.50 (0.60)	0.80 1.00 (1.20)	KΩ
		Δ|V_{ON}| = 0.5V; V5 = –20.0V, V5 = –14.0V, *(V5 = –8.0V); When outputting the V0, V5 levels; *Reference value		—	0.60 0.70 (0.90)	1.20 1.40 (1.80)	
Average operating current consumption (1)	I_{SS1}	V_{SS} = –5.0V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{YSCL} = 12KHz, Frame frequency = 60KHz, Input data: 1/200, "H" is without load on each duty cycle	V_{SS}	—	7	15	µA
		V_{SS} = –3.0V; other parameters are identical		—	5	10	
Average operating current consumption (2)	I_{SS2}	V_{SS} = –5.0V, V1 = –2.0V, V4 = –18.0V, V5 = –20.0V; other parameters are the same as for I_{SS1}	V5	—	7	15	µA
Input terminal capacitance	C_I	T_a = 25°C	YSCL, SEL, DI3, FR	—	—	8	pF
I/O terminal capacitance	$C_{I/O}$		DI1, DO	—	—	15	pF

- **AC Characteristics**
  - **Input Timing Characteristics**



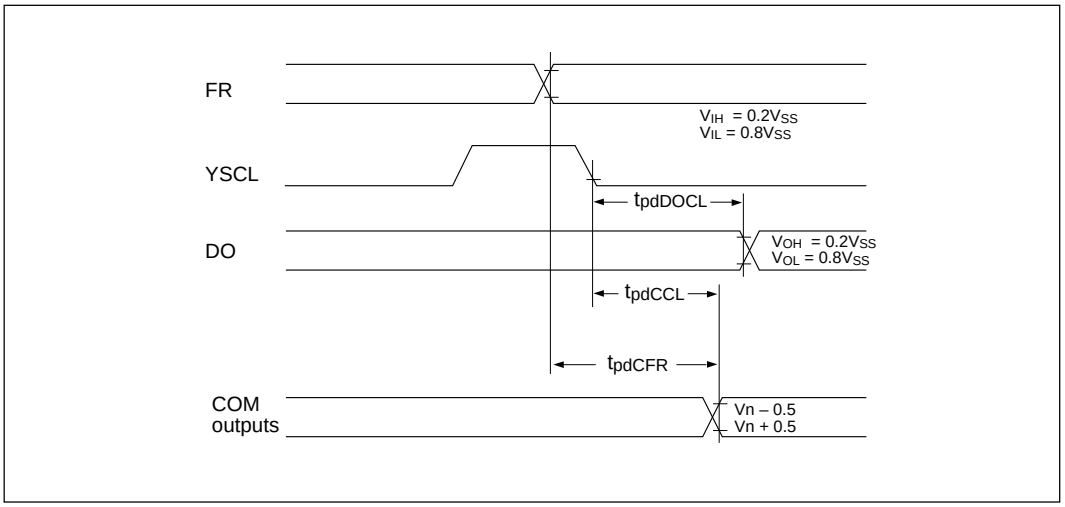
V_{SS} = –5.0 ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input signal rise time	tr		—	50	ns
Input signal fall time	tf		—	50	ns
YSCL frequency	t_{CCL}		500	—	ns
YSCL high-level pulse width	t_{WCLH}		70	—	ns
YSCL low-level pulse width	t_{WCLL}		330	—	ns
Data setup time	t_{DS}		100	—	ns
Data hold time	t_{DH}		10	—	ns
Allowable FR delay	t_{DFR}		–500	500	ns

V_{SS} = –2.7 to –4.5V, Ta = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input signal rise time	tr		—	50	ns
Input signal fall time	tf		—	50	ns
YSCL frequency	t_{CCL}		1000	—	ns
YSCL high-level pulse width	t_{WCLH}		160	—	ns
YSCL low-level pulse width	t_{WCLL}		330	—	ns
Data setup time	t_{DS}		200	—	ns
Data hold time	t_{DH}		10	—	ns
Allowable FR delay	t_{DFR}		–500	500	ns

○ **Output Timing Characteristics**



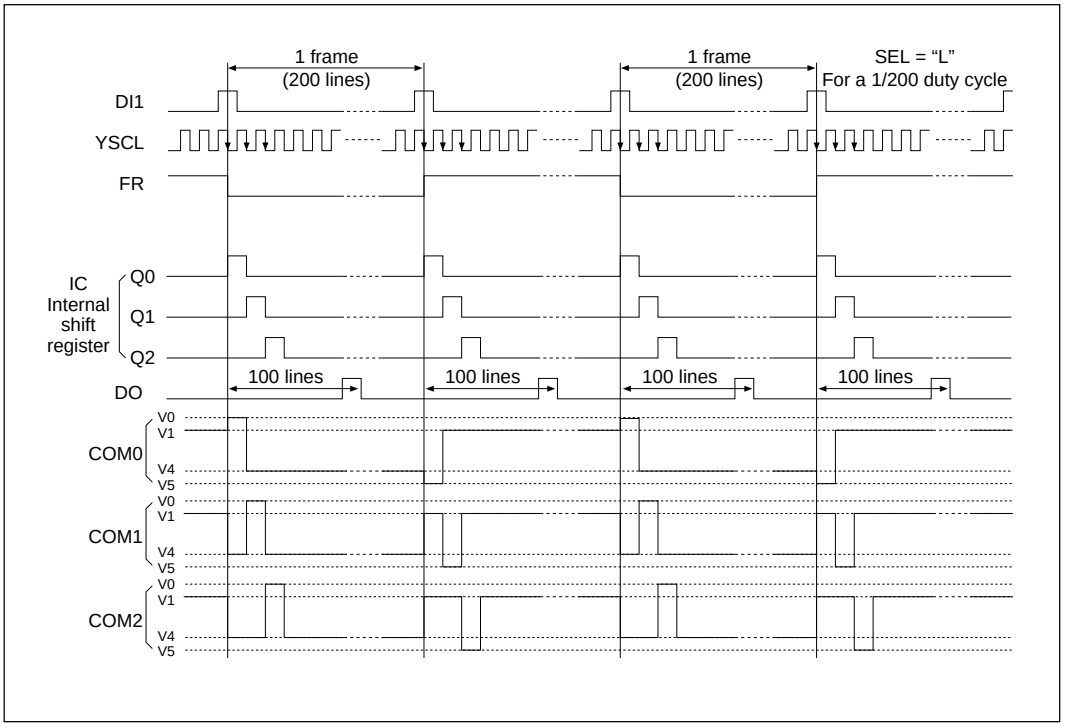
V_{SS} = –5.0V ± 10%, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
(YSCL fall → D0) delay time	t_{pdDOCL}	CL = 15pF	30	300	ns
(YSCL fall → COM output) delay time	t_{pdCCL}	V5 = –12.0 to –28.0V	—	3.0	µs
(FR → COM output) delay time	t_{pdCFR}	CL = 100pF	—	3.0	µs

V_{SS} = –2.7 to –4.5V, T_a = –40 to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
(YSCL fall → D0) delay time	t_{pdDOCL}	CL = 15pF	60	600	ns
(YSCL fall → COM output) delay time	t_{pdCCL}	V5 = –12.0 to –28.0V	—	3.0	µs
(FR → COM output) delay time	t_{pdCFR}	CL = 100pF	—	3.0	µs

- **Timing Diagram**



■ LCD DRIVING POWER

- **Method of Forming Each Voltage Level**

The simplest way to obtain the voltage levels for driving the LCs is to use resistive voltage dividers, as shown in the example connection figure. Because a high quality display requires precise and stable voltage levels, the values of the dividing resistances must be set at the low end of the tolerance range of the power capacity.

When there is the need to operate with low power, the values of the voltage dividing resisters must be set high, and the LCs must be driven by an op amp voltage follower. In consideration of the use of op amps, V0 (the highest voltage setting for driving LCs) and V_{DD} are separated and given separate terminals.

However, when the voltage level of V0 is below V_{DD} and the voltage difference between the two is large, the performance of the LC output driver is reduced. Therefore ensure that the voltage gap between V0 and V_{DD} is in the range of 0V to 2.5V.

Connect V0 and V_{DD} when an op amp is not used.

- **Cautions During Power Up and Power Down**

Because of the high voltage of the LC driving system of this LSI, if the power to the logic system is floating when a high voltage is applied to the LC driving system, then too much current will flow, causing damage to the LSI.

Follow the sequences below during power up and power down:

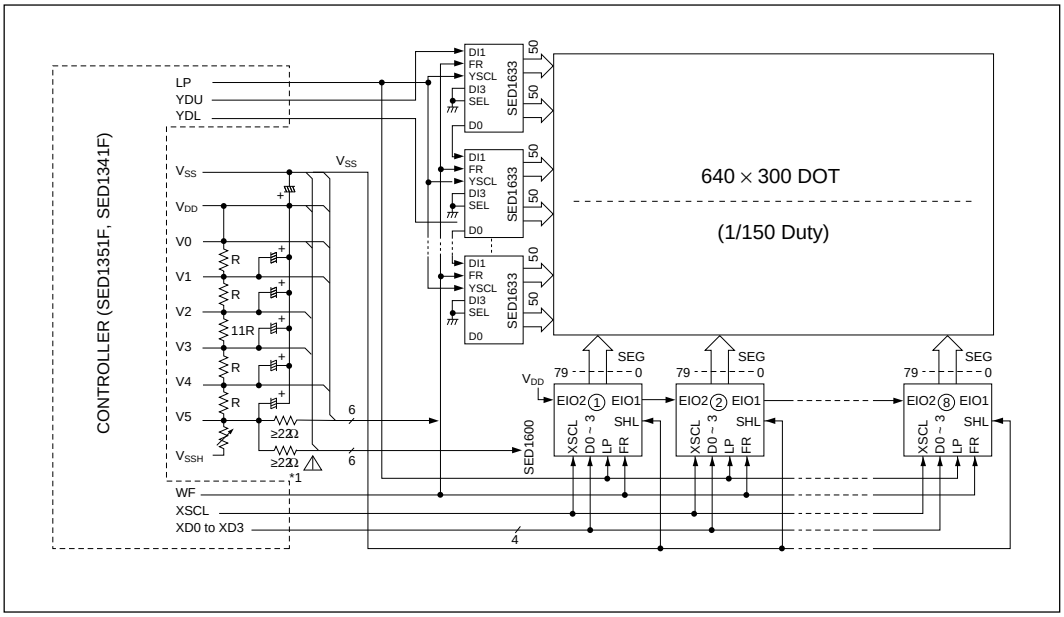
Power up: Logic system on → LC drive system on (or simultaneous)

Power down: LC drive system off → Logic system off (or simultaneous)

In order to prevent excessive current, insert a guard resistance of at least 22 Ω in series with V5.

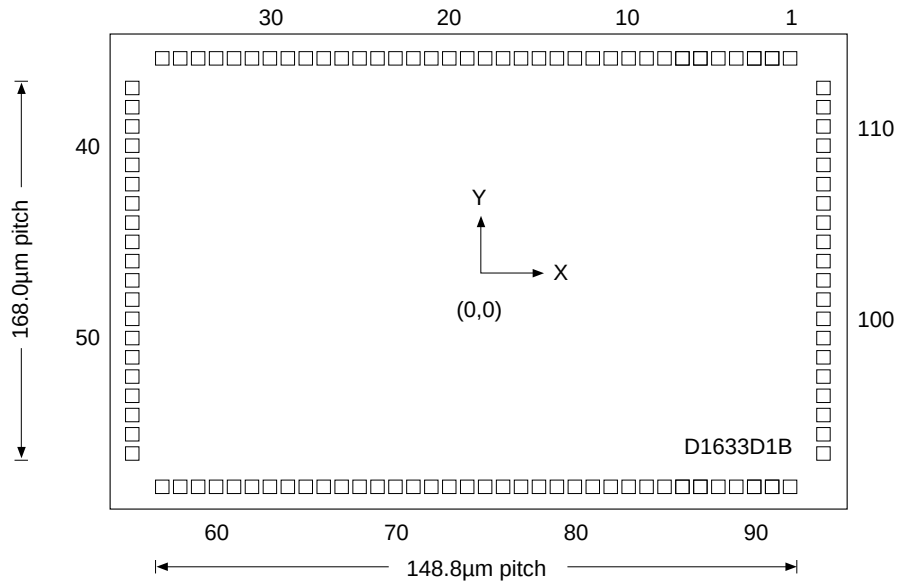
■ EXAMPLE OF CONNECTION

● Connections for a 640 × 300 dot matrix LCD



Note: *1. A guard resistance must be used to prevent excessive current. Moreover, a bypass capacitor (0.01µF) should be used near the V_{SS} and V5 pins of each LSI to prevent noise.

■ PAD LAYOUT



SED1663D1A Specifications (The Al Pad Model)

Chip size ..... 6.03 mm × 4.01 mm
Chip thickness ..... 0.400 mm
Pad opening ..... 101 mm (X) × 110 mm (Y)
(where the Y direction is the direction of the chip center line)

SED1663D1B Specifications (The Au Bump Model)

Chip size ..... 6.03 mm × 4.01 mm
Chip thickness ..... 0.525 mm
Bump size ..... 117 µm × 105 µm
Bump height: ..... 20 µm +10 µm
(reference values) –5 µm

■ PAD COORDINATES

Applicable to the SED1633D1A and SED1633D1B.

Unit: µm

Pad No.	Pad Name	X Coord.	Y Coord.
1	COM5	2604	1834
2	COM6	2455	1834
3	COM7	2306	1834
4	COM8	2158	1834
5	COM9	2009	1834
6	COM10	1860	1834
7	COM11	1711	1834
8	COM12	1562	1834
9	COM13	1414	1834
10	COM14	1265	1834
11	COM15	1116	1834
12	COM16	967	1834
13	COM17	818	1834
14	COM18	670	1834
15	COM19	521	1834
16	COM20	372	1834
17	COM21	223	1834
18	COM22	74	1834
19	COM23	–74	1834
20	COM24	–223	1834
21	COM25	–372	1834
22	COM26	–521	1834
23	COM27	–670	1834
24	COM28	–818	1834
25	COM29	–967	1834
26	COM30	–1116	1834
27	COM31	–1265	1834
28	COM32	–1414	1834
29	COM33	–1562	1834
30	COM34	–1711	1834
31	COM35	–1860	1834
32	COM36	–2009	1834
33	COM37	–2158	1834
34	COM38	–2306	1834
35	COM39	–2455	1834
36	COM40	–2604	1834
37	COM41	–2842	1596
38	COM42	–2842	1428
39	COM43	–2842	1260
40	COM44	–2842	1092
41	COM45	–2842	924
42	COM46	–2842	756
43	COM47	–2842	588
44	COM48	–2842	420
45	COM49	–2842	252
46	COM50	–2842	84
47	COM51	–2842	–84
48	COM52	–2842	–252
49	COM53	–2842	–420
50	COM54	–2842	–588
51	COM55	–2842	–756
52	COM56	–2842	–924
53	COM57	–2842	–1092
54	COM58	–2842	–1260
55	COM59	–2842	–1428
56	COM60	–2842	–1596
57	COM61	–2604	–1834
58	COM62	–2455	–1834
59	COM63	–2306	–1834
60	COM64	–2158	–1834
61	COM65	–2009	–1834
62	COM66	–1860	–1834
63	COM67	–1711	–1834
64	COM68	–1562	–1834
65	COM69	–1414	–1834
66	COM70	–1265	–1834
67	COM71	–1116	–1834
68	COM72	–967	–1834
69	COM73	–818	–1834
70	COM74	–670	–1834
71	COM75	–521	–1834
72	COM76	–372	–1834
73	COM77	–223	–1834
74	COM78	–74	–1834
75	COM79	74	–1834
76	COM80	223	–1834
77	COM81	372	–1834
78	COM82	521	–1834
79	COM83	670	–1834
80	COM84	818	–1834
81	COM85	967	–1834
82	COM86	1116	–1834
83	COM87	1265	–1834
84	COM88	1414	–1834
85	COM89	1562	–1834
86	COM90	1711	–1834
87	COM91	1860	–1834
88	COM92	2009	–1834
89	COM93	2158	–1834
90	COM94	2306	–1834
91	COM95	2455	–1834
92	COM96	2604	–1834
93	COM97	2842	–1596
94	COM98	2842	–1428
95	COM99	2842	–1260
96	D0	2842	–1092
97	DI3	2842	–924
98	FR	2842	–756
99	YSCL	2842	–588
100	SEL	2842	–420
101	V_{DD}	2842	–252
102	V_{SS}	2842	–84
103	V0	2842	84
104	V1	2842	252
105	V4	2842	420
106	V5	2842	588
107	DI1	2842	756
108	COM0	2842	924
109	COM1	2842	1092
110	COM2	2842	1260
111	COM3	2842	1428
112	COM4	2842	1596

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