DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT7132

Quad precision adjustable Schmitt-trigger / comparator with output latches; 3-state

Product specification
File under Integrated Circuits, IC06

September 1993

Philips Semiconductors

PHILIPS

Quad precision adjustable Schmitt-trigger / comparator with output latches; 3-state

74HC/HCT7132

FEATURES

- Precision inputs
- 2 operation modes: PAST and comparator
- In PAST mode: Inverting outputs in view of the precision oscillator application
- In comparator mode: Non-inverting outputs to simplify the design of an external hysteresis network
- 3-state outputs for bus oriented applications
- Output capability: Bus driver
- I_{CC} category: MSI

APPLICATIONS

- Precision oscillators
- Signal reconditioning
- Level conversion
- Process control (temperature, pressure, power e.g.)
- Accurate level detectors
- Time delays
- Overvoltage, overcurrent protection
- Bargraph display with LED's
- Battery charge control
- Analog to digital conversion

DESCRIPTION

The 74HC/HCT7132 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7132 contain 4 comparators with two common reference inputs V_{rH} and V_{rL} and four separate signal inputs V_{in0} to V_{in3}. The circuits can be applied in two modes:

1. The PAST (precision adjustable Schmitt-trigger) mode at which a voltage level equal to the wanted V_{T+} must be applied to the V_{rH} input and a voltage level equal to the wanted V_{T-} to the V_{rL} input.
2. The comparator mode at which the V_{rL} input must be connected to GND and the V_{rH} input is the active reference level input. In this mode a few resistors must be added to achieve a small hysteresis in order to avoid oscillations. The operation in both modes will be further explained by means of the logic diagram of Fig.5.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
V_{rH}	High trip level	PAST mode; V_{CC} = 3 to 6 V	1.15 to V_{CC} – 1.2	V
	reference level	Comparator mode; V_{CC} = 3 to 6 V	0.6 to V_{CC}	V
V_{rL}	Low trip level	PAST mode; V_{CC} = 3 to 6 V	1.10 to V_{CC} – 1.25	V
δV_t	DC inaccuracy	V_{CC} = 3 to 6 V	±20	mV
C_{PD}	power dissipation capacitance per function	V_{CC} = 5 V		
		PAST mode	100	pF
		Comparator mode	30	pF
P_d	Total DC power dissipation	Comparator mode; V_{CC} = 4.5 V; $V_{rL} = V_{INn}$ = 0 V; V_{rH} = 2.25 V	8	mW
t_{rmin}/t_{fmin}	Minimum rise and fall time for optimum operation	PAST mode; V_{CC} = 4.5 V; V_{rH} = 3 V; V_{rL} = 1.5 V	180	ns
t_{PHL}/t_{PLH}	propagation delay V_{inn} to Q	PAST mode; V_{CC} = 4.5 V	40/60	ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + C_L \times V_{CC}^2 \times f_o$ where:

   f_i = input frequency in MHz;

   f_o = output frequency in MHz;

   C_L = output load capacity in pF;

   V_{CC} = supply voltage in V.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT7132P	14	DIL	plastic	SOT27
74HC/HCT7132T	14	SO	plastic	SOT108

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 6, 8, 13	Q_0 to Q_3	3-state latch outputs
2	$\overline{OE}$	3-state output enable input (active LOW)
3, 5, 10, 12	V_{in0} to V_{in3}	signal inputs
4	V_{rL}	low reference voltage input
7	GND	ground (0 V)
9	LE	latch enable input (active HIGH)
11	V_{rH}	high reference voltage input
14	V_{CC}	positive supply voltage

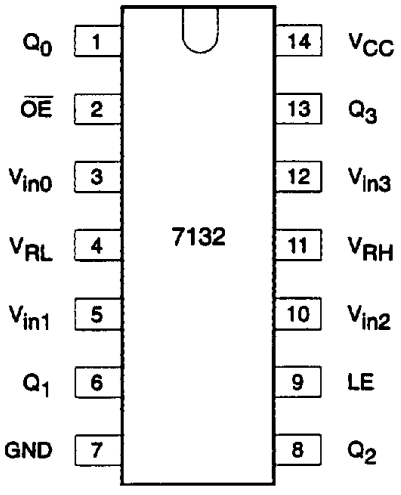


Fig.1 Pin configuration.

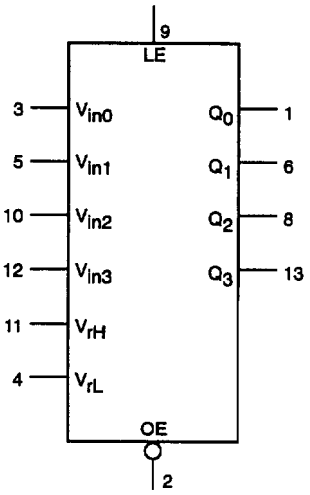


Fig.2 Logic symbol.

Table 1 Function table for PAST mode

V_{inn} (rising edge)	LE	$\overline{OE}$	Q_n
$V_{inn} < V_{LL}$	L	L	H
$V_{LL} < V_{inn} < V_{rH}$	L	L	H
$V_{HH} > V_{inn} > V_{rH}$	L	L	L
$V_{inn} > V_{HH}$	L	L	L
V_{inn} (falling edge)	**LE**	**$\overline{OE}$**	**Q_n**
$V_{HH} > V_{inn} > V_{rL}$	L	L	L
$V_{LL} < V_{inn} < V_{rL}$	L	L	H
$V_{inn} < V_{LL}$	L	L	H
V_{inn} = X	H	L	Q_{t-1}
V_{inn} = X	X	H	Z

Note

1. H = HIGH voltage level
   L = LOW voltage level
   Z = high impedance OFF-state
   X = don't care
   Q_{t-1} = initial state

DETAILED DESCRIPTION

The mode selector.

See Fig.5 for logic diagram. The circuit can be applied in two modes that are selected by the mode selector on bases of the level on the V_{rL} input. When the level on this input is in the operating area of the PAST mode ($V_{rL} > 1$ V) the true output of the mode detector is "0" which means that the PAST mode is selected. When the V_{rL} input is at GND level the true output of the mode detector is "1" by which the comparator mode is selected. This mode needs only one reference input being the V_{rH} input.

The Power-on Detector

The power-on detector selects a window typically between $V_{INn} = 1$ V and $V_{INn} = V_{CC} - 1$ V in which in case of the PAST mode the power of the analog part (comparator) is switched on. When operating in the comparator mode the power is always switched on by means of an OR gate.

The digital detector

The digital detector is a Flip-Flop which output is set to LOW when $V_{INn} < 1$ V and to HIGH when $V_{INn} > V_{CC} - 1$ V. This detector controls the output stage in the cases that the power of the comparator is switched off. This is performed by means of the switches SW_3 and SW_4.

The latch

The output information can be stored in a latch on activating the LE input. In the PAST mode this latch is also used to control the reference input of the comparator which is either connected to the V_{rH} input via SW_1 or to the V_{rL} input via SW_2. In case of the comparator mode the reference input is always connected to the V_{rH} input. This is done by means of an AND gate.

The exclusive OR gate

By means of this function the output stage is switched between inverting and non-inverting. In the PAST mode the inverting output of the mode selector is "1" so the exclusive OR is inverting. In the comparator mode this output is "0" so the exclusive OR is non-inverting.

The operation in the PAST mode

The operation in the PAST mode will be further outlined with the aid of Fig.5 and 9. and Table 1. When the level of V_{INn} is 0 V the power of the comparator is switched OFF and the output circuit is controlled by the digital detector which output is LOW in that situation. So the output of the transparent latch is LOW. As the output stage is inverting now Q_n is HIGH. In this condition the reference input of the comparator is connected to the $+V_{rH}$ input. When starting from 0 V the level at V_{inn} is increased, at about the V_{LL} level (≈1 V) the DC power of the comparator is switched ON. The control of the output circuit is switched over from the digital detector output to the comparator output, when after a delay the voltage at this node is stabilised. During this operation the output level of the latch output remains LOW and the level of Q_n HIGH. When the level at V_{inn} reaches the V_{rH} level the output level of the comparator turns to HIGH and so the output level of the transparent latch. The level at Q_n turns to LOW. In this instant the reference input of the comparator is switched over from V_{rH} to V_{rL} leaving the output voltage at Q_n constant. When the level at V_{inn} reaches the V_{HH} level ($\approx V_{CC} - 1$ V) the DC power of the comparator is switched OFF. The control of the output circuit is switched over from the comparator output to the digital detector output which voltage level is HIGH in this situation. During this action the level at Q_n remains LOW. When the level at the V_{inn} input is decreased starting at V_{CC} level, at the V_{HH} level ($\approx V_{CC} - 1$ V) the power of the comparator will be switched on again. The control of the output circuit is switched over from the digital detector output to the comparator output when after a delay the voltage at this node is stabilised. As the comparator output level is HIGH in this situation the output level of the latch remains HIGH and the Q_n output LOW. When the level at V_{inn} reaches the V_{rL} level the

output level of the comparator turns to LOW and so the output level of the transparent latch. The level at Q_n turns to HIGH. In this instant the reference input of the comparator is switched over from V_{rL} to V_{rH} leaving the output voltage at Q_n constant. When the level at V_{inn} reaches about 1 V the DC power of the comparator is switched OFF again. The control of the output circuit is switched over from the comparator output to the digital detector output which voltage level is LOW in this situation. During this action the level at Q_n remains HIGH. The function of the circuit is a Schmitt-trigger of which the V_{T+} and V_{T-} levels can be set at the V_{rH} and V_{rL} inputs. These levels can be varied from $\approx$1 V up to $\approx V_{CC} - 1$ V. so the maximum obtainable hysteresis is $\approx V_{CC} - 2$ V. The on-and off switching of the power and the stabilization of the comparator needs time, therefore the minimum applicable rise- and fall time of the input signal are limited when the maximum accuracy is required. When during the rise time of the input signal the input level has past the V_{LL} level, the power starts to switch on. Only when the comparator is stable at the moment that the input signal passes the V_{rH} level the comparator has its true delay and its optimal accuracy. When the V_{rH} level is passed before the comparator is stable an extra delay occurs due to the switching of the power and the accuracy of the comparator is less. At the positive going edge, this extra delay depends on the difference between V_{LL} and V_{rH} and the rise time of the signal. This is shown in Fig.8, where by means of curves A and B t_{PHL} is plotted at V_{rH} is 1.15 V and 2.25 V respectively and V_{CC} = 4.5 V. As with curve a V_{rH} is very close to V_{LL} the part of the input edge that is available for switching the power on is very small. This causes that only at a rise time > 500 ns/V the delay will be equal to the true delay of the comparator. At V_{rH} = 2.25 V this situation is reached already at a rise time of 120 ns/V. At a very short rise time, the major part of the propagation delay is due to the switching time of the power. At the negative going edge, the power is switched on when the level V_{HH} is passed so the extra delay depends on the difference between V_{HH} and V_{rL} and the fall time of the signal. This situation is referred to with curves C and D where t_{PLH} is drawn against the fall time of the input signal. With curve C V_{rL} is 3.25 V which is on the edge of the operating region. Curve D corresponds with a V_{rL} value of 2.25 V. For linear input edges the recommended minimum rise time at V_{CC} = 4.5 V or 6 V is 100 ns/V and at V_{CC} = 3 V, 300 ns/V. For non-linear input signals, during the rising edge there must be a delay between the time at which the V_{LL} level is passed and the time at which the V_{rH} level is passed. This delay will be dependent on the V_{CC} level and the amplitude of the overdrive of V_{LL}. There is no limitation on the signal slope during the passing of the levels. For the same reasons, during the falling edge there must be a delay between the time at which the V_{HH} level is passed and the time at which the V_{rL} level is passed. A possible application of the circuit is as precision oscillator see Fig.6. The operating frequency is:

$$f = \frac{1}{t_{RC} + 2 \times (t_{PLH} + t_{PHL})}$$

where $t_{RC} = 2 \times \ln\left(\frac{V_{CC} - V_{rL}}{V_{CC} - V_{rH}}\right) \times RC$

The operation in the comparator mode

The IC can be applied as a comparator by connecting the V_{rL} input to GND and adjusting the level at V_{rH} to the wanted detection level see Fig.7. In this mode the DC power of the comparator is always on and the output stage is set to non-inverting. The function table for this operation mode is given in table 2.

Table 2 Function table for Comparator mode

INPUT	LE	$\overline{OE}$	Q_n
$V_{inn} < V_{ref}$	L	L	L
$V_{inn} > V_{ref}$	L	L	H
V_{inn} = X	H	L	Q_{n-1}
V_{inn} = X	X	H	Z

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   Z = high impedance OFF-state
   X = don't care

The fact that the power is always on offers the feature of a more extended operation region of the V_{rH} input voltage which is at a V_{CC} of 4.5 V from 1.1 V up to 4.2 V see also Fig.12. A hysteresis of about 50 mV is required to overcome oscillations. This has to be performed by means of a few external resistors. The DC power in this operation mode at V_{CC} = 4.5 V is typical 2 mW per function. A curve showing t_{PD} as a function of the overdrive is given in Fig.11. A possible diagram for a bargraph display is shown in Fig.10.

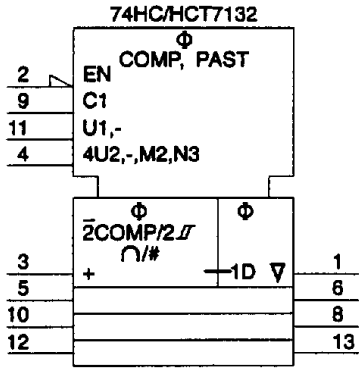


Fig.3 IEC Logic symbol.

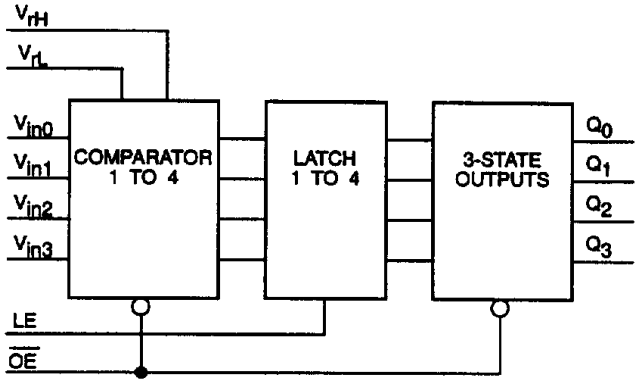


Fig.4 Functional diagram.

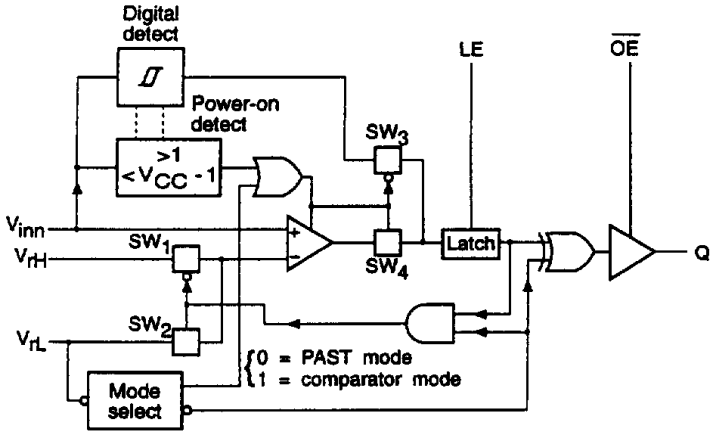


Fig.5 Logic diagram.

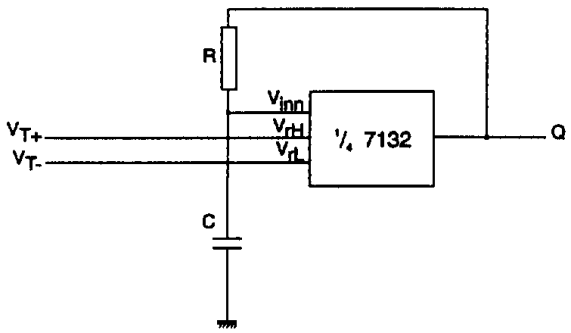


Fig.6 ¼ 7132 Precision oscillator application.

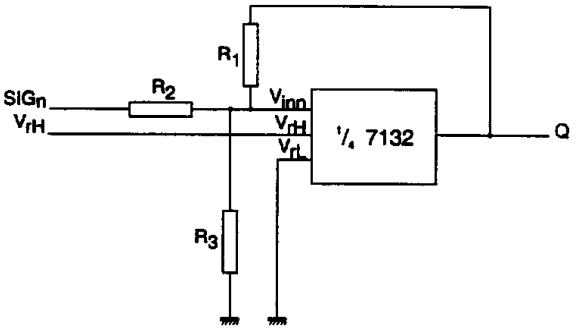


Fig.7 ¼ 7132 Comparator application.

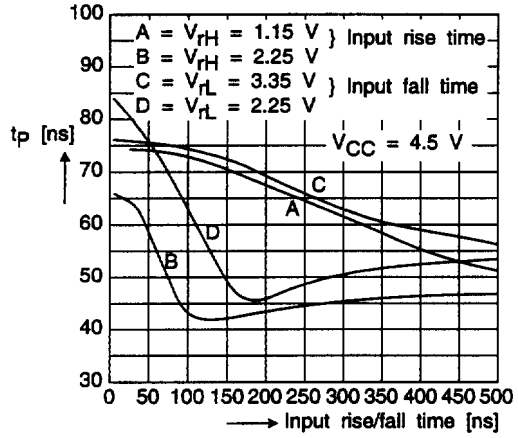


Fig.8 Waveforms applied during measurements see Fig.13

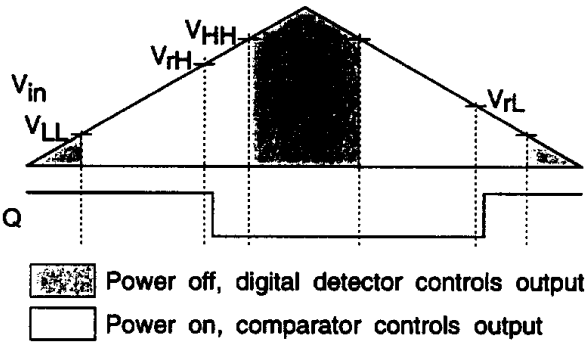


Fig.9 Input voltage switching levels.

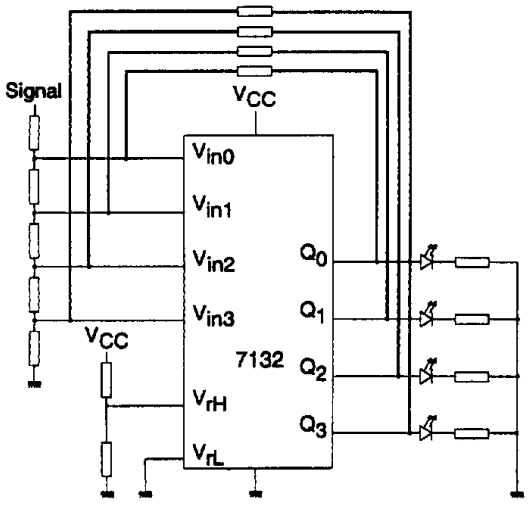


Fig.10 Possible circuit for a bargraph.

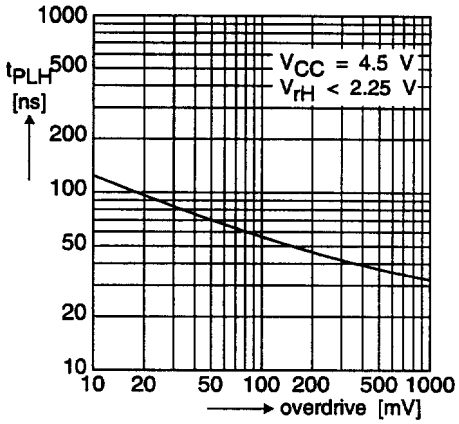


Fig.11 Curve showing the t_{PLH}/t_{PHL} as a function of the overdrive for the comparator application. Waveforms applied during measurements see Fig.13.

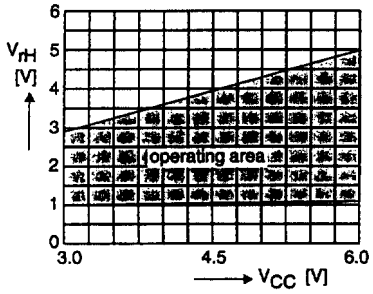


Fig.12 Operating area for V_{rH} in comparator mode.

DC CHARACTERISTICS FOR 74HC

Output capability: Bus driver
I_{CC} category: MSI
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I (V)	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.				
V_{CC}	DC supply voltage	3.0	–	6.0	3.0	6.0	3.0	6.0	V			
V_{err}	Error on trip level	–	±20	–	–	–	–	–	mV	3.0 to 6.0		over V_{ref} range
V_{LL}	V_{IN} at which power for comparator is switched ON	0.4	0.7	0.9	0.4	0.9	0.4	0.9	V	3.0 to 6.0		Fig.9
V_{HH}	V_{IN} at which power for comparator is switched OFF	V_{CC} – 1.1	V_{CC} – 0.9	V_{CC} – 0.5	V_{CC} – 1.1	V_{CC} – 0.5	V_{CC} – 1.1	V_{CC} – 0.5	V	3.0 to 6.0		Fig.9
I_{CC}	active supply current. Comparator mode	–	2.0	3.4	–	–	–	–	mA	4.5		V_{rH} = 2.25 V V_{rL} = 0 V
I_{CC}	supply current. PAST mode	–	30	50	–	–	–	–	µA	4.5		V_{rH} = 3 V V_{rL} = 1.5 V
I_{CC}	quiescent supply current	–	–	8	–	80	–	160	µA	6.0		$V_{rH} = V_{rL} = V_{CC}$ V_{IN} = 0 V
PAST mode												
V_{rH}	HIGH reference level, (V_{T+})	1.15	–	V_{CC} – 1.2	1.15	V_{CC} – 1.2	1.15	V_{CC} – 1.2	V	3.0 to 6.0		
V_{rL}	LOW reference level, (V_{T-})	1.1	–	V_{CC} – 1.25	1.1	V_{CC} – 1.25	1.1	V_{CC} – 1.25	V	3.0 to 6.0		
V_{Hmin}	Minimum hysteresis voltage, ($V_{rH} - V_{rL}$)	–	50	–	–	–	–	–	mV	3.0 to 6.0		
COMPARATOR mode												
V_{rHmin}	minimum referene level	–	0.6	–	–	–	–	–	V	4.5		over V_{ref} range
V_{rHmax}	maximum reference level	–	V_{CC}	–	–	–	–	–	V	4.5		over V_{ref} range

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_{rH}	V_{rL}	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.					
t_{PHL}	propagation delay V_{inn} to Q_n; PAST mode	– – –	80 50 40	– – –	– – –	– – –	– – –	– – –	ns	3.0 4.5 6.0	1.67 3.00 4.00	1.50 1.50 2.00	t_r = 300 ns/V t_r = 100 ns/V t_r = 100 ns/V Fig.13
t_{PLH}	propagation delay V_{inn} to Q_n; PAST mode	– – –	80 50 40	– – –	– – –	– – –	– – –	– – –	ns	3.0 4.5 6.0	1.67 3.00 4.00	1.50 1.50 2.00	t_r = 300 ns/V t_f = 100 ns/V t_f = 100 ns/V Fig.13
t_{PHL}	propagation delay V_{inn} to Q_n; Comparator mode	– – –	100 60 50	– – –	– – –	– – –	– – –	– – –	ns	3.0 4.5 6.0	V_{CC}/2	0.00	Fig.14, overdrive: 100 mV
t_{PLH}	propagation delay V_{inn} to Q_n; Comparator mode	– – –	80 50 40	– – –	– – –	– – –	– – –	– – –	ns	3.0 4.5 6.0	V_{CC}/2	0.00	Fig.14, overdrive: 100 mV
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	– – –	35 23 18	– – –	– – –	– – –	– – –	– – –	ns	3.0 4.5 6.0			Fig.15
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	– – –	22 15 13	– – –	– – –	– – –	– – –	– – –	ns	3.0 4.5 6.0			Fig.17
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	– – –	22 17 14	– – –	– – –	– – –	– – –	– – –	ns	3.0 4.5 6.0			Fig.17
t_{THL}/t_{TLH}	output transition time	– – –	25 10 9	– – –	– – –	– – –	– – –	– – –	ns	3.0 4.5 6.0			Fig.13
t_W	LE pulse width LOW	– – –	12 6 5	– – –	– – –	– – –	– – –	– – –	ns	3.0 4.5 6.0			Fig.15
t_{su}	set-up time V_{inn} to LE	–	30	–	–	–	–	–	ns	4.5	3.00	1.50	Fig.16, for V_{INn}: $t_r = t_f$ = 180 ns
t_h	hold time V_{inn} to LE	–	–30	–	–	–	–	–	ns	4.5 6.0	3.00	1.50	Fig.16, for V_{INn}: $t_r = t_f$ = 180 ns

DC CHARACTERISTICS FOR 74HCT

Output capability: Bus driver
I_{CC} category: MSI
Voltages are referenced to GND (ground = 0 V)

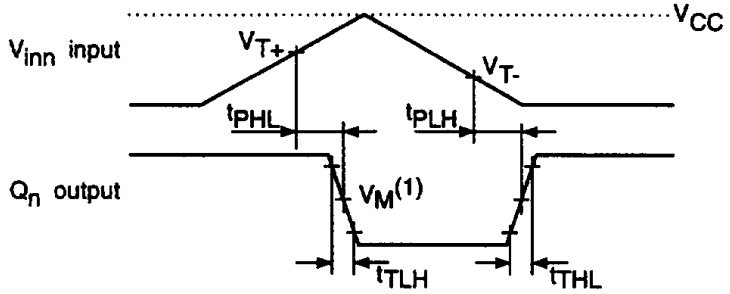
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I (V)	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.				
V_{CC}	DC supply voltage	4.5	–	5.5	4.5	5.5	4.5	5.5	V			
V_{err}	Error on trip level	–	±20	–	–	–	–	–	mV	4.5 to 5.5		over V_{ref} range
V_{LL}	V_{IN} at which power for comparator is switched ON	0.4	0.7	0.9	0.4	0.9	0.4	0.9	V	4.5		Fig.9
V_{HH}	V_{IN} at which power for comparator is switched OFF	3.4	3.6	4.0	3.4	4.0	3.4	4.0	V	4.5		Fig.9
I_{CC}	active supply current. Comparator mode	–	2.0	3.4	–	–	–	–	mA	4.5		V_{rH} = 2.25 V V_{rL} = 0 V
I_{CC}	supply current. PAST mode	–	30	50	–	–	–	–	µA	4.5		V_{rH} = 3 V V_{rL} = 1.5 V
I_{CC}	quiescent supply current	–	–	8	–	80	–	160	µA	4.5		$V_{rH} = V_{rL} = V_{CC}$ V_{IN} = 0 V
PAST mode												
V_{rH}	HIGH reference level, (V_{T+})	1.05	–	V_{CC} – 1.20	1.05	V_{CC} – 1.20	1.05	V_{CC} – 1.20	V	4.5 to 5.5		
V_{rL}	LOW reference level, (V_{T-})	1.00	–	V_{CC} – 1.25	1.00	V_{CC} – 1.25	1.00	V_{CC} – 1.25	V	4.5 to 5.5		
V_{Hmin}	Minimum hysteresis voltage, ($V_{rH} - V_{rL}$)	–	50	–	–	–	–	–	mV	4.5 to 5.5		
COMPARATOR mode												
V_{rHmin}	minimum reference level	–	0.6	–	–	–	–	–	V	4.5		over V_{ref} range
V_{rHmax}	maximum reference level	–	V_{CC}	–	–	–	–	–	V	4.5		over V_{ref} range

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

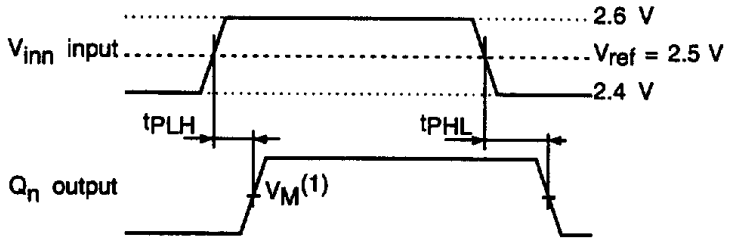
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_{rH}	V_{rL}	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.					
t_{PHL}	propagation delay V_{inn} to Q_n; PAST mode	–	50	–	–	–	–	–	ns	4.5	3.00	1.50	Fig.13, t_r = 100 ns/V
t_{PLH}	propagation delay V_{inn} to Q_n; PAST mode	–	50	–	–	–	–	–	ns	4.5	3.00	1.50	Fig.13, t_r = 100 ns/V
t_{PHL}	propagation delay V_{inn} to Q_n; Comparator mode	–	60	–	–	–	–	–	ns	4.5	V_{CC}/2	0.00	Fig.14, overdrive: 100 mV
t_{PLH}	propagation delay V_{inn} to Q_n; Comparator mode	–	50	–	–	–	–	–	ns	4.5	V_{CC}/2	0.00	Fig.14, overdrive: 100 mV
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	–	28	–	–	–	–	–	ns	4.5			Fig.15
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	–	20	–	–	–	–	–	ns	4.5			Fig.17
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	–	22	–	–	–	–	–	ns	4.5			Fig.17
t_{THL}/t_{TLH}	output transition time	–	10	–	–	–	–	–	ns	4.5			Fig.13
t_W	LE pulse width LOW	–	6	–	–	–	–	–	ns	4.5			Fig.15
t_{su}	set-up time V_{inn} to LE	–	25	–	–	–	–	–	ns	4.5	3.00	1.50	Fig.16, for V_{INn}: $t_r = t_f$ = 180 ns
t_h	hold time V_{inn} to LE	–	–25	–	–	–	–	–	ns	4.5	3.00	1.50	Fig.16, for V_{INn}: $t_r = t_f$ = 180 ns

AC WAVEFORMS



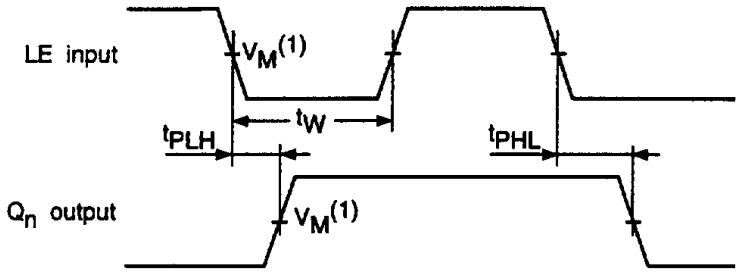
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.13 Waveforms showing the input (V_{inn}) to output Q_n propagation delays for PAST mode.



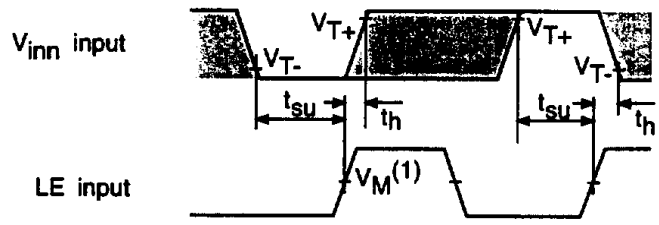
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.14 Waveforms showing the input (V_{inn}) to output Q_n propagation delays for Comparator mode at V_{rL} = 0 V and V_{ref} = ½ V_{CC}.



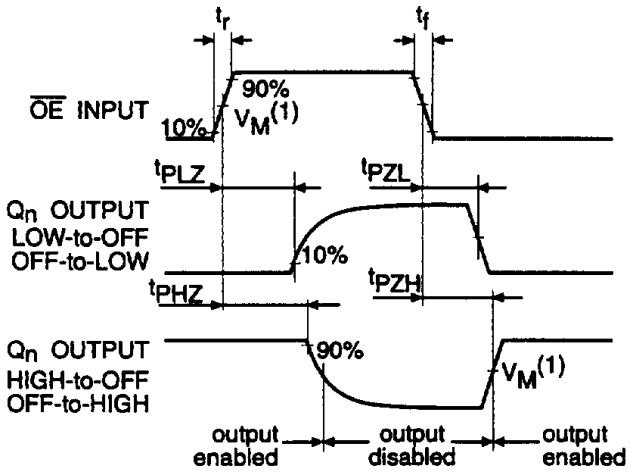
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.15 Waveforms showing the input (LE) to output Q_n propagation delays for Comparator mode.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.16 Waveforms showing the input set-up and hold times for V_{inn} input to LE input.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.17 Waveforms showing the 3-state enable and disable times.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.