IXF3208

Octal T1/E1/J1 Framer with Intel® On-Chip PRM

Advance Datasheet

The Intel® IXF3208 with Intel® On-Chip Performance Report Messaging (Intel® On-Chip PRM) is an octal framer for T1/E1/J1 and ISDN primary rate interfaces operating at 1.544 Mbps or 2.048 Mbps. Each of the eight framers operates independently, allowing each channel to be individually configured for T1, E1, or J1 operation. Configuration is handled using the Intel supplied Application Program Interface (API). Each framer consists of a receive and transmit framer and receive and transmit slip buffer. Direct interface to the Intel® IXF3208 with the Intel® LXT3108 or the Intel® LXT384 octal LIUs or LIUs of other manufacturers is supported. To comply with ANSI T1.231, T1.403 and ETSI G.826 specifications, comprehensive performance monitoring is done on-chip providing Intel PRM. The Intel IXF3208 is the ideal framer for voice and data applications, as it incorporates 24 independent HDLC controllers that can be allocated to any time slot in the eight T1/E1/J1 links it supports. This greatly simplifies the implementation of scalable GR-303 and V5.2 interfaces. The Intel IXF3208 has an eight-bit bus supporting both Intel and Motorola microprocessor interfaces. A flexible TDM interface supports bus rates from 1.544 MHz to 16.384 MHz and industry-standard buses including MVIP, H-MVIP, H.100, and CHI. The Intel IXF3208 is in a 17 mm x 17 mm PBGA package to enable the design of high-port density, multi-service line cards.

Product Features

- Octal T1/E1/J1 Framer
- Software selectable – fully independent T1/E1/J1 operation
- Support T1/E1/J1 standards:
  - T1-SF, ESF, SLC-96
  - E1-PCM30, G.704, G.706, G.732 ISDN PRI
  - J1-SF, J1-ESF
- Programmable transmit/receive slip buffers
- On-Chip Intel® Performance Report Messaging (Intel® PRM) per ANSI T1.231, T1.403 and ITU G.826
- 24 fully independent HDLC controllers with 128 byte transmit/receive FIFOs, support GR-303 and V5.1/5.2 standards
- FDL Support:
  - DL support for ESF per ANSI T1.403 or AT&T TR54016 (T1/J1)
  - DDL bit access for SLC-96
  - Sa bit access for E1
- 256 PBGA package, 17 mm x 17 mm
- Operating temperature -40°C to 85°C
- Diagnostics:
  - BERT – generators and analyzers for extensive error testing on chip at DS-0, DS-1 and E1 rates
    - Pseudo random and programmable bit sequence generator and monitoring
  - Per link diagnostics and loopbacks
- Programmable system backplane data rates operating at 1x/2x/4x and 8x of T1/E1 data rates. Supports: MVIP, H-MVIP, H.100, and CHI
- Support for fractional T1/E1
- Signaling:
  - Support T1/E1 CAS and T1/E1 CCS
  - Signaling state change indication
  - Signaling freeze/debounce per DS-1
  - Signaling force per DS-0
- Red/Yellow/AIS alarm indication
- Intel/Motorola 8-bit microprocessor interface
- Industry standard P1149.1 JTAG test port
- Low power 1.8/3.3V CMOS technology with 5V tolerant I/Os

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Revision History

Revision	Date	Description
-001	06/15/01	Initial Issue.
-002	11/21/01	Modified and added chapters 2 -26.
-003	01/25/02	Modified chapters 1 - 3; Added chapters 14 and 15; Relocated and modified chapters 4 - 13 and 16 - 27.

Introduction 1

1.1 Description

The IXF3208 is an eight-channel framer for T1/E1/J1 and Integrated Service Digital Network (ISDN) primary rate interfaces operating at 1.544 Mbps or 2.048 Mbps. All framers are completely independent and each port can be configured for either T1/E1/J1 operation. An 8 bit microprocessor interface is provided that supports both Intel® and Motorola microprocessors. The internal registers are directly addressable through the microprocessor interface. Extensive support to the data link channels (SLC-96 DDL, FDL, Sa bits, CCS) are also provided.

IXF3208 offers Intel On-Chip Performance Report Message (Intel On-Chip PRM). The On-Chip PRM processing is done automatically with data stored on the device. An internal database with performance monitor units (accessible by a host) provides status and performance parameters already integrated and filtered according to the available configurations. This feature off loads the external processor from the handling of the parameters associated with the functions of this device.The standards supported are ANSI T1.231 (T1) and ITU G.826 (E1). Support is also provided for ETSI ETS 300 011 and ETS 300 233.

Each of the channels supports T1-D4 SF, T1-ESF T1-SLC-96, J1-12, J1-24, E1-FAS/NFAS, E1-CRC4, E1-CAS, E1-CRC4/CAS, G.704, and G.706 frame structures. Cyclic Redundancy Check (CRC) inter-working as defined in ITU G.706 is also supported.

Each port is independent in timing and format from the others. For plesiochronous applications, independent two-frame deep slip buffers are provided in both transmit and receive directions. Smaller elastic store depths are available for minimum delay applications.

The system backplane can be configured to handle different rates and waveforms. The backplane has data, signaling, and framing indication pins. The clock can be run at speeds of 1x, 2x, 4x, and 8x of the nominal value. The Pulse Code Modulation (PCM) highway can be configured to handle different industry standard buses such as MVIP, H-MVIP, IOM/GCI, CT-Bus (H.100), SCSA (S.100), and Concentration Highway Interface (CHI) bus interfaces.

Test and diagnostic functions are provided through a full set of loopbacks and a Bit Error Rate Test (BERT) module. Local Loopback, Dual Loopback, Payload Loopback, Line Loopback, and per-time slot loopbacks are available. The BERT module can handle simultaneously eight generators and analyzers. Any generator and analyzer is available for each port and can be set to any time slot or set of time slots. Subrate testing is also available using a mask to define which bits in the time slots are tested. The generators and analyzers can be set to operate on either the line or system sides. Additionally, Bipolar Pulse Violations (BPVs) frame or CRC errors can be inserted in the Tx line direction.

Signaling support, robbed bit or TS16CAS is provided for all eight ports. Signaling information is available either from the system backplane bus or internally selected from a table that can be accessed by the external host. The signaling at the Tx direction on the system backplane can be sent to the line side. Also, the user can set a table of signaling values to be sent in any direction. The freeze and de-bouncing functions are programmable. Four, nine, and sixteen signaling states are available.

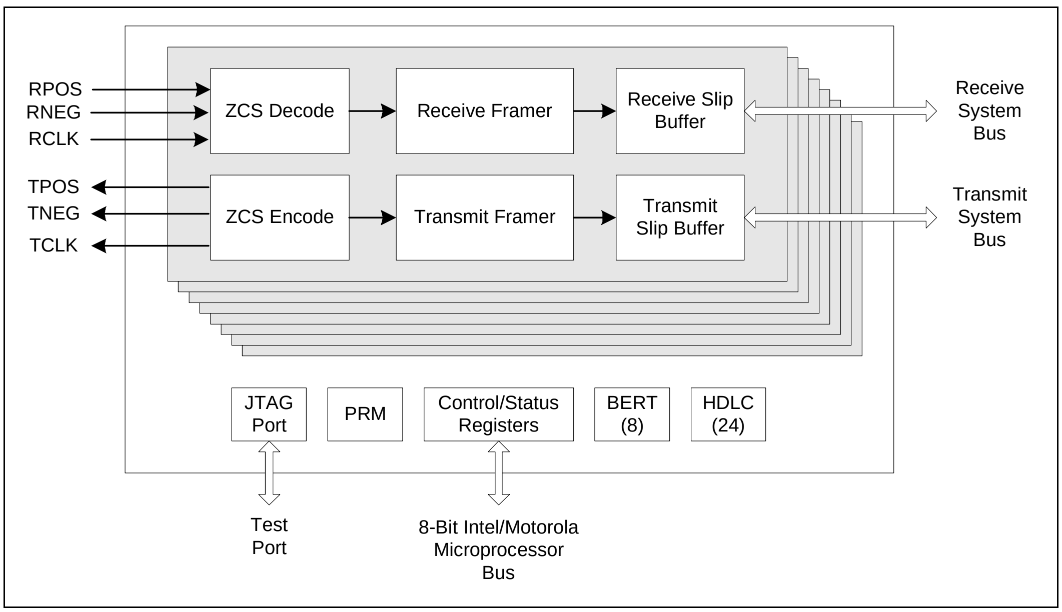
Extensive support to the data link channels (DDL, FDL) is provided. The user can select the Sa bits to use in the E1 stream to handle the data link channel. Performance Report Messages (PRM) can be generated and detected automatically. Once a T1.403 PRM is received, the internal far end database is updated and the external host could be informed. A PRM message can be sent when requested by the host or on a one second basis, generated internally.

An internal database with performance monitor units is generated by the internal circuitry. The database holds near end and far end parameters in accordance with ANSI T1.231, G.826, and G.821. The external host can access this database.

Alarms and error conditions at DS1/E1 levels are detected and reported. These include AIS, LOS, yellow, TS16 AIS. Integration times are applied to the detected defects in order to provide the failure indications (LOS, LOF, AIS failures). A user defined pattern, AIS or AUXP can be sent to the backplane as a consequent action on the reception of defect conditions. Likewise, AIS, AUXP, REBE or codewords can be sent to the line side as a consequent action.

The Intel IXF3208 interfaces directly with the Intel LXT3108 Octal, T1/E1/J1 Long Haul/Short Haul (LH/SH), Line Interface Unit (LIU), or the Intel LXT384 Octal T1/E1/J1 Short Haul (SH) LIU.

Figure 1. IXF3208 Block Diagram



1.2 Reference Material

In addition to the Intel IXF3208 Datasheet, please refer to the:

- Intel® IXF3208 API — Software Developer's Manual (Order Number 249880)
- Intel® IXF3208 Evaluation Board — Developer's Manual (Order Number 250272)
- Intel® IXF3208 Memory Map — Developer's Manual (Order Number 250280)
- Intel® IXF3208 Quick Start Guide — Developer's Manual (Order Number 250455)
- Intel® IXF3208 Basic Configuration — Developer's Manual (Order Number 250537)
- Intel® IXF3208 Device Drivers — Developer's Manual (Order Number 250538)
- Intel® IXF3208 FAQ (Order Number 250193)
- Intel® IXF3208 HDLCs for Voice Over Packet — Application Note (Order Number 250194)
- Intel® IXF3208 HDLCs for V5.x & GR-30 — Application Note (Order Number 250195)
- Intel® IXF3208 Interfacing with the LXT384 — Application Note (Order Number 250196)
- Intel® IXF3208 BERTs — Application Note (Order Number 250534)
- Designing in Intel® IXF3208 Over Combos — Application Note (Order Number 250535)
- Intel® IXF3208 Device Drivers — Application Note (Order Number 250536)

Figure 2. LXT3108/IXF3208 System Interface

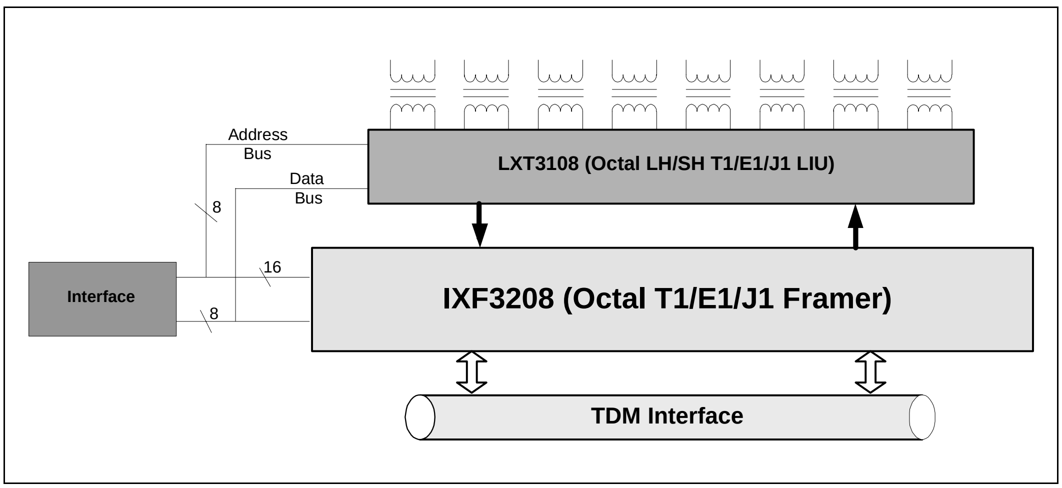
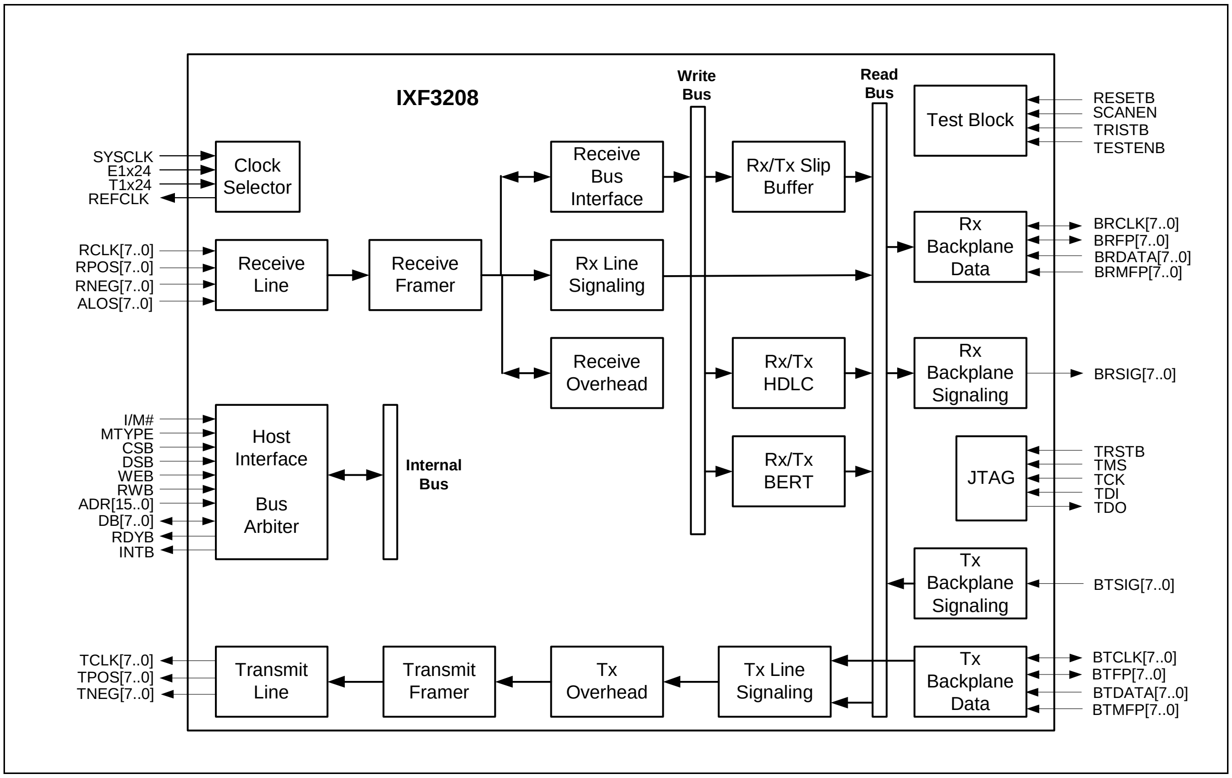


Figure 3. IXF3208 Detailed Block Diagram



Applications

- Voice over packet gateways
- Integrated Multi-service Access Platforms (IMAPs)
- Integrated Access Devices (IADs)
- Inverse Multiplexing for ATM (IMA)
- Wireless base stations
- Routers
- Frame relay access devices, CSU/DSU equipment

1.3 T1/E1 Nomenclature

This section describes the terminology and conventions used throughout this document.

The nomenclature in this document follows telecommunication industry standard conventions, i.e., bit, channel (timeslot), and frame numbering increase sequentially with time. In the case of bit ordering, unless otherwise stated, the Most Significant Bit (MSB) is transmitted first and is designated Bit 1.

Both T1 and E1 conventions define the numbering of bits within a timeslot to be designated “Bit 1” through “Bit 8,” with Bit 1 defined as the MSB.

T1 bits within a frame are numbered from 1 to 193, with bit 1 being the “F’ (framing) bit. E1 bits within a frame are numbered from 1 to 256, with bits 1 to 8 occupying the FAS/NFAS Word timeslot (timeslot 0).

The T1 convention is to sequentially number channels (timeslots) beginning with “1” i.e., the first channel in a T1 frame is frame number 1. The E1 convention is to number this timeslot “0” i.e., the first timeslot in a E1 frame is timeslot number 0.

In multiframe structures, the T1 convention is to sequentially number frames beginning with “1” i.e., the first frame in a T1 multiframe is frame number 1. The E1 convention is to number this frame “0” i.e., the first frame in a E1 multiframe is frame number 0.

In T1 terminology, “Yellow Alarm” and “Remote Alarm Indication” (RAI) are synonymous. Also, “Blue Alarm” and “Alarm Indication Signal” (AIS) are synonymous.

The terms, “Out Of Frame” (OOF) and “Loss Of Frame” (LOF) are used interchangeably in this document.

1.4 IXF3208 Nomenclature

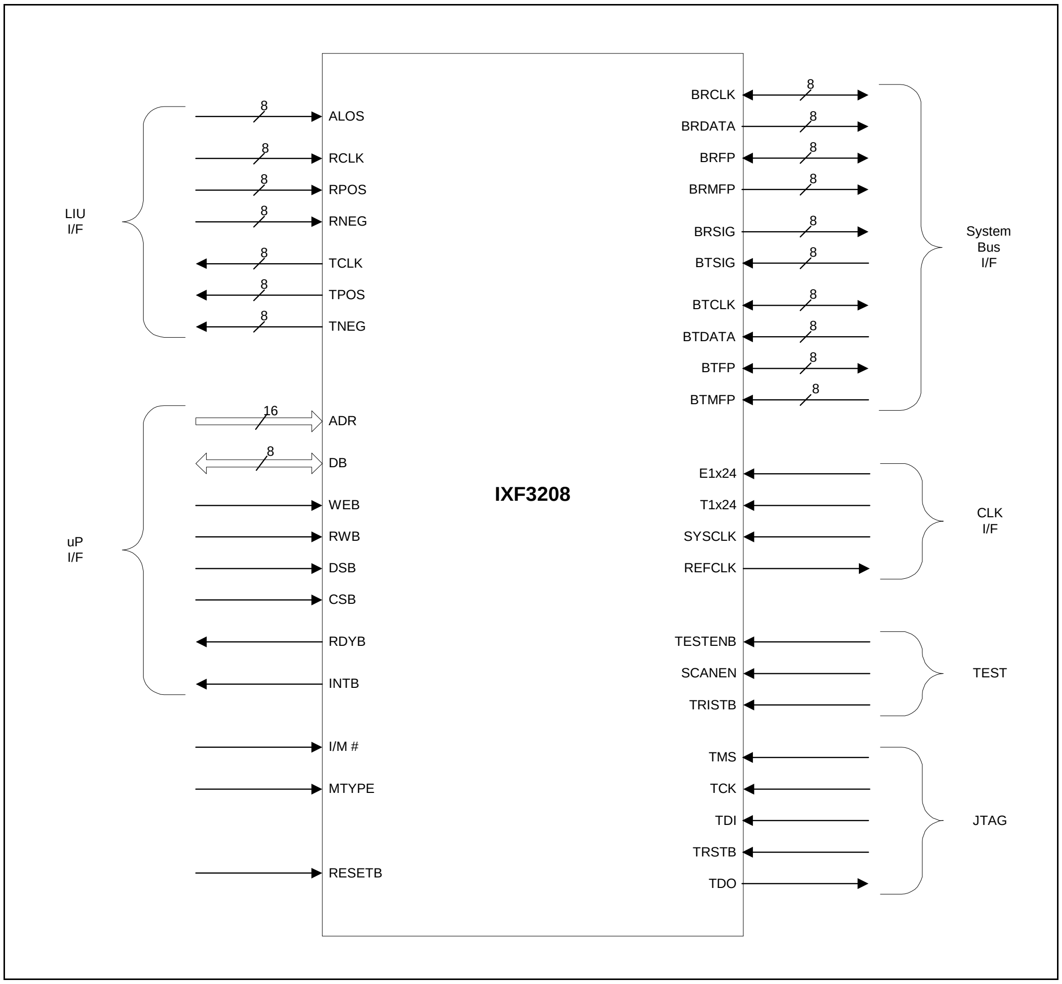
The IXF3208 is an octal device, meaning that it supports up to eight T1/E1/J1 links. The links are numbered sequentially, beginning with zero (0) and ending with seven (7). The time slots are numbered 0 to 23 for T1 cases and 0 to 31 for E1 cases. Note that T1 channel 1 corresponds to TS0, channel 2 to TS1, etc.

A link is defined as the standard 4 wire receive/transmit pair T1/E1/J1 interface. The terms *link*, *port*, and *span* may be used interchangeable in this document.

IXF3208 Signal Description 2

The IXF3208 is packaged in a 256 PBGA package, with 17 mm X 17 mm foot print size, and ball pitch of 1.0 mm. The following diagram describes the logical symbol. Mechanical information for this package is described in Section 26, “Mechanical Specifications” on page 169. See “Ball Assignment” on page 168.

Figure 4. IXF3208 Logical Symbol



2.1 Ball Description

Table 1. IXF3208 Ball Description

PBGA	Ball Name	I/O	Description
Line Interface			
C3 D2 B16 A14 R13 T16 N3 T3	RCLK7 RCLK6 RCLK5 RCLK4 RCLK3 RCLK2 RCLK1 RCLK0	I I I I I I I I	Receive clock input from LIU. This clock is used to clock data to the receive side framer. Data can be clocked in on either edge, depending on the channel selection. Each clock is independently controlled.
B3 D3 C14 A13 T13 R15 R1 T4	RPOS7 RPOS6 RPOS5 RPOS4 RPOS3 RPOS2 RPOS1 RPOS0	I I I I I I I I	Receive positive data input from LIU. Sampled on the selected edge of the RCLK to receive data for the receive side framer (default is falling edge). When working in unipolar mode, this is the data pin that carries the information.
A2 C1 C15 C13 P12 T15 P2 R4	RNEG7 RNEG6 RNEG5 RNEG4 RNEG3 RNEG2 RNEG1 RNEG0	I I I I I I I I	Receive negative data input from LIU. Sampled on the selected edge of the RCLK to receive data for the receive side framer (default is falling edge). When working in unipolar mode, this pin carries other information. See the description of the configuration bits in the Memory Map.
C2 E2 D15 B15 R14 N14 N2 R2	TCLK7 TCLK6 TCLK5 TCLK4 TCLK3 TCLK2 TCLK1 TCLK0	O O O O O O O O	Transmit clock output to LIU. This clock is used to clock the data from the transmit side framer. The edge to deliver data can be selected to rising or falling.
A1 E3 D14 A15 T14 R16 P3 T2	TPOS7 TPOS6 TPOS5 TPOS4 TPOS3 TPOS2 TPOS1 TPOS0	O O O O O O O O	Transmit positive data output to LIU. This signal is updated on the selected edge of the TCLK to transmit positive bipolar data (Default is rising edge). When working in unipolar mode, this pin carries the data to transmit.

Table 1. IXF3208 Ball Description

PBGA	Ball Name	I/O	Description
B2 D1 C16 B14 P13 P15 P1 R3	TNEG7 TNEG6 TNEG5 TNEG4 TNEG3 TNEG2 TNEG1 TNEG0	O O O O O O O O	Transmit negative data output to LIU. Updated on the selected edge of the TCLK to transmit negative bipolar data (Default is rising edge). When working in unipolar mode, this pin carries other information. See the description of the configuration bits in the Intel IXF3208 Memory Map æ Developer's Manual (Order Number 250280).
Backplane Interface			
T12 K15 H12 F14 E10 C8 C6 D4	BRCLK7 BRCLK6 BRCLK5 BRCLK4 BRCLK3 BRCLK2 BRCLK1 BRCLK0	I/O I/O I/O I/O I/O I/O I/O I/O	Receive clock at the backplane. This signal can be run at 1x, 2x, 4x and 8x the base clock rate (1.544 MHz, 2.048 MHz, 1.536 MHz). This allows replication and concentration modes, as well as HMVIP and CHI modes to be supported.
R11 K14 H13 F13 B11 A8 A6 B4	BRDATA7 BRDATA6 BRDATA5 BRDATA4 BRDATA3 BRDATA2 BRDATA1 BRDATA0	O O O O O O O O	Receive data at the backplane. This pin normally carries data from the time slots. However in a CHI mode, it can carry data and signaling information, in an interleaved fashion. The clock edge to deliver this data can be configured to rising or falling.
P11 L16 H16 F15 D11 D8 C7 A3	BRFP7 BRFP6 BRFP5 BRFP4 BRFP3 BRFP2 BRFP1 BRFP0	I/O I/O I/O I/O I/O I/O I/O I/O	Receive frame pulse at the backplane. The clock edge to deliver or sample this signal can be configured to rising or falling. Additional parameters that can be configured is the delay from bit 0, the polarity and the width of the active pulse.
T11 M16 J13 F16 A11 D9 B7 C5	BRMFP7 BRMFP6 BRMFP5 BRMFP4 BRMFP3 BRMFP2 BRMFP1 BRMFP0	O O O O O O O O	Receive multi-frame pulse at the backplane. The parameters selected for the FP signal are used to deliver this signal (delay, width, polarity).

Table 1. IXF3208 Ball Description

PBGA	Ball Name	I/O	Description
P10	BRSIG7	O	Rx signalling output at the backplane. The output signaling bits are in PCM format. The clock edge and rate selected for BRDATA are used to deliver the signaling information.
M13	BRSIG6	O	
J15	BRSIG5	O	
G15	BRSIG4	O	
C11	BRSIG3	O	
C9	BRSIG2	O	
D6	BRSIG1	O	
B5	BRSIG0	O	
R10	BTCLK7	I/O	Transmit clock at the backplane. This signal can be run at 1x, 2x, 4x and 8x the base clock rate (1.544 MHz, 2.048 MHz, 1.536 MHz). This allows replication and concentration modes, as well as HMVIP and CHI modes to be supported.
N13	BTCLK6	I/O	
J14	BTCLK5	I/O	
G16	BTCLK4	I/O	
D13	BTCLK3	I/O	
B9	BTCLK2	I/O	
E7	BTCLK1	I/O	
A4	BTCLK0	I/O	
T10	BTDATA7	I	Transmit data at the backplane. This pin normally carries data from the time slots, however in a CHI mode, it can carry data and signaling information, in an interleaved fashion. The clock edge to sample this data can be configured to rising or falling.
M14	BTDATA6	I	
J16	BTDATA5	I	
G14	BTDATA4	I	
A12	BTDATA3	I	
A9	BTDATA2	I	
A7	BTDATA1	I	
A5	BTDATA0	I	
T9	BTFP7	I/O	Transmit frame pulse at the backplane. The clock edge to deliver or sample this signal can be configured to rising or falling. Additional parameters that can be configured are the delay from bit 0, the polarity and the width of the active pulse.
L15	BTFP6	I/O	
L13	BTFP5	I/O	
G13	BTFP4	I/O	
B12	BTFP3	I/O	
D10	BTFP2	I/O	
D7	BTFP1	I/O	
D5	BTFP0	I/O	
P9	BTMFP7	I	Transmit multi-frame pulse at the backplane. The parameters selected for the FP signal are used to sample this signal (delay, width, polarity).
L14	BTMFP6	I	
K13	BTMFP5	I	
H14	BTMFP4	I	
C12	BTMFP3	I	
C10	BTMFP2	I	
E8	BTMFP1	I	
E6	BTMFP0	I	

Table 1. IXF3208 Ball Description

PBGA	Ball Name	I/O	Description
R9 M15 K16 H15 D12 B10 B8 B6	BTSIG7 BTSIG6 BTSIG5 BTSIG4 BTSIG3 BTSIG2 BTSIG1 BTSIG0	I I I I I I I I	Transmit signaling input at the backplane. When enabled, this input will sample the signaling bits for insertion into the out going PCM T1/E1 data stream. The clock edge and rate selected for BTDATA is also used to sample the signaling information.
C4 B1 A16 B13 R12 N11 T1 P4	ALOS7 ALOS6 ALOS5 ALOS4 ALOS3 ALOS2 ALOS1 ALOS0	I I I I I I I I	Loss of Signal Indicator from LIU. This is an indicator that can be provided by an external LIU to inform of an LOS condition. This indication is sampled, stored and then an internal indicator can be set and propagated to the external host processor.
Host Interface			
G2 G1 G3 H4 H1 H3 H2 J1 J3 K1 J2 J4 K4 K3 L1 K2	ADR15 ADR14 ADR13 ADR12 ADR11 ADR10 ADR9 ADR8 ADR7 ADR6 ADR5 ADR4 ADR3 ADR2 ADR1 ADR0	I I I I I I I I I I I I I I I I	The 16 bit microprocessor address lines enable the user to read or write any internal register or RAM region defined in the memory map section of the Developers Manual.
N1 M3 M2 N4 M1 L3 M4 L2	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0	I/O I/O I/O I/O I/O I/O I/O I/O	The eight bit data bus enables the user to transfer data to read or write transactions. Three stated when not in a transfer or when the transfer is a write process.
N12	I/M #	I	Intel/Motorola I/M# - Micro processor interface mode I/M# = 1 selects Intel I/M# = 0 selects Motorola

Table 1. IXF3208 Ball Description

PBGA	Ball Name	I/O	Description
F1	MTYPE	I	MTYPE - microprocessor type selection MTYPE - 0 selects 68K family (68302) MTYPE - 1 selects PPC family (μPC860)
F3	CSB	I	Chip select, active low. A low signal selects the IXF3208 for read/write operations.
N16	RWB	I	Read = 1, Write = 0. This signal distinguishes between read and write operation.
N15	RDYB	O	Ready signal, active low. Open Drain. When programmed as an input, this pin will be three stated. When the transfer to this device is selected, this signal is set to one, then when the transfer can be completed it is set to one and when the host removes CSB (CSB='1') then this signal goes to three state.
P16	INTB	O	Hardware interrupt output. Open Drain.
F2	WEB	I	Write enable, active low (for MPC860). Depending on the microprocessor being used, this signal indicates a write operation when CSB is active, the IXF3208 loads the internal register with data provided on the data bus.
P14	DSB	I	Data strobe, active low. Depending on the microprocessor being used, this signal operates in a different way in the modes supported by the three processors. See the microprocessor interface description.
Clock References			
P5	E1x24	I	Clock input to be used to generate E1 rates locked to the reference, with jitter removed. This signal is also required if a divided down frequency is going to be used as a timing reference for the Tx line side. Otherwise it can be set to '0'.
T5	T1x24	I	Clock input to be used to generate T1 rates locked to the reference, with jitter removed. This signal is required if the internal PLL is to be used to remove jitter from a reference line signal. This signal is also required if a divided down frequency is going to be used as a timing reference for the Tx line side. When not in use, set to '0'.
System Clock			
E1	SYSCLK	I	The system clock used for the internal state machines. Typically a 33 MHz clock.
R6	RESETB	I	Master hardware reset, active low.
Clock Outputs			
R5	REFCLK	O	Reference clock that can be taken from any of the Rx lines.
JTAG Interface			

Table 1. IXF3208 Ball Description

PBGA	Ball Name	I/O	Description
E15	TMS	I	JTAG Test Mode. Test Mode Select (TMS). This signal controls the test operation that can be carried out using the IEEE P1149.1 test access port. This is sampled on the rising edge of TCLK. TMS includes an internal pull-up resistor.
E14	TCK	I	JTAG clock. Test Clock (TCK). This signal provides timing for the test operations which can be carried out using the IEEE P1149.1 test access port.
D16	TDI	I	JTAG data input. Test Data Input (TDI). This signal carries test data via IEEE P1149.1 test access port. TD1 is sampled on the rising edge of TCK. TD1 has an internal pull-up resistor.
E13	TDO	O	JTAG data output. Test Data Out (TDO). This signal carries test data out via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO has a three state output which is inactive except when scanning of data is in progress.
E16	TRSTB	I	JTAG reset, active low. Test Reset (TRST) active low This signal provides test access port reset via IEEE P1149.1 test access port. TRST has a pull-up resistor and must be asserted during power up sequence.
Test			
R7	TESTENB	I	1 = Normal operation, 0 = Scan mode.
P7	SCANEN	I	Set to 0 when in normal operation.
T7	TRISTB	I	1 = Normal operation, 0 = Three state all outputs.
P6	NC_5	NC	Reserved (This pin is a No Connect).
T6	NC_6	NC	Reserved (This pin is a No Connect).
P8	NC_3	NC	Reserved (This pin is a No Connect).
R8	NC_4	NC	Reserved (This pin is a No Connect).
H6	NC_1	NC	Reserved (This pin is a No Connect).
T8	NC_2	NC	Reserved (This pin is a No Connect).

Table 1. IXF3208 Ball Description

PBGA	Ball Name	I/O	Description
A10, E4, E5, E12, F4, F8, F9, F11, F12, G4, G6, G7, G8, G9, G10, G11, H5, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, K12, L4, L5, L6, L7, L8, L9, L10, L11, M5, M11, M12, N5, N6, N7, N8, N9, N10	VSS		Ground return, all VSS pins should be connected to ground.
F5, F7, F10, G12, J12, K5, M7, M9	VDD_IO		Interface circuitry supplied voltage. Should be connected to a decoupled 3.3V power supply.
E9, E11, F6, G5, J5, L12, M6, M8, M10	VDD_CORE		Core logic supply voltage. Should be connected to a decoupled 1.8V power supply.

Feature Set 3

Table 2. Line and Framing

Feature	Description
Interface	Bipolar: POS, NEG, CLK Unipolar: NRZ, CLK
Line coding	T1: Selectable AMI (per ANSI T1.102) B8ZS (per ANSI T1.102) Forced one's density function ZCS (bit 7) in Tx direction only E1: Selectable AMI (per ITU G.703) HDB3 (per ITU G.703)
Line monitoring	T1 – Maskable interrupt generated for all conditions AIS – Alarm Indication Signal. A ones density of at least 99.9% in a window of 3 ms to 75 ms. (Per ANSI T1.231 and ITU G.775). Optionally the OOF condition can be used to validate AIS (per ANSI T1.403) LOS - Loss of signal: 175 ± 75 clocks with no pulse transitions (per ANSI T1.231) BPV - Bipolar violation EXZ – Excess zero detection E1 - Maskable interrupt generated for all conditions AIS – Alarm Indication Signal. Two or less 0s in two consecutive double-frame windows (per ITU G.775) Or: OOF and less than 3 zeros in a 512 bits period (per ETS 300 233) LOS – Loss of signal: N consecutive intervals with no pulse transitions, where N is in the range of 10 to 255 (per ITU G.775) Or: A 1ms window with no transitions will cause LOS (per ITU I.431) BPV – Bipolar Violation Detection. Two consecutive marks of the same polarity HDB3 – Two consecutive BPVs of the same polarity

Table 2. Line and Framing

Feature	Description
Framing modes	T1: D4-SF (per ANSI T1.107, T1.403) ESF (per ANSI T1.107, T1.403) SLC-96 (per Bellcore TR-TSY-008, GR-303) E1: FAS/NFAS double frame (per ITU G.704, G.706) CRC-4 Multiframe (per ITU G.704, G.706) CAS multiframe (per ITU G.704, G.706, G.732) CRC4 and CAS multiframe (per ITU G.704, G.706, G.732) J1: J1 12 frame multiframe (per JT G.703, JT G.704, JT G.706, I.431) J1 24 frame multiframe (per JT G.703, JT G.704, JT G.706, I.431) Transparent: The device does not search or generate framing information. T1 or E1 transparent. If a frame pulse is generated or received at the backplane it must follow the T1 or E1 frame duration (193 or 256 bits).
Maximum average reframe time	T1 – D4 SF 50 ms (per G.704) T1 – ESF 15 ms (per G.706) T1 – SLC-96 50 ms (per G.706) J1 – 12 frames 50 ms (using as reference G.704) J1 – ESF (24 frames) 15 ms (using as reference G.706) E1 – FAS/NFAS ---_____ E1 – CRC4 50------_____ E1 – CAS-------------_____ E1 – CRC4/CAS----_____

Table 2. Line and Framing

Feature	Description
False framing protection	T1 - D4 SF: Ft coupled with Fs framing bits T1- ESF: Fe framing bits coupled with CRC-6 error detection bits. T1- SLC-96: Ft framing bits coupled with Fs bits plus DDL spoiler bits E1 - CRC4: FAS/NFAS coupled with CRC4 sync sequence. CRC4 calculation also checked.
Out Of Frame (OOF) conditions	Out Of Frame detection (OOF) - Maskable interrupt generated. Reframing Automatic or manual reframing upon detection of OOF condition. Change of Frame Alignment (COFA) Latest receiver synchronization results in a change of frame or multiframe alignment. After reset, the first time the port gets synchronized, a COFA is always declared. T1 D4: out of frame is forced when there are M errors in a programmable window of N consecutive Ft or Fs bits. N= 1,2,...,7, M= 1,2,...,7 T1 ESF: out of frame is forced when there are M errors in a programmable window of N consecutive Fe bits. M, N= 1,2,...,7 If the number of CRC6 errors is equal or exceeds 320 in a one second this will also force reframe (optional). Loss of Basic Frame Alignment (BFA): Three consecutive errors in FAS or three consecutive errors in NFAS. Optionally, in CRC mode, If 915 or more CRC errors are detected in a one second window then the reframe process is started or If N errors in a window of M bits occur in the CRC multiframe alignment signal. E1 Doubleframe: Loss of BFA. Whenever BFA is lost CAS and CRC multiframes are lost. E1 CAS Multiframe: Two consecutive CAS multiframe alignment words received in error or if all TS16 in a multiframe are 0 (optional).
CRC of T1 ESF and E1 CMF disabling	CRC checking/generation can be disabled. The CRC bits can be taken from the backplane data.

Table 3. Slip Buffers

Feature	Description
Slip buffers	Separate slip buffers for both the receive and transmit paths. Always engaged, the options are Minimum delay or Two Frames Read and Write pointer can be accessed (read and write) from the external host Slip indication Slip direction indication Pointer separation indication (RdPtr – WrPtr) Manual or automatic re-centering under COFA conditions

Table 4. Signaling

Feature	Description
Signaling	T1/J1-Robbed bit signaling D4 SF – Four states: AB bits ESF – Sixteen states: ABCD bits SLC-96 – Four or Nine states: AB or AB+ toggling T1/E1/J1 Common Channel Signaling (CCS) Available using the HDLC section of the FDL module. E1 Channel Associated Signaling (CAS) On TS16 (per ITU G.704) T1/E1/J1: Signaling freeze per DS1/E1 Triggered by loss of Frame conditions. (LOS, AIS, OOF, OOCAS) Signaling debounce Disable or two multiframes Signaling forced by the host The external host can define the signaling to Tx in each direction (line and CSU) This value is kept until the host changes it or releases it Signaling access Signaling can be accessed through the microprocessor port or on the signaling bus Signaling change indicators per DS0 CCS available by selecting any TS in either T1 or E1 modes

Table 5. T1 Performance Monitoring

Feature	Description
Compliance	ANSI T1.231, T1.403
PRM	Automatic generation and detection of one second T1.403 PRM
Counters	15 minutes 24 hours Automatic integration and parameterization of primitives and alarms.

Table 5. T1 Performance Monitoring

Feature	Description
Performance primitives	(per ANSI T1.231) Anomalies: Line BPV – Bipolar Violations Pulse of the same polarity as previous pulse excluding those which are a part of the B8ZS Code EXZ – Excess zeroes AMI/ZCS – Any string with greater than 15 consecutive 0s B8ZS – Any string with greater than 7 consecutive 0s Path CRC-6 – CRC errors Any received CRC-6 code that is not identical to the corresponding locally calculated code FE – Frame bit errors SF – any Ft or Ft and Fs bit error ESF – any Fe Bit error CS – Controlled slips The intentional occurrence of a replication or deletion of an entire DS1 frame to maintain framing under differing Line/System clock conditions Change of Frame Alignment (COFA) Indication Defects: Line LOS – Loss Of Signal OOF – Out Of Frame Path SEF – Severely Errored Seconds In SF mode 2 or more Ft bit errors in a 3 ms window (2 of 12 Ft bits in error) In ESF mode 2 or more Fe bit errors in a 3 ms window (2 of 6 Fe bits in error) AIS – Alarm Indication Signal

Table 5. T1 Performance Monitoring

Feature	Description
Performance failures	Detected Performance Failures (per ANSI T1.231) LOS – LOS defect for more than 2 seconds AIS – AIS defect for more than 2 seconds LOF – OOF defect for more than 2 seconds RAI – Remote Alarm Indication. Indicated as soon as alarm is detected
Far end performance reporting	(per ANSI T1.403) User controllable Automatic message assembly and Transmission FDL PRM support in both receive and transmit directions
Performance parameters	The following performance parameters are collected, integrated and stored (per: ANSI T1.231). The Parameters are Accessible via the Microprocessor Interface. Line parameters - Near end CV-L ES-L SES-L Path parameters - Near end CV-P ES-P SES-P SAS-P CSS-P UAS-P Line parameters - Far end ES-LFE Path parameters - Far end CV-PFE ES-PFE SES-PFE CSS-PFE UAS-PFE ESA-PFE ESC-PFE SEFS-PFE

Table 6. E1 Performance Monitoring

Feature	Description
Compliance	ITU G.821, G.826, O.150, ETS 300 011, ETS 300 233
Counters	Accumulative counters of size 32 bits
Line code violations	(per ITU O.161) AMI - Two consecutive marks of the same polarity HDB3 - Two consecutive marks of the same polarity
Performance primitives	(per ITU G.826) Near End Anomalies a_1 an errored frame alignment signal a_2 an EB as indicated by the CRC not matching the received CRC4 Near End Defects d_1 loss of signal d_2 alarm indication signal d_3 loss of frame alignment In addition, Far end parameters are defined as follows Far End FE-a1 E bit received set (0) FE-d1 RAI is received set
Performance parameters	The following performance parameters are collected and stored (per ITU G.826). The parameters are accessible via the microprocessor interface. Events - EB – Errored Block ES – Errored Second SES – Severely Errored Second BEB – Background Error Block Parameters - ESR – Errored Seconds Ratio SESR – Severely Errored Seconds Ratio BBER – Background Block Error Ratio

3.1 Indicators

This refers to interrupt, status and counters available to the host to convey the state of the device.

Table 7. Main T1 Indicators

Feature	Description
Out Of Frame (OOF)	Indicator and status T1 D4: out of frame is forced when there are M errors in a programmable window of N consecutive Ft or Fs bits. N= 1,2,...,7, M= 1,2,...,7. Default values are 2 errors in a window of 4. T1 ESF: out of frame is forced when there are M errors in a programmable window of N consecutive Fe bits. M, N= 1,2,...,7. Default values are 2 errors in a window of 4. If the number of CRC6 errors is equal or exceeds 320 in a one second this will also force reframe (optional). Synchronization is achieved when 24 (default or 10 optional) Fe for ESF of Ft/Fs consecutive bits are found to match the synchronization pattern.
Loss Of Signal (LOS)	Indicator and status LOS - Loss of signal: 175 ± 75 clocks with no pulse transitions (per ANSI T1.231). The user can define the number of consecutive 0s to declare LOS. The default value is 128. The LOS state is removed if there are at least N ones (default is 16) in a window of M bits (default is 128). (16/128 gives a 12.5% density).
Alarm Indication Signal (AIS)	Indicator and status AIS - Alarm Indication Signal. A ones density of at least 99.9% in a window of 3 ms to 75 ms. (Per ANSI T1.231 and ITU G.775). Optionally the OOF condition can be used to validate AIS (per ANSI T1.403) The user can program the window to use to declare AIS. The default value is 3ms. The AIS indication is cleared when the 99.9% density is not met in the 3ms window.
Remote Alarm Indication (RAI) (yellow alarm)	Indicator and status SF and SLC-96. Normal mode Sets when bit 2 is 0 in every channel (per ANSI T1.231) Clears when the set condition is not present In this case, it is declared when the 24 TSs have bit 2 set to 0 SF Alternate mode (J1 D4 SF) Sets when 12^{th} framing bit = 1 for two consecutive superframes Clears when 12^{th} framing bit = 0 for two consecutive superframes ESF Sets when FDL BOM = 1111111100000000 occurs in 16 contiguous pattern intervals. Cleared when the above pattern does not occur in 2 consecutive intervals.
LOF failure (red alarm)	Sets when an OOF defect persists for a period of 2.5 ± 0.5 seconds. Clears when OOF has been removed for a period of 20 seconds or less. (per ANSI T1.231). The user can change the set and the clear thresholds from 125 microseconds to 8.19 seconds.

Table 7. Main T1 Indicators

Feature	Description
LOS failure	Sets when an LOS defect persists for a period of 2.5 ± 0.5 seconds. Clears when LOS has been removed for a period of 20 seconds or less. (per ANSI T1.231). The user can change the set and the clear thresholds from 125 microseconds to 8.19 seconds.
AIS Failure (Blue Alarm)	Sets when an AIS defect persists for a period of 2.5 ± 0.5 seconds. Clears when AIS has been removed for a period of 20 seconds or less. (per ANSI T1.231). The user can change the set and the clear thresholds from 125 microseconds to 8.19 seconds.
COFA	COFA is declared when the new frame location is different to the previous one.
CRC6 errors Indicator and count	CRC errors latched indicator CRC errors counter
Ft/Fe bit errors Indicator and count	Framing error indication Ft (D4)or Fe (ESF) counters
Fs bit errors Indicator and count	Fs error counter and indicator
Ft+Fs errors Indicator and count	Counter of Ft plus Fs errors and indicator
Slip Indicator and count	Slip indicator and counter
PRM detected	PRM reception indicator and PRM data
MOP detected Indication plus other status info	MOP detected indicators (it does not include PRM)
BOP Indication and count	BOP detected indicator and value The BOP is declared detected when it is continuously detected a number of times indicated by the threshold (default = 10).
Japanese application support	Compliance with JT-G.704: Yellow Alarm generation and detection CRC checking and transmission
Out Of Frame (OOF)	Indicator and status T1 D4: out of frame is forced when there are M errors in a programmable window of N consecutive Ft or Fs bits. N= 1,2,...,7, M= 1,2,...,7. Default values are 2 errors in a window of 4. T1 ESF: out of frame is forced when there are M errors in a programmable window of N consecutive Fe bits. M, N= 1,2,...,7. Default values are 2 errors in a window of 4. If the number of CRC6 errors is equal or exceeds 320 in a one second this will also force reframe (optional). Synchronization is achieved when 24 (default or 10 optional) Fe for ESF of Ft/Fs consecutive bits are found to match the synchronization pattern.

Table 8. Main E1 Indicators

Feature	Description
Out Of Frame (OOF) Out of CRC multiframe Out of CAS multiframe	Loss of Basic Frame Alignment (BFA): Three consecutive errors in FAS or three consecutive errors in NFAS. Optionally, in CRC mode, If 915 or more CRC errors are detected in a one second window, then the reframe process is started (per ITU G.706) or If N errors in a window of M bits occur in the CRC multiframe alignment signal. (default values ar N=2 and M=4). Whenever BFA is lost CAS and CRC multi frames are lost. E1 CAS Multiframe: Two consecutive CAS multiframe alignment words received in error or if all TS16 in a multiframe are 0 (optional). The device gets BFA first and then starts checking for CRC or CAS multi frames, depending on the selected mode.
Loss of Signal (LOS)	(per ITU G.775) Set when there are no transitions in a window of 10 to 255 bit periods. Cleared when there is at least one transition in a window of 10 to 255 bit. The windows are user programmable. or (per ITU I.431, ETS 300 233) Set when there are no transitions in a window of 1 ms (2048 bits) Clear occurs when the programmable ones density is met. The user can program the set, clear and threshold windows. The default value to set LOS is 128 bit periods in 0 and to clear is 16 transitions in a window of 128 bit periods (12.5% ones density).
Blue Alarm (AIS)	(per ITU G.775) Set when less than three 0s are detected in each of two consecutive double frame periods (each doubleframe period is 512 bits). Cleared when each of two consecutive double frame periods contain three or more 0s or when the Frame Alignment Signal (FAS) has been found. Optional: OOF set and less than 3 zeros in a 512 bits period (per ETS 300 233).
Remote Alarm Indication (RAI)	(Per ITU G.775) Set when bit 3 in timeslot 0 of NFAS is 1 for three consecutive times. Cleared when bit 3 of TS 0 in NFAS frames = 0 for three consecutive times.
Remote Multiframe Alarm (TS16 RAI)	(per ITU G.704) Set when bit 6 of TS16 of frame 0 = 1 for two consecutive multi frames. Cleared when bit 6 of TS16 of frame 0 = 0 for two consecutive multi frames.
TS 16 AIS	(per ITU G.775) Set when there are less than four 0s in TS16 in each of two consecutive multi frames. Cleared when each of two consecutive multiframe periods contain 4 or more 0s or when the Multiframe Alignment Signal (MFAS) has been found.
TS 16 LOS	(per ITU G.732) Set when all the TS16 bytes are 0 in two consecutive multi frames. Cleared when at least a 1 is present in a TS16 preceding the multiframe alignment signal.

Table 8. Main E1 Indicators

Feature	Description
COFA	COFA is declared when the new frame location is different to the previous one.
AUX-P	Set when the sequence “10” has been detected in a window of 512 bits with no error or just one error. Cleared when two or more errors in the pattern “10” are found in a 512 bit window.
LOF failure (Red Alarm)	Sets when an OOF defect persists for a period of 2.5 ± 0.5 seconds. Clears when OOF has been removed for a period of 20 seconds or less. The user can change the set and the clear thresholds.
LOS failure	Sets when an LOS defect persists for a period of 2.5 ± 0.5 seconds. Clears when LOS has been removed for a period of 20 seconds or less. The user can change the set and the clear thresholds.
AIS failure (blue alarm)	Sets when an AIS defect persists for a period of 2.5 ± 0.5 seconds. Clears when AIS has been removed for a period of 20 seconds or less. The user can change the set and the clear thresholds.
CRC4 errors Indicator and count	CRC4 errors indicator and count.
FAS errors Indicator and count	FAS error indicator and counter.
NFAS bit errors Indicator and count	NFAS error indicator and counter.
FAS+NFAS errors Indicator and count	FAS+NFAS error indicator and counter.
Slip Indicator and count	Slip indicator and counter.

Table 9. Data Link

Feature	Detail
Dedicated FDL Processors	Dedicated transmit and receive FDL processor per line port Includes MOP (HDLC) processing and BOPs
T1 Data Links	Supported Data Links: SLC-96 Derived Data Link (DDL) (per: Bellcore TR-TSY-008) ESF Facility Data Link (FDL) (per: ANSI T1.403, and Bellcore TR-TSY-499) ESF Facility Data Link (FDL) (per: AT&T TR 54016) ISDN PRI D-Channel handler Support (per: Bellcore TR-TSY-754) The Data Link is accessed through the Microprocessor Interface.
E1 Data Links	Supported Data Links: TS0 Sa4 Bit Data Link (M Channel) (per: ITU I.431 and G.962 (ETS 300 233)) User may select any combination of any of the Sa(4:8) bits TS16 Data Link V5.2 DLC Data Link Support (Timeslots 15, 16, 31) (per: ETS 300 347-1, ITU G.965) The Data Link is accessed through the Microprocessor Interface.

Table 10. Embedded HDLC Controller

Feature	Detail
General	Twenty four full duplex processors, each mappable from one payload bit on any line port, up to the entire clear payload.
Data rates	From 8 Kbps (one payload bit) up to the entire payload (minus framing and signaling bits). Consecutive/Non-Consecutive channel concatenation for H0, H11, H12 support.
Control/access	Control via Processor Interface, byte interface. Access via FIFO registers. Maskable Interrupts for each channel/source.
Applications/ protocols supported	ISDN LAPD/LAPB (HDLC) protocol messaging (per ITU Q.921) Integrated DLC (per: Bellcore GR-303) V5.1 & V5.2 Interfaces (per: ITU G.964/ETS 300 324, ITU G.965/ETS 300 347)
Modes	Non-Automatic: HDLC LAPB and LAPD protocols without procedure support and with address matching. Framed without address matching Framed without CRC check/insertion Fully Transparent. Clear channel, not processing is performed, every byte is stored in the FIFO.
HDLC features	Non-Automatic Mode Supports All LAPx protocols Programmable rate per channel: Any combination of bits, including DS0 sub-rate, DS1, H0, H11, H12 Bit oriented functions: Flag generation/recognition Address recognition Bit stuffing, zero insertion/deletion CRC generation/check Abort generation/recognition Non octet frame content recognition Minimum frame length check and maximum frame length check and cut off Interframe generation/support for 7EHex or FF Hex Supports reception of shared opening/closing flag Supports reception of shared 0 in flags Framed Transparent Mode Starting and ending flag of 7E generation/recognition Removal of starting and ending flag and interframe time fill at receive side Fully Transparent Mode Byte aligned data transmission for transparent mode
FIFO buffers	Transmit FIFO depth of 128 bytes (128 x 1 bytes) Receive FIFO depth of 128 bytes (128 x 1 bytes) FIFO status via Processor Interface

Table 11. Interfaces

Feature	Detail
Processor interface	8 bit parallel data interface Non-multiplexed mode 16 bit address bus Supports MPC860, M68302, I486 and compatibles like M68360 and I960 Motorola and Intel busses supported Asynchronous bus support Wait states are inserted by handling the RDYB signal Internal wait state generator One open drain interrupt output, INTB Internal one second timer for performance data latching Support for interrupt-driven, polled, or mixed access architectures
Line interface	Types: Bipolar data (POS & NEG) and clock NRZ data and clock Independent clock and data inputs/outputs for each channel
System interface: general features	Non-multiplexed or N-Channel multiplexed operation (N = 4 or 8) Byte replication in multiplexed Mode Clock source selection for each port Programmable clock rate selection (1x or 2x data rates) Full user control of frame sync polarity, width, and position TDM, MVIP/ST-BUS, H-MVIP, CHI (data and signaling in the same pin), etc. compatibility Support for gapped clock generation Independent clock, data, signaling, frame pulse and multi-frame pulse signals per port.
System interface: timing	Port timing is independent Tx and Rx timing on each port is fully independent (Tx and Rx can work asynchronously) and use independent clock/frame sync pairs. Selectable internal clock source generated from a single reference; line or external reference clock. Selectable Master or Slave Operation Tx and Rx Clock/Frame Sync signals can be inputs (Slave) or outputs (Master) When the Tx or Rx timing signals are outputs (Master) their timing can be derived from the internal clock source or from a selected Rx Line Clock. Master Clock input can be N x 1.536 MHz, N x 1.544 MHz or N x 2.048 MHz (N = 1, 2, 4 or 8)
Overhead information	Signaling data is accessible: In-band Signaling TDM port Microprocessor Interface The method of access is independent of data direction (i.e., Tx and Rx for a particular port can use different means of access). FDL data is accessible via the microprocessor Interface.

Table 12. Maintenance/Diagnostics

Feature	Detail
Maintenance loopbacks	The following line-side loopbacks are supported: • T1 Line (per: ANSI T1.403, AT&T TR 54016) • T1 Payload (per: ANSI T1.403, AT&T TR 54016) • T1 Partial payload loopback (Up to 24 DS0s simultaneously per port) • E1 Line • E1 Payload • E1 Partial payload loopback (Up to 32 timeslots simultaneously per port) The following system-side loopbacks are supported: • T1 Local loopback (data back from Tx line to system backplane) • E1 local loopback Line and local loopback can be active at the same time. Selective Manual or Automatic Loopback support. Automatic AIS transmit upon loopback activation is selectively supported.
Error injection	Selectable BPV, F-bit (T1)/ FAS Word (E1), and CRC Error Injection. Single errors Programmable rate from 1 to 10exp-6 The error insertion rate is related to the related event, so that errors in Fe bits set to 10exp-1 means that every 10 Fe bits there will be one error inserted. In the case of BPVs, the same rate will be applied to every ten marks.
External indicators	Multiframe signals per line port are reported to the system. Frame sync polarity, width and position are fully programmable. The polarity, width and position of the multiframe signal follows that of the corresponding Frame Sync.
Timeslot code insertion	T1 DRS pattern T1: Selectable digital milliwatt pattern insertion (as per ITU G.711) E1 DRS pattern E1: Selectable digital milliwatt pattern insertion (as per ITU G.711)

Initialization 4

Initialization of the device is performed by executing the following process:

1. Reset the device using either hardware or software reset. Software reset is accomplished by writing the value A1 Hex to Address 00 Hex.
2. Remove the device from reset state.
3. Load the firmware. The IRAM address range is 8000 to BFFF Hex.
4. Enable the internal processor. This is done by writing the value 00 Hex to the CPUREG register at address 0003 Hex.
5. Wait for the processor to indicate that it is ready. This is done by reading register 1D0F Hex. The value after reset is 0. Once the firmware has initialized all the internal registers, it writes a 01Hex to that location.
6. At this point the host can start configuring each module.

4.1 Software Reset

Register 0000 Hex is the reset register: RST. This register is set to 00 Hex by the hardware reset. Once the hardware reset is removed, the device can be set into the reset state by writing A1 Hex to it. The reset state will be maintained as long as the value is maintained. The device will be removed from the reset state by writing a 00 Hex to RST.

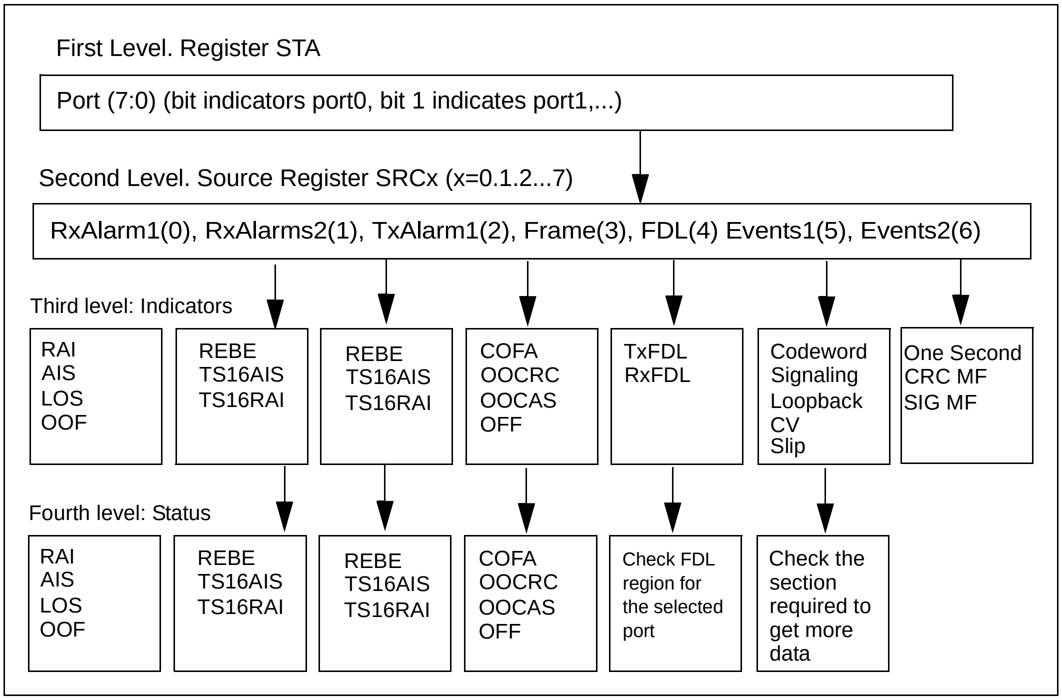
There is also a software reset signal that affects only the internal processor. Register CPURST at address 03 Hex can be used to control this operation. After hardware or software reset, this register is set to 01 Hex. If the host requires only to reset the internal CPU then it must write 01Hex to CPURST. The internal CPU will be held in the reset state as long as CPURST=01Hex.

4.2 Interrupt Handling

The host interacts with the device with configuration, control and status operations performed via direct read and write operations. The device requests servicing by asserting the interrupt line. The host enables the generation of interrupts by programming the interrupt masks. The host could work in polling mode by masking the interrupt pin and monitoring the indicators. If the host is to work in interrupt mode, then it allows the propagation of the selected interrupts to the interrupt pin.

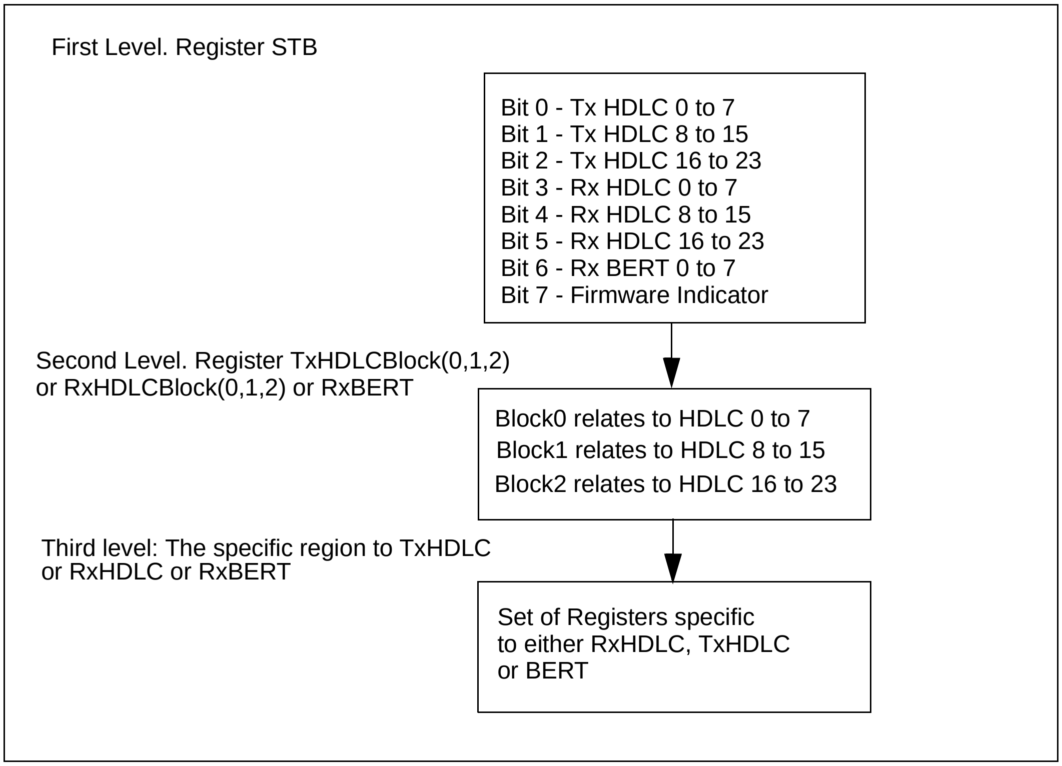
The interrupts and masks are hierarchical. A register points to the port that is generating the interrupt. Once the host knows the port, it can read it and that register points to the source of the interrupt: RxAlarm1, RxAlarm2, TxAlarm1, Frame, FDL, Events1 or Events2. As an example, if RxAlarms1 bit is set, then by reading the RxAlarm register, we find that the AIS bit is set, indicating that an AIS event has been generated. The associated state register can then be read to know the state of the AIS condition, either set or cleared. Note that some registers, like Events2, do not have an associated status register, since the interrupt provides all the required information, in this case a one second, or CAS or CRC multiframe period interrupt.

Figure 5. Interrupt Handling



In addition, there are masks for HDLC and BERT functional units which are also hierarchical. Since these modules can be associated with any port, a set of registers provide the unit where the event has occurred. The host then has to go to the respective memory region to get the proper status.

Figure 6. Interrupt Mapping



T1 Framer 5

5.1 T1 Line Coding

The IXF3208 provides T1 line coding and decoding functions to support non-coding line interfaces and to facilitate performance monitoring. The following sections detail the supported T1 coding formats and associated functions. Unless otherwise noted, coding is separately selectable in both the receive and transmit sides of each port via the port configuration registers.

5.1.1 Alternate Mark Inversion (AMI)

(per: ITU G.703)

AMI is a Return to Zero (RZ) format where a binary "one" (mark) is represented by either a positive or negative going pulse and a binary "zero" (space) is represented by the absence of a pulse. Each consecutive pulse should alternate in polarity (i.e., a positive pulse should always be followed by a negative pulse and a negative pulse should always be followed by a positive pulse) regardless of the number of intervening spaces between the two pulses. In short, *alternating marks* are *inverted*. Two consecutive pulses of the same polarity is known as a Bipolar Violation (BPV). The IXF3208 actively monitors the line signal and provides a count of detected BPVs for performance monitoring purposes. By definition, *all* T1 line signals use basic AMI line coding. However, because T1 receivers rely on the presence of marks in the signal to recover clocking, various standards specify maximum space and minimum mark density requirements.

AMI coding alone does not provide any method of ensuring compliance to mark/space requirements. However, the IXF3208 does provide a means of enforcing the ones density requirement, as described below.

The term "AMI coding" is often used to mean that no specific methods are used to suppress excess zeroes in the signal.

5.1.2 Zero Code Suppression (ZCS or B7)

(per: Bellcore TR-TSY-510)

Zero Code Suppression (ZCS) - also referred to as "Bit 7 "(B7) coding - is the simplest means of assuring that the T1 mark density requirement is met. When the eight bit word (bits 1 to 8) of any T1 channel consists of all zeros, bit 7 is forced to a one (e.g., 00000000 becomes 00000010). ZCS is performed on the transmitted data only. There is no ZCS decoding function defined, since it is impossible for the receiver to differentiate between a ZCS coded "00000010" word, and an actual "00000010" word. Use of ZCS is enabled through the LIMODE register.

In SF and SLC-96, the RAI (Yellow Alarm) insertion occurs prior to ZCS coding. The reason for this is as follows: Suppose the data in a particular channel has only bit 2 set (01000000). Then suppose a yellow alarm was to be transmitted (bit 2 of every channel set to 0). If ZCS coding occurred before RAI insertion, the transmitted data would be 00000000 (ZCS does not set bit 7 since the word is not all zeroes, and the following RAI insertion set bit 2 to zero). If ZCS coding occurred after RAI insertion, the transmitted data would be 00000010 (RAI insertion sets bit 2 to zero, then ZCS sets bit 7 since the word is all zeroes). ZCS is also controlled by (robbed bit) signaling action, as explained in “T1 Robbed-Bit Signaling” on page 82. ZCS can be used in SF, SLC-96, and ESF framing applications.

5.1.3 Binary Eight Zero Substitution (B8ZS)

(per: ANSI T1.102)

ZCS works well for voice band data but can have fatal effects on digital data. B8ZS overcomes this limitation and allows the support of clear channel (64 kbps) data. It is compatible with all standard T1 framing formats. In B8ZS coding, eight consecutive zeroes in the T1 data stream will be replaced by the B8ZS substitution pattern of “000VB0VB”, in which “V” is an intentional bipolar violation (BPV) and “B” is a valid bipolar mark. Note that the polarity of the BPVs and marks depend upon the polarity of the last mark before the “eight zero” occurrence. This substitution is made regardless of where the eight consecutive zeroes occur in the datastream, including framing, signaling, and alarm bits. As opposed to ZCS, which operates on data within a DS0 channel, B8ZS coding can occur across frame boundaries. The IXF3208 performs both B8ZS coding (on the T1 transmitted signal) and B8ZS decoding (on the T1 received signal). Received BPVs that are part of the B8ZS pattern are not counted as BPVs in the coding error counter of the port status register. B8ZS coding/decoding can be selected through the LIMODE register.

5.2 T1 Line Monitoring

The T1 line signal is monitored for the following alarms and impediments. Such monitoring occurs prior to any framing activity.

5.2.1 Alarm Indication Signal (AIS)

(per: ANSI T1.231, ITU G.775, ANSI T1.403)

Also known as Blue Alarm, AIS is declared when less than five spaces are detected in a 3 msec. window of data. This condition will be reliably detected in the presence of a 1.0E-03 Bit Error Rate (BER). When AIS is detected, the appropriate bit in the status register is set and a microprocessor interrupt is generated (unless masked). The window to declare AIS can be set from 3 to 42 ms. The default value is 3 msec.

In addition, the user can select AIS to be validated with OOF (ANSI T1.403)

5.2.2 Bipolar Violations (BPV)

A BPV is defined as two consecutive pulses (marks) of the same polarity. The IXF3208 actively monitors the line signal and provides a status register count of detected BPVs for performance monitoring purposes. The internal counter is copied to the host accessible register on a one second basis.

5.2.3 Excess Zeroes (EXZ)

(per: ANSI T1.231)

The definition of an EXZ occurrence depends upon the line coding format. EXZ will be declared in B8ZS if 8 or more consecutive zeros are detected. In HDB3, when 4 or more consecutive zeros are detected. In AMI, when 16 or more consecutive zeros are detected.

The line signal is monitored for any violations of the maximum space rule and provides a count of EXZ occurrences for performance monitoring purposes.

5.2.4 Loss of Signal (LOS)

(per: ATT TR 62411, ANSI T1.231, ITU G.775)

A LOS is defined as any period of 175 +/- 75 (i.e., 175 clock cycles nominal) clock cycles in which no pulse transitions have occurred. The line signal is monitored for LOS occurrences. When LOS is detected, the appropriate bit in the port status register is set and a microprocessor interrupt is generated (unless masked). The LOS condition is not cleared until the mark density is at least 12.5% for the interval defined in the appropriate specification. The alarm threshold is programmable by modifying the window of measurement and the density of 0s in that window to clear the condition as well as the number of consecutive 0s to declare LOS.

5.3 BPV Error Insertion

The IXF3208 supports the controlled injection of line errors for testing purposes. Different types of errors can be set; BPV, framing, and CRC at rates from continuous to one in a million.

For B8ZS, ZCS, or AMI modes, the transmitter may be programmed to transmit BPV errors. The error insertion register allows insertion of single BPVs and insertions at a rate of 100% (insert continuous BPVs) to 10exp-6 (insert one BPV every million of marks).

BPV insertions are subject to the following conditions:

— B8ZS zero suppression coding is not violated.

— During Line Loopback BPV insertion is not performed even if enabled.

— If the device has detected a DS1 in-band Network Loop back code the IXF3208 will enter a line loopback. This will effectively disable any BPV insertion that may be enabled.

— If the device has a full or partial (DS0s) payload loopback code, if BPV insertion is not desired during this loopback BPV insertion must be manually disabled.

— BPV insertion does not violate data integrity.

5.4 T1 Framing

The basic T1 frame begins with 1 overhead framing bit (F-bit), followed by 192 payload bits. The payload is divided into 24 channels (timeslots), consisting of 8 bits per channel. The bit rate for the T1 frame is fixed at 1.544 Mbps.

Table 13. T1 Basic Frame Description

Parameter	Value
Bit rate	1.544 Mbps
Frame length	193 bits
Number of overhead bits per frame	1 bit
Channelization	24 Channels, 8 bits/channel

Table 13. T1 Basic Frame Description

Parameter	Value
Frame period	125 µs
Frame rate	8 KHz
Channel rate	64 Kbps

In the transmit direction, the IXF3208 may do one of the following:

- Internally generate the Framing (F) bits for the various multi-framing modes using the system interface synchronization frame pulses selected through the TxFramer registers, bits B4:B2.
- The F bits are provided from the system interface and are passed transparently to the line interface by selecting the transparent mode in the Tx Framer register.

In the receive direction, the framer may do one of the following:

- Transport the F bit in a totally dedicated timeslot into the system interface data stream (backplane rate at 2.048 Mbps).
- Integrate the F bits for the various multi-framing modes into the system interface data stream (backplane rate at 1.544 Mbps).
- Strip the F bits, providing only the channelized payload data with the appropriate frame synchronization pulse outputs (backplane rate at 1.536 Mbps).

The basic frame format is combined into various T1 multiframe formats, described in the following sections.

5.5 Superframe (SF)/D4 Format

(per: ANSI T1.107, T1.403)

This mode is selected by programming the appropriate bits in the configuration registers associated to the Rx and Tx direction.

5.5.1 Description

The T1 Superframe (SF) format (also known as D4 Framing) consists of 12 consecutive basic T1 frames, with 1 F-Bit and 192 payload bits per frame. The 12 F-bits are divided into two groups, described as follows:

- Six terminal framing (Ft) bits, used to identify frame boundaries.
- Six signaling framing (Fs) bits, used to identify robbed-bit signaling frames and superframe boundaries.

This arrangement is detailed in Table 14, and shown in Figure 2.

Table 14. SF Framing

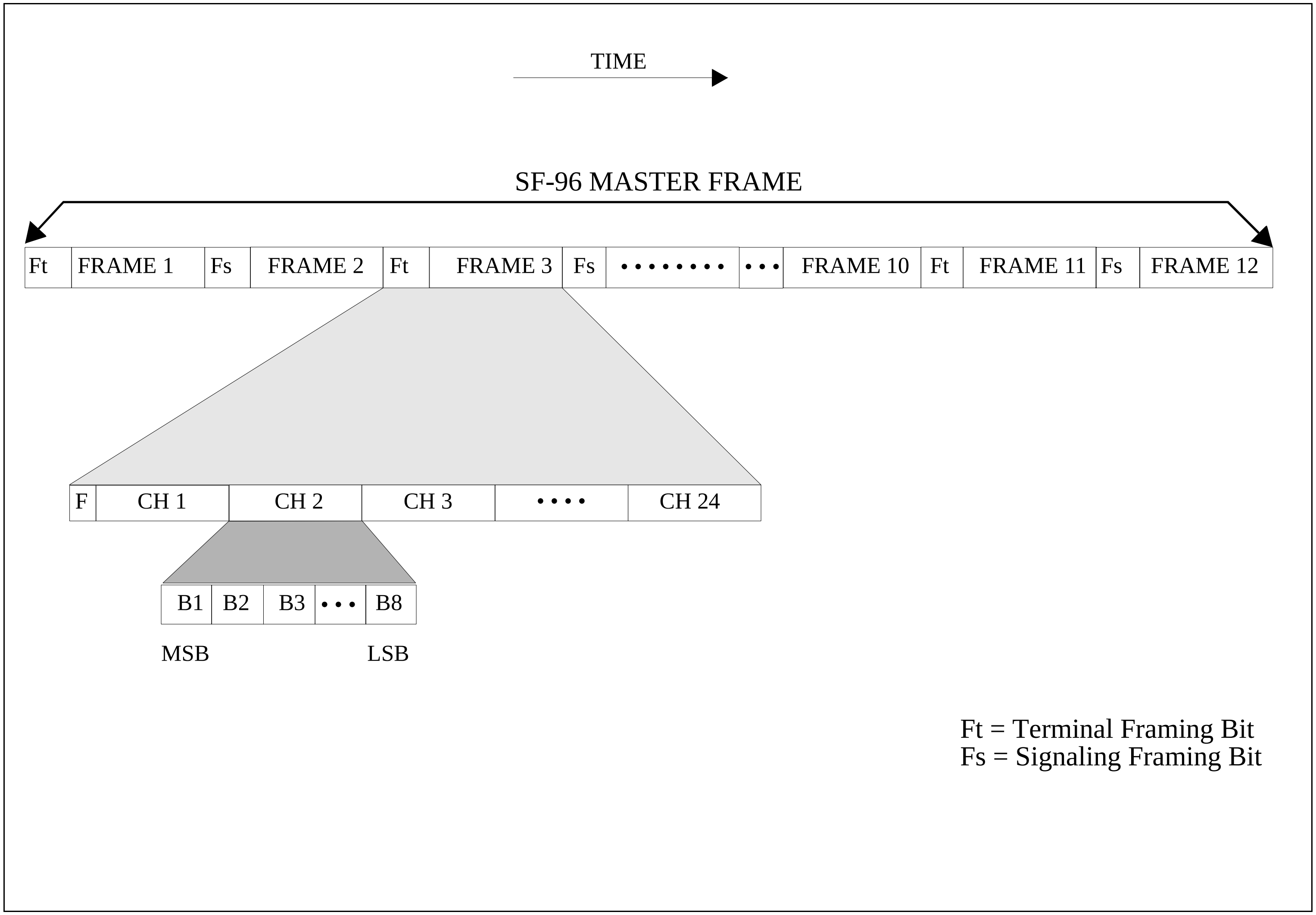
Frame No.	F-Bits			Timeslot Bit Usage			
	Bit No.	Terminal Framing Bit Ft	Signaling Framing Bit Fs	PCM	Signaling (If Used)	Signaling Bit Def'n	
						2-State	4-State
1	1	1	-	1-8	-	-	-
2	194	-	0	1-8	-	-	-
3	387	0	-	1-8	-	-	-
4	580	-	0	1-8	-	-	-
5	773	1	-	1-8	-	-	-
6	966	-	1	1-7	8	A	A
7	1159	0	-	1-8	-	-	-
8	1352	-	1	1-8	-	-	-
9	1545	1	-	1-8	-	-	-
10	1738	-	1	1-8	-	-	-
11	1931	0	-	1-8	-	-	-
12	2124	-	0	1-7	8	A	B

5.5.2 Framing Algorithm

The IXF3208 receive framer declares SF/D4 frame synchronization when a pre-determined number of consecutive correct framing bits (Ft and Fs) are detected. This threshold can be set to *10 Ft and 10 Fs* or *24 Ft and 24 Fs bits (default)*. If valid frame synchronization is not found, then the framing algorithm is restarted. The framing search may be set to look for both the Ft and Fs patterns, to achieve frame synchronization or to look only for Ft bits.

- Ft Bits alone can be used to validate framing or Ft bits qualified with Fs bits can be used to validate framing.
- While in frame, both Ft and Fs bits will be monitored for F bit and Loss of Frame errors.

Figure 7. SF Frame Structure



5.6 SLC-96

(per: Bellcore TR-TSY-008, GR303)

This mode is selected by programming the appropriate bits in the configuration registers for Rx and Tx direction.

5.6.1 Description

The SLC-96 is a digital subscriber loop carrier system which utilizes a modified SF framing format on one or more of four T1 lines serving 96 subscribers. The Fs bit represented in the SF framing pattern is periodically replaced with a low speed data link called the Derived Data Link (DDL). SLC-96 master frames are 9 ms in length and are made up of six SF superframes (72 frames total). In this format, Ft bits are located in odd-numbered frames, and consists of the standard 101010... repeating pattern. The Fs pattern consists of a 000111000111 binary sequence in the F-bit position of even frames from 2 through 22 and frame 72 (total 12 bits). The Fs bit position in the even frames from 24 through 70 contain the 24 bits which make up the SLC-96 DDL.

The entire SLC-96 multiframe structure is shown in Table 15.

DDL operation require bits to be sourced and interpreted by an external processor.
Signalling is discussed in “T1 Robbed-Bit Signaling” on page 82.

5.6.2 Framing Algorithm

The IXF3208 receive framer declares SLC-96 frame synchronization when a complete frame sequence has been detected, including the spoiler bits. If valid frame synchronization is not found then the framing algorithm is restarted. To prevent spurious Fs synchronization, four spoiler bits are incorporated into the DDL block.

- Ft, Fs and spoiler bits are used to validate framing. A complete frame must be detected before declaring synchronization.
- While in frame, Ft and (non-DDL) Fs bits will be monitored for frame errors.

Table 15. SLC-96 Framing[1]

Frame No.		F-Bits			Bit Use In Each Time Slot			Frame No.		F-Bits			Bit Use In Each Time Slot	
	Bit No.	F_t	F_s	DL	PCM	Sig			Bit No.	F_t	F_s	DL	PCM	Sig
1	1	1	-	-	B1-B8	-		37	6949	1	-	-	B1-B8	-
2	194	-	0	-	B1-B8	-		38	7142	-	-	C8	B1-B8	-
3	387	0	-	-	B1-B8	-		39	7335	0	-	-	B1-B8	-
4	580	-	0	-	B1-B8	-		40	7528	-	-	C9	B1-B8	-
5	773	1	-	-	B1-B8	-		41	7721	1	-	-	B1-B8	-
6	966	-	1	-	B1-B7	B8(A)		42	7914	-	-	C10	B1-B7	B8(A)

NOTE:
1. The Cn, Mn, An, and Sn symbols respectively represent: Concentrator, Maintenance, Alarm, and Line-Switched Field Bits. The Spoiler Bits (‘S=n’) are used to prevent spurious superframe synchronization.

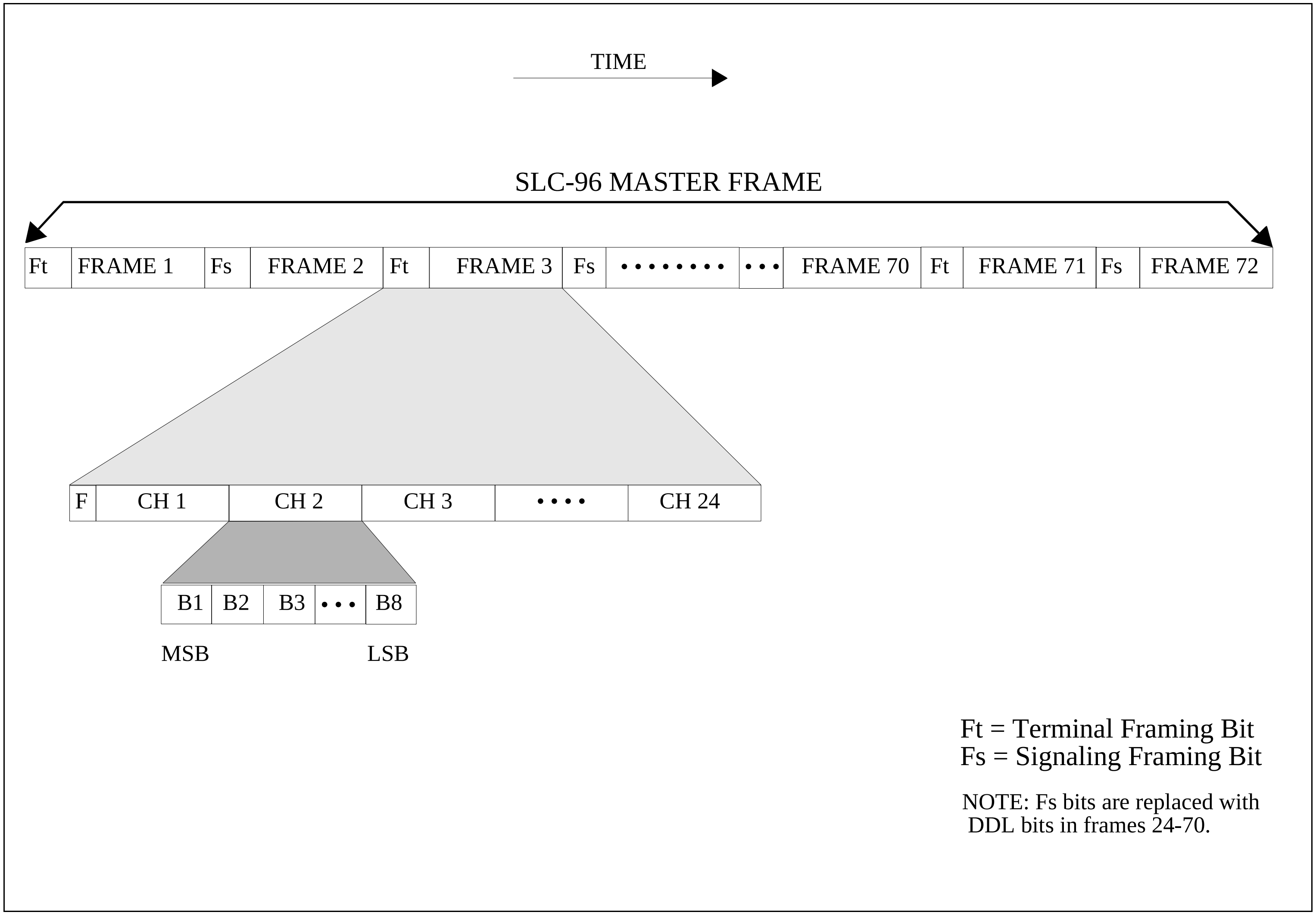
Table 15. SLC-96 Framing[1]

Frame No.		F-Bits			Bit Use In Each Time Slot			Frame No.		F-Bits			Bit Use In Each Time Slot	
	Bit No.	F_t	F_s	DL	PCM	Sig			Bit No.	F_t	F_s	DL	PCM	Sig
7	1159	0	-	-	B1-B8	-		43	8107	0	-	-	B1-B8	-
8	1352	-	1	-	B1-B8	-		44	8300	-	-	C11	B1-B8	-
9	1545	1	-	-	B1-B8	-		45	8493	1	-	-	B1-B8	-
10	1738	-	1	-	B1-B8	-		46	8686	-	-	S=0	B1-B8	-
11	1931	0	-	-	B1-B8	-		47	8879	0	-	-	B1-B8	-
12	2124	-	0	-	B1-B7	B8(B)		48	9072	-	-	S=1 .	B1-B7	B8(B)
13	2317	1	-	-	B1-B8	-		49	9265	1	-	-	B1-B8	-
14	2510	-	0	-	B1-B8	-		50	9458	-	-	S=0	B1-B8	-
15	2703	0	-	-	B1-B8	-		51	9651	0	-	-	B1-B8	-
16	2896	-	0	-	B1-B8	-		52	9844	-	-	M1	B1-B8	-
17	3089	1	-	-	B1-B8	-		53	10037	1	-	-	B1-B8	-
18	3282	-	1	-	B1-B7	B8(A)		54	10230	-	-	M2	B1-B7	B8(A)
19	3475	0	-	-	B1-B8	-		55	10423	0	-	-	B1-B8	-
20	3668	-	1	-	B1-B8	-		56	10626	-	-	M3	B1-B8	-
21	3861	1	-	-	B1-B8	-		57	10809	1	-	-	B1-B8	-
22	4054	-	1	-	B1-B8	-		58	11002	-	-	A1	B1-B8	-
23	4247	0	-	-	B1-B8	-		59	11195	0	-	-	B1-B8	-
24	4440	-	-	C1	B1-B7	B8(B)		60	11388	-	-	A2	B1-B7	B8(B)
25	4633	1	-	-	B1-B8	-		61	11581	1	-	-	B1-B8	-
26	4826	-	-	C2	B1-B8	-		62	11774	-	-	S1	B1-B8	-
27	5019	0	-	-	B1-B8	-		63	11967	0	-	-	B1-B8	-
28	5212	-	-	C3	B1-B8	-		64	12160	-	-	S2	B1-B8	-
29	5405	1	-	-	B1-B8	-		65	12353	1	-	-	B1-B8	-
30	5598	-	-	C4	B1-B7	B8(A)		66	12546	-	-	S3	B1-B7	B8(A)
31	5791	0	-	-	B1-B8	-		67	12739	0	-	-	B1-B8	-
32	6984	-	-	C5	B1-B8	-		68	12932	-	-	S4	B1-B8	-
33	6177	1	-	-	B1-B8	-		69	13125	1	-	-	B1-B8	-
34	6370	-	-	C6	B1-B8	-		70	13318	-	-	S=1	B1-B8	-
35	6563	0	-	-	B1-B8	-		71	13511	0	-	-	B1-B8	-
36	6756	-	-	C7	B1-B7	B8(B)		72	13704	-	0	-	B1-B7	B8(B)

NOTE:

1. The Cn, Mn, An, and Sn symbols respectively represent: Concentrator, Maintenance, Alarm, and Line-Switched Field Bits. The Spoiler Bits (‘S=n’) are used to prevent spurious superframe synchronization.

Figure 8. SF Structure



5.7 ESF

(per: ANSI T1.107, T1.403)

This mode is selected by programming the appropriate bits in the configuration registers in the Rx and Tx direction.

5.7.1 Description

The T1 Extended SuperFrame (ESF) format consists of 24 consecutive basic T1 frames. The corresponding 24 F-bits are used for a variety of functions, described as follows:

- Framing (a 2 kbit pattern) - This is the terminal synchronization channel where frame and superframe alignment is provided by the F-bit of frames 4, 8, 12, 16, 20, and 24. This sequence is referred to as the Framing Pattern Sequence (FPS). Bits that comprise this sequence are referred to as Fe-bits. The repeating pattern is 001011 binary (uses 6 F-bits per extended superframe).
- Error detection (a 2 kbps pattern) - The Cyclic Redundancy Check (CRC bits) carrying the CRC-6 code of the preceding superframe is located in F-bit of frames 2, 6, 10, 14, 18, 22; (uses 6 F-bits per extended superframe).
- Facility Data Link **(**FDL) (a 4 kbps pattern) - Carried by the odd F-bits using 12 F-bits per extended superframe. The FDL is described in “Facility Data Link” on page 90.

The full ESF structure is detailed in table 20 and shown in figure 4.

5.7.2 CRC-6 Procedures

(per: ITU G.706)

The CRC-6 is a method of performance monitoring that is carried in the F-bit position of frames 2, 6, 10, 14, 18, and 22. The CRC-6 bits computed on the 4,632 bits of ESF (n) are transmitted in ESF (n+l) as per CCITT G.704. At the receiver, the CRC-6 bits are computed again based on the received superframe and compared with the CRC-6 check bits received in the subsequent superframe. The compared check bits will be identical in the absence of transmission errors.

Note that in calculating the CRC-6 bits, the F-bits are replaced by binary ls. All information in the other bit positions will be identical to the information in the corresponding multiframe bit positions.

An alternate method of calculating the CRC-6 is used for J1 1.544 Mbps 24-frame Multiframe mode only. The algorithm is similar to that described above and the *actual F-bits are used* in the calculation (rather than being replaced by 1s).

A programmable option that ensures against false framing confirms Fe candidates by CRC-6 verification. Various CRC options are available and are described below:

On the transmit side,

- *The CRC-6 bits are computed by the IXF3208 internally on the output data sent to the LIU for transmission in the default mode.*
- *The CRC-6 bit positions in the transparent input transmit serial data stream will be sent to the line when transparent mode of CRC6 is selected.*

The CRC is calculated before 1s density enforcement (if selected) has been performed.

When an ESF frame is sent, the CRC-6 bits are computed and transmitted in the bit positions indicated in Table 16. The CRC-6 bits computed on the 4632 bits of ESF(N) are transmitted in ESF(N+1). The check bits, Tl through E6 contained in ESF(N+1) shall always be those associated with contents of ESF(N), the immediately preceding ESF. When there is no ESF immediately preceding, the check bits may be assigned any value.

On the receive side,

- *The IXF3208 can be set to perform no verification or to check CRC-6 before declaring a valid frame alignment.*

On the receive side the error verification is performed by recomputing the CRC bits and comparing the result to the received CRC-6 bits of the previous superframe. In case of an error, the CRC error counter is incremented.

5.7.3 Framing Algorithm

Multiframe alignment in ESF mode requires that the proper ordering of Fe bits be found before multiframe alignment is declared. The user can program 24 bits (default) or 10 bits to be validated before declaring synchronization. Multiframe alignment can be further qualified with a programmable option to validate the alignment by CRC-6 verification. When the option is enabled, framing is declared only if the Fe bits sequence is correct for 24 consecutive bits and the CRC-6 calculation matches the expected one. If that is not the case, a new search is started.

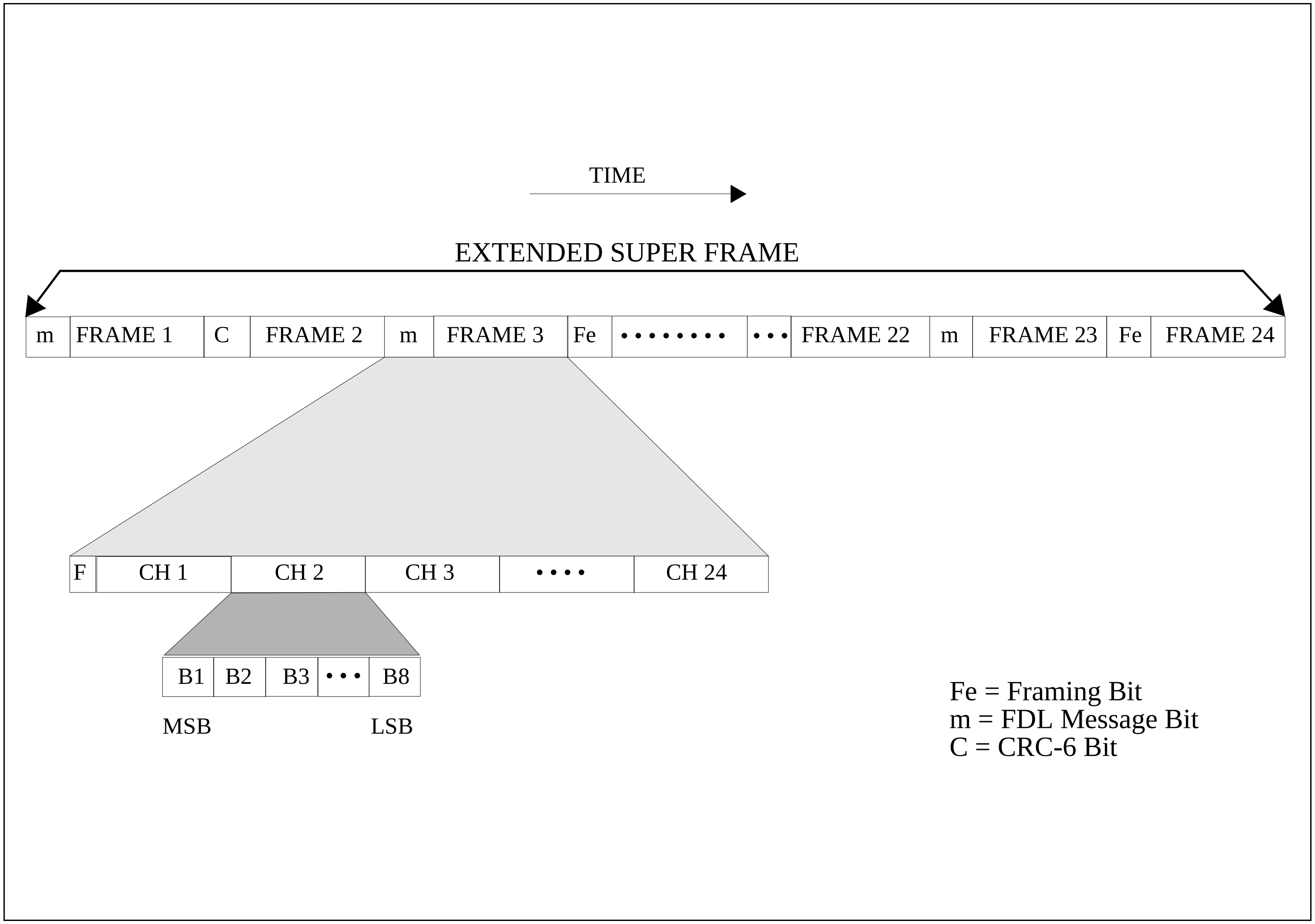
Table 16. ESF Framing

Frame No.	F-Bits				Timeslot Bit Usage		Signaling Bit Def’n		
	Bit No.	Framing Bit Fe	Facility Data Link	CRC-6	PCM	Signaling (If used)	2-State	4-State	16-State
1	1	-	m	-	1-8	-	-	-	-
2	194	-	-	e1	1-8	-	-	-	-
3	387	-	m	-	1-8	-	-	-	-
4	580	0	-	-	1-8	-	-	-	-
5	773	-	m	-	1-8	-	-	-	-
6	966	-	-	e2	1-7	8	A	A	A
7	1159	-	m	-	1-8	-	-	-	-
8	1352	0	-	-	1-8	-	-	-	-
9	1545	-	m	-	1-8	-	-	-	-
10	1738	-	-	e3	1-8	-	-	-	-
11	1931	-	m	-	1-8	-	-	-	-
12	2124	1	-	-	1-7	8	A	B	B
13	2317	-	m	-	1-8	-	-	-	-
14	2510	-	-	e4	1-8	-	-	-	-
15	2703	-	m	-	1-8	-	-	-	-
16	2896	0	-	-	1-8	-	-	-	-
17	3089	-	m	-	1-8	-	-	-	-

Table 16. ESF Framing

Frame No.	F-Bits				Timeslot Bit Usage		Signaling Bit Def'n		
	Bit No.	Framing Bit Fe	Facility Data Link	CRC-6	PCM	Signaling (If used)	2-State	4-State	16-State
18	3282	-	-	e5	1-7	8	A	A	C
19	3475	-	m	-	1-8	-	-	-	-
20	3668	1	-	-	1-8	-	-	-	-
21	3861	-	m	-	1-8	-	-	-	-
22	4054	-	-	e6	1-8	-	-	-	-
23	4247	-	m	-	1-8	-	-	-	-
24	4440	1	-	-	1-7	8	A	B	D

Figure 9. ESF Structure



5.8 General T1 Framing Properties

This section details T1 framing properties not covered elsewhere.

5.8.1 False Framing Protection

(per: Bellcore TR-TSY-000507)

Each T1 framing mode provides a means of false framing as indicated in the following table:

Table 17. T1 False Framing Prevention

Framing Mode	False Framing Prevention Method
SF/D4	Ft framing bits coupled with Fs framing bits
SLC-96	Ft framing bits coupled with Fs framing bits
ESF	Fe framing bits coupled with CRC-6 error detection bits

5.8.2 Maximum Average Reframe Time

Maximum average reframe time applies to a signal with no errors and assumes all bits besides the framing bits have an equal probability of being a 0 or 1. The maximum average reframe time for each mode is specified as follows:

Table 18. Maximum Average Reframe Time

Framing Mode	Maximum Average Reframe Time	Specification
SF/D4	50 msec	ITU G.704
SLC-96	50 msec	Bellcore TR-TSY-8
ESF	15 msec	ITU G.706

Maximum average reframe time is defined as the difference between the instance a known good pseudo-random DS-1 framed signal is applied to the receiver, and a valid framed and channelized signal is observed at the output of the receiver when the maximum number of frame positions have been examined.

5.9 T1 Framing Indicators

5.9.1 Frame Bit Error

Individual frame bits (Ft, Fs for SF) are monitored for errors. An indicator of individual bit error is provided, along with a maskable interrupt upon error and a count of individual errors, on a one second basis.

5.9.2 Out of Frame Detection

An Out of Frame (OOF) condition is declared when a particular ratio of framing bits are determined to be in error. The OOF ratio is user selectable by setting the appropriate FWIN and FERR bits in the configuration register. The user can select any window from 1 to 7 and any error threshold from 1 to 7. The most common selectable combination of bits and ratios are given in the following table:

Table 19. Out Of Frame (OOF) Criteria Options[1]

Format	Ratio	Fe	Ft	Fs	Ft & Fs
ESF	2/4 2/5 2/6 3/5	X X X X	-	-	-
D4 SF	2/4 2/5 2/6	-	X X X	X X X	X X X
SLC-96	2/4 2/5	-	X X	X X	X X

NOTES:
1. applicable.
2. 2/n refers to any two framing bits in error in a sliding window of n framing bits (including 2 consecutive frame bit errors). An Ft bit window, an Fs bit window, and Ft & Fs combined window may all be monitored simultaneously by user selection.
3. In SLC-96, once DDL alignment is determined, only Fs bits that do not carry DDL information will be used in OOF detection. DDL bits can be considered unerrored Fs bits.

When a receive OOF event occurs, the framer declares a maskable OOF interrupt to the host processor.

5.9.3 Resynchronization

The framer may be configured to resynchronize automatically (default) or manually upon detection of an OOF condition. When an OOF condition is present, the IXF3208 will automatically search for Frame Sync, if enabled to do so.

5.9.4 Change Of Frame Alignment (COFA)

A COFA condition is reported when the last receiver resynchronization resulted in a change of frame alignment. COFAs indicate that a new bit position has been selected as the valid framing bit location, whereas OOFs indicate that only some percentage of the framing bits are in error. COFAs are always associated with an OOF.

The IXF3208 provides a COFA indication bit in the port status register.

5.10 Frame and Cyclic Redundancy Check (CRC) Error Insertion

The IXF3208 supports the controlled injection of various classes of errors for testing purposes. The injection of errors is controlled by setting the appropriate bits.

5.10.1 Frame Bit Error Insertion

The transmit framer may be programmed to insert either single frame bit errors or F-bit errors at several rates up to one in a million. The errors can be inserted in Ft, Fs or Fe bits, by inverting the value generated by the framer.

5.10.2 CRC Error Insertion

When the IXF3208 sources the CRC bits, an additional feature allows the IXF3208 to command deliberate inversion (and thereby corruption) of the outgoing CRC code words. A single CRC error can be inserted. CRC error insertions at a rate of one per multiframe (continuous) or at a different rate up to 10E-6 are available. CRC error insertion is only available in ESF mode and only affects the framing bits which carry the CRC.

5.11 T1 Alarms

Details are provided in this section for the detection and transmission of the following alarms:

- Red. This alarm indicates loss of receive-side framing.
- Yellow. Also known as Remote Alarm Indication (RAI). Indicates a receive-side fault on the far-end and is therefore an indication of local-side transmit path performance. Typically, a yellow alarm is transmitted by a terminal in response to the detection of a blue alarm and some cases a red alarm.
- Blue. Also known as the Alarm Indication Signal (AIS). This signal indicates that the remote terminal is off-line and/or undergoing maintenance. Also known as the “Keep-Alive” signal, it is generated to allow proper clock recovery on lines undergoing maintenance (therefore preventing excess jitter transmission, etc.).

5.11.1 Red Alarm Detection

(per: ANSI T1.231)

The loss of frame condition is integrated for N time (N from 125 µ sec to 8.19 sec.) before the Red alarm status bit (RED) goes active and a maskable interrupt is generated. Intermittent OOF conditions are integrated so that if the density of OOF conditions is equal or above the set value, the alarm is declared. The Red alarm flag will be cleared if no OOF occurs for M time after re-acquisition of frame synchronization, where N can be any number up to 8.19 seconds. The clear condition is also integrated so that if the OOF state is not present for a density above the clear value, the alarm is removed. The default values are 2.5 seconds to set and 8.19 seconds to clear.

The Loss Of The Frame (OOF) condition, as well as, the failure (red alarm) are reported in separate bits with change indicator and real time status.

5.11.2 Yellow Alarm Detection

The detection of yellow alarm is dependent upon framing mode, as described below.

5.11.2.1 SF and SLC-96

(per: ANSI T1.403)

In the SF mode, detection is based on bit 2 being equal to 0 in all TS of a frame. When this condition is detected, the Receive Yellow Alarm flag bit is set, and a maskable interrupt is generated. Further integration of yellow alarm can be done using the programmable thresholds available for the integrated version of this alarm.

5.11.2.2 J1 SF

(per: TTC JT-G704)

In J1 (12-Frame Multiframe) mode, an alternate yellow alarm (Japanese Yellow Alarm) is defined. Japanese yellow alarm is detected if the Fs bit in frame 12 of the superframe is equal to 1 for 2 consecutive superframes, and is cleared when the 12th F-bit is not equal to one for 2 consecutive superframes. Status indication and interrupt operation are identical to SF operation.

5.11.2.3 ESF FDL

In ESF an additional yellow alarm is detectable based upon the FDL (per: ANSI T1.403). In this mode, the Yellow Alarm is declared if an FDL pattern (1111 1111 0000 0000) occurs in 16 contiguous 16-bit pattern intervals on the ESF datalink. The yellow alarm is cleared if the pattern does not match the alarm pattern in two contiguous patterns.

5.11.2.4 J1 ESF FDL

(per: TTC JT-G704)

In J1-24 multiframe structure, the yellow alarm is detected when 16 consecutive ones are detected in the DL bit.

5.11.3 Yellow Alarm Transmission

A yellow alarm transmission is initiated when the configuration bit is set or as a result of a consequent action.

Yellow Alarm may be sent automatically if the receiver automatic consequent action feature is enabled, and a triggering event is received by the IXF3208. The triggering event is controlled by the automatic alarm control register. The alarm is sent as long as the receive event is present.

Depending on the selected framing mode, the yellow alarm transmission is performed differently.

5.11.3.1 SF and SLC-96

(per: ANSI T1.403)

In SF framing modes (SF, SLC-96), yellow alarm transmission is accomplished by forcing the 2nd most significant bit of all the PCM channels to a 0. This function is performed before ZCS processing, if the coding option is enabled.

5.11.3.2 J1 SF

(per: TTC JT-G704)

In J1 12-Frame Multiframe (SF) mode, an alternate yellow alarm transmission (Japanese Yellow Alarm) is enabled which will invert the 12th frame bit to 1.

5.11.3.3 ESF FDL

In ESF, the Yellow Alarm can be transmitted in the FDL. This provides compliance with ANSI T1.403. In this mode, the FDL yellow alarm pattern (1111 1111 0000 0000) is transmitted on the FDL. When the yellow alarm transmit bit is cleared, the IXF3208 will send the idle code and wait for the next message from the selected FDL data source.

5.11.3.4 J1 ESF FDL

(per: TTC JT-G704)

In J1 24-frme multiframe mode, the FDL yellow alarm is detected when 16 consecutive ones n the data link bits.

5.11.4 Blue Alarm Detection

(per: ANSI T1.231)

An Alarm Indication Signal is declared when less than five 0s exist in a 3 ms window of received data. AIS is reported by the RAIS flag, and causes a maskable processor interrupt. This indicator will be cleared if a sufficient number of 0s (6 or more in a 3 ms window) are present in the received signal. The blue alarm will be reliably detected in the presence of a $1x10^{-3}$ BER.

The AIS condition, as well as, the failure (blue alarm) are reported in separate bits with change indicator and real time status.

5.11.5 Blue Alarm Transmission

(per: ANSI T1.231)

By setting the appropriate bits in the transmitter an AIS can be sent as an unframed all-ones from TPOS and TNEG pins.

AIS also may be sent automatically if the receiver automatic alarm response feature is enabled, and a triggering event is received by the IXF3208. The triggering event is controlled by the automatic alarm control register. The alarm is sent as long as the receive event is present.

5.12 Fractional T1

The IXF3208 provides a simple mechanism to support Fractional T1 operation.

In Fractional T1 mode, the system side can be programmed to source gapped clock outputs for both the receive and transmit directions. Gapping is possible at a DS0 level and is programmable. Fractional T1 is enabled by programming the appropriate receive and transmit gap selections. The f bit is optionally gapped when in gap clock mode. The clock must be output from the device in both the Rx and Tx backplane directions.

Gapping should be used in 1x streams only. Two clocks per bit period is supported.

Gapped clocks will only be generated when the IXF3208 is the clock source. When the IXF3208 is a clock sink, it requires a continuous, non-gapped clock for correct operation. In this case, clock gapping for fractional T1 must be handled externally.

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(per: TTC JT-G703, JT-G704, JT-G706, and JT-I431)

The operation of J1 frames is very similar to that of T1 frames. In this chapter only the differences between J1 and T1 will be described. The rest of the functions, like line coding, AIS, OOF, etc. are the same and the user should refer to the T1 section for the description of them.

6.1 J1 Operation

(per: TTC JT-G704)

The primary differences between the J1 and T1 operations are the following:

- Sightly modified multiframe structures (both 12-frame multiframe (SF) and 24-frame multiframe (ESF)).
- Different yellow alarm definition in 12 AND 24 multiframe modeS.
- Different CRC-6 procedure in 24-frame (ESF) multiframe mode.

These differences and operation are described below.

6.2 Multiframe Structures

6.2.1 12-Frame Multiframe

The modified J1 1.544 Mbps 12-Frame multiframe structure is shown in Table 20, below:

Table 20. J1 12-Frame Multiframe Structure

Frame No.	F-Bits			Timeslot Bit Usage			
	Bit No.	Terminal Framing Bit Ft	Signaling Framing Bit Fs	PCM	Signaling (If Used)	Signaling Bit Def'n	
						2-State	4-State
1	1	1	-	1-8	-	-	-
2	194	-	0	1-8	-	-	-
3	387	0	-	1-8	-	-	-
4	580	-	0	1-8	-	-	-
5	773	1	-	1-8	-	-	-
6	966	-	1	1-7	8	A	A
7	1159	0	-	1-8	-	-	-
8	1352	-	1	1-8	-	-	-
9	1545	1	-	1-8	-	-	-

Table 20. J1 12-Frame Multiframe Structure

Frame No.	F-Bits			Timeslot Bit Usage			
	Bit No.	Terminal Framing Bit Ft	Signaling Framing Bit Fs	PCM	Signaling (If Used)	Signaling Bit Def'n	
						2-State	4-State
10	1738	-	1	1-8	-	-	-
11	1931	0	-	1-8	-	-	-
12	2124	-	Japanese Yellow Alarm	1-7	8	A	B

The most notable difference (from T1 SF) is the (re)definition of the F-bit in the 12th frame of the multiframe structure. This bit is now defined to be a far-end receive failure alarm, also known as "Japanese Yellow Alarm."

Operation of Japanese Yellow Alarm is described in "J1 ESF FDL" on page 60. Note that this alarm is valid only when J1 12-Frame multiframe mode is selected.

Furthermore, the use of Japanese Yellow Alarm, in which an Fs bit is lost to RAI use, requires a modified framing algorithm (from the T1 SF algorithm) to robustly handle the modified framing structure.

The 12-Frame multiframe structure is selected by enabling J1 operation, selecting Frame 12 yellow alarm and SF framing.

6.2.2 24 Frame Multiframe

The modified J1 1.544 Mbps 24-Frame multiframe structure is shown in the table below:

Table 21. J1 24-Frame Multiframe Structure

Frame No.	F-Bits				Timeslot Bit Usage		Signaling Bit Def'n		
	Bit No.	Framing Bit Fe	Facility Data Link	CRC-6	PCM	Signaling (If used)	2-State	4-State	16-State
1	1	-	m	-	1-8	-	-	-	-
2	194	-	-	e1	1-8	-	-	-	-
3	387	-	m	-	1-8	-	-	-	-
4	580	0	-	-	1-8	-	-	-	-
5	773	-	m	-	1-8	-	-	-	-
6	966	-	-	e2	1-7	8	A	A	A
7	1159	-	m	-	1-8	-	-	-	-
8	1352	0	-	-	1-8	-	-	-	-
9	1545	-	m	-	1-8	-	-	-	-
10	1738	-	-	e3	1-8	-	-	-	-
11	1931	-	m	-	1-8	-	-	-	-
12	2124	1	-	-	1-7	8	A	B	B

Table 21. J1 24-Frame Multiframe Structure

Frame No.	F-Bits				Timeslot Bit Usage		Signaling Bit Def'n		
	Bit No.	Framing Bit Fe	Facility Data Link	CRC-6	PCM	Signaling (If used)	2-State	4-State	16-State
13	2317	-	m	-	1-8	-	-	-	-
14	2510	-	-	e4	1-8	-	-	-	-
15	2703	-	m	-	1-8	-	-	-	-
16	2896	0	-	-	1-8	-	-	-	-
17	3089	-	m	-	1-8	-	-	-	-
18	3282	-	-	e5	1-7	8	A	A	C
19	3475	-	m	-	1-8	-	-	-	-
20	3668	1	-	-	1-8	-	-	-	-
21	3861	-	m	-	1-8	-	-	-	-
22	4054	-	-	e6	1-8	-	-	-	-
23	4247	-	m	-	1-8	-	-	-	-
24	4440	1	-	-	1-7	8	A	B	D

The major difference in operation of the J1 24-Multiframe format and T1 ESF is the (re)definition of the CRC-6 calculation procedures. In J1, 1.544 Mbps 24-frame multiframe format, the CRC-6 calculation is based upon the actual values of all 4,632 bits in the multiframe structure, *including the actual Fe bit values*. In T1 ESF, the CRC-6 calculation "assumes" all Fe bits to a value of one for calculation purposes. See "CRC-6 Procedures" on page 52.

The 24-Frame multiframe structure is selected by enabling J1 operation, selecting 24 frames structure.

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7.1 E1 Line Coding

The IXF3208 provides E1 line coding and decoding functions to support non-coding line interfaces and to facilitate performance monitoring. The following sections detail the supported E1 coding formats.

7.1.1 Alternate Mark Inversion (AMI)

(per: ITU G.701)

AMI is a Return to Zero (RZ) format where a binary “one” (mark) is represented by either a positive or negative going pulse and a binary “zero” (space) is represented by the absence of a pulse. Each consecutive pulse should alternate in polarity (i.e., a positive pulse should always be followed by a negative pulse and a negative pulse should always be followed by a positive pulse) regardless of the number of intervening spaces between the two pulses.

To prevent excess zeroes from occurring, the HDB3 line coding method is used, and is described below.

7.1.2 High Density Bipolar Three (HDB3)

(per: ITU G.703)

In HDB3 coding, four consecutive zeroes in the E1 data stream will be replaced by the HDB3 substitution pattern of either “000V” or “B00V, in which “V” is an intentional bipolar violation (BPV) and “B” is a valid bipolar mark. This limits the maximum number of consecutive spaces to three. The choice of substitution pattern is made so that the number of B pulses between consecutive V pulses is odd (i.e., successive V pulses are of alternate polarity). This substitution is made regardless of where the four consecutive zeroes occur in the datastream, including framing, signaling, and alarm bits. The IXF3208 performs both HDB3 coding on the E1 transmitted signal and HDB3 decoding on the E1 received signal. Receive side HDB3 decoding is selected by setting the decoding bit in the port control register. Similarly, transmit side HDB3 encoding is selected by setting the encoding bit in the port control register. Received BPVs that are part of the HDB3 pattern are not counted as BPVs in the coding violation error counter. HDB3 encoding/decoding is selected by programming the appropriate bits in the LIMODE register.

7.2 E1 Line Monitoring

The E1 line signal is monitored for the following alarms and impediments. Such monitoring occurs prior to any framing activity.

7.2.1 Alarm Indication Signal (AIS)

(per: ITU G.775)

AIS is declared when less than three spaces (i.e., 2 or less zeroes) are detected in a 250 µsec. period of data (512 bit window), on each of two consecutive periods. This condition should be reliably detected in the presence of a 1.0E-03 Bit Error Rate (BER), implying that a framed all-ones pattern will not be mistaken as an AIS.

(per: ETS 300 233)

Alternatively, the AIS indicator can be coupled with the Loss of Frame Detector, in which case the detection of both AIS and LOF are used to set the received AIS indicator bit.

Once AIS is detected, the port status flag is set, and a maskable processor interrupt is generated. The AIS will be cleared when the set conditions are not met.

The device can also send the AIS signal towards the line side when programmed by the user or as a consequent action.

7.2.1.1 Auxiliary Pattern (AUXP)

(per: ETSI 300 233)

ETS 300 233 defines an alternative signal to AIS for E1 lines. This signal, AUXP is an unframed continuous pattern of marks and spaces (101010...).

AUXP is declared when a continuous alternating mark/space pattern is detected over 512-bit period (250 µs, or 2 frames) in the presence of a 10^{-3} Bit Error Rate (BER), implying that a framed 1:1 pattern will not be mistaken as an AUXP. Once AUXP is detected, the alarm status flag is set, and a maskable processor interrupt is generated. The AUXP will be cleared when the pattern is not detected in any subsequent 512-bit period after the detection of AUXP.

When the user programs the device to send AUXP, an unframed 1:1 pattern is transmitted on the line. AIS and AUXP transmission should not be set at the same time, but if they are AIS will take precedence.

7.2.2 Coding Violations

Two basic types of E1 line coding violations are defined:

(per: ITU G.703)

1. A Bipolar Violation (BPV) is defined as two consecutive pulses (marks) of the same polarity.

(per: ITU O.161)

2. An HDB3 coding violation is defined as the occurrence of two consecutive BPVs of the same polarity.

The IXF3208 actively monitors the line signal for coding violations and provides a status register count of detected violations for performance monitoring purposes. The information can be read from the LIV and LICV registers.

7.2.3 Loss of Signal (LOS)

A LOS is defined as any period of 175+/- 75 clock cycles in which no pulse transitions have occurred. The line signal is continually monitored for LOS occurrences. The LOS indication is set when no pulse transitions are detected for a period that exceeds the programmed threshold limit. The LOS indication is cleared if there are N transitions detected in a window of duration M. Receive signal losses set a maskable interrupt flag.

7.2.4 Bipolar Violation (BPV) Error Injection

The IXF3208 supports the controlled injection of line errors for testing purposes. Different types of errors can be set; BPV, framing, CRC at rates from continuous to one in a million.

For HDB3 or AMI modes, the transmitter may be programmed to transmit BPV errors. The error insertion register allows insertion of single BPVs and insertions at a rate of 100% (insert continuous BPVs) to 10E-6 (insert one BPV every million of marks).

BPV insertions are subject to the following conditions:

— HDB3 zero suppression coding is not violated.

— During Line Loopback BPV insertion is not performed even if enabled.

— If the device has detected a DS1 in-band Network Loop back code, the IXF3208 will enter a line loopback. This will effectively disable any BPV insertion that may be enabled.

— If the device has a full or partial (DS0s) payload loopback code, if BPV insertion is not desired during this loopback BPV insertion must be manually disabled.

— BPV insertion does not violate data integrity.

7.3 E1 Framing

(per: ITU G.704, G.706, and G.732)

The basic E1 frame consists of 256 bits, beginning with 8 overhead bits, followed by 248 payload bits. The payload is divided into 31 channels (timeslots), consisting of 8 bits per channel. The bit rate for the E1 frame is fixed at 2,048,000 bits per second.

Table 22. E1 Basic Frame Description

Parameter	Value
Bit rate	2,048 Kbps
Frame length	256 bits
Channelization	32 Channels, 8 bits/channel
Frame period	125 µs
Frame rate	8 KHz
Channel rate	64 Kbps
Payload	30 Channels

This basic frame format is combined into various multiframe formats, described in the following sections.

7.4 FAS/NFAS Framing

(per: ITU G.704, G.706)

Basic G.704 FAS/NFAS framing is selected by enabling E1 framing mode and disabling CAS and CRC-4 multiframing.

7.4.1 Description

Two distinct basic frame types are defined, one with the Frame Alignment Signal (FAS) word in Time Slot 0 (TS0), and one with the Not FAS (NFAS) word in TS0. These two different frame types are alternately transmitted and are used to determine frame synchronization and provide bandwidth for maintenance and overhead functions.

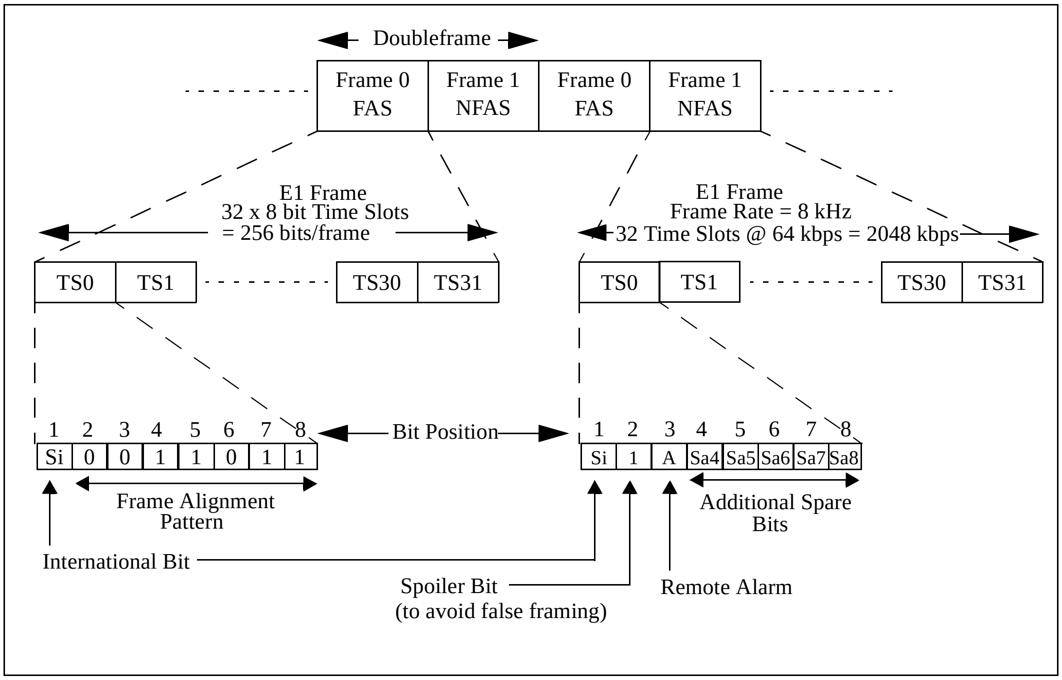
The bits of TS0 have specific definitions, as shown in Table 23, and the entire doubleframe structure is shown in Figure 10 on page 69.

Table 23. E1 Timeslot 0 Bit Allocation

	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
FAS	International Bit (Si)[1]	0	0	1	1	0	1	1
NFAS	International Bit (Si)	1	Remote Alarm Indication (A)[2]	Spare Bit (Sa4)[3]	Spare Bit (Sa5)	Spare Bit (Sa6)	Spare Bit (Sa7)	Spare Bit (Sa8)

NOTES:
1. Reserved for international use. Usage defined in ITU G.704.
2. 0 = No Alarm. 1 = Alarm Condition.
3. Spare Bits. Usage defined in ITU G.704. Possible uses include point-to-point applications (Sa4-Sa8), message-based data link (Sa4), national bit usage (Sa5-Sa7), or PDH synchronization status messages (Sa4-Sa8). User must set these bits to 1 on links crossing an international border.

Figure 10. FAS/NFAS Doubleframe



7.4.2 Operation

In order to achieve synchronization, the following detection sequence is required:

- Reception of a FAS word (0011011 binary) with no errors.
- Reception of a NFAS word with bit 2 = 1 precisely one frame period later.
- Reception of a FAS word with no errors precisely one frame period later.

The OOF flag bit is set when frame sync is lost and cleared when frame alignment is established. It generates a maskable interrupt for the system processor. If frame sync is lost and then regained at a different position (as marked by the off-line framer circuit), the Change Of Frame Alignment (COFA) bit is set.

In the receive direction:

In a FAS frame, the Si bit is extracted and stored in a byte register. The byte is updated on multiframe boundaries. In the NFAS frame, the Si, Sa4 to Sa8 bits are also extracted and stored on multiframe boundaries in byte registers. All those bytes are accessible to the host. When the framer is not in CRC4 mode, the byte is updated every 16 frames without any specific alignment to a frame number, eight FAS and eight NFAS. The Sa bits are also accessible to the data link module. Refer to the Sa-bit handling description in "Sa/Si Bit Access and Handling" on page 79 for configuration details, and see Figure 10 for a diagram of TS0 bit usage.

In the transmit direction:

The FAS/NFAS frame timeslot 0 information can be:

- Generated internally, assembled from the provided Si, Sa, and RAI bits in the appropriate registers.

- Sourced transparently from the system interface to the line.
- A combination of the two above.

The Si bits in the FAS (Sif) and NFAS (Sinf) frames may be passed through transparently from the system interface. This configuration results in the IXF3208 sourcing the FAS and NFAS words from the respective internal sources with the exception of the Si bits, which are now furnished by the external source.

Likewise, the Sa bits in the NFAS frame may be passed through transparently from the serial interface.

7.4.3 FAS/NFAS Error Generation

The LIEI register allows insertion of single FAS or NFAS bit errors or bit error insertions at several rates from continuous to one in a million frames.

7.5 CRC-4 Multiframe

(per: ITU G.704)

This mode is selected when CRC-4 mode is set in the configuration registers in Rx or Tx mode.

7.5.1 Description

Four-bit Cyclic Redundancy Check (CRC-4) Multiframing is used for immunity against false framing and also provides non-intrusive error monitoring capabilities for the E1 payload data. The implementation consists of redefinition of Bit 1 of the FAS/NFAS frames, and definition of a larger multiframe structure.

The CRC-4 Multiframe is comprised of 16 alternating FAS/NFAS frames, consecutively numbered from 0 to 15. This Multiframe is in turn divided into two 8-frame “sub-multiframes,” known as SMF I and SMF II. When CRC-4 multiframing is enabled a CRC is calculated for each “sub-multiframe” and is reported in the next multiframe. In the frames containing FAS, Bit 1 is used to send the four CRC-4 bits, designated C1 - C4, in each SMF. In NFAS frames, Bit 1 is used to transmit the six bit CRC-4 multiframe alignment pattern (001011) and two CRC-4 error indication bits (E).

The CRC-4 Multiframe structure is illustrated in Table 24.

Table 24. CRC-4 Multiframe Structure

SMF	Frame No.	TSO Bit No.							
		1	2	3	4	5	6	7	8
I	0	C1	0	0	1	1	0	1	1
	1	0	1	A	Sa4	Sa5	$Sa6_1$	Sa7	Sa8
	2	C2	0	0	1	1	0	1	1
	3	0	1	A	Sa4	Sa5	$Sa6_2$	Sa7	Sa8
	4	C3	0	0	1	1	0	1	1
	5	1	1	A	Sa4	Sa5	$Sa6_3$	Sa7	Sa8
	6	C4	0	0	1	1	0	1	1
	7	0	1	A	Sa4	Sa5	$Sa6_4$	Sa7	Sa8
II	8	C1	0	0	1	1	0	1	1
	9	1	1	A	Sa4	Sa5	$Sa6_1$	Sa7	Sa8
	10	C2	0	0	1	1	0	1	1
	11	1	1	A	Sa4	Sa5	$Sa6_2$	Sa7	Sa8
	12	C3	0	0	1	1	0	1	1
	13	E1	1	A	Sa4	Sa5	$Sa6_3$	Sa7	Sa8
	14	C4	0	0	1	1	0	1	1
	15	E2	1	A	Sa4	Sa5	$Sa6_4$	Sa7	Sa8

NOTE:
1. C1 - C4: CRC-4 Bits; En: Remote End CRC-4 Block Error Indicator Bits; A: Remote Alarm Indication; Sa4 - Sa8: Additional Spare Bits; $Sa6_N$: Sa6 Bit Numbering per ETS 300 233 Codeword Definition.

7.5.2 Operation

(Per: ITU G.706)

When CRC-4 is selected as the receive framing option, and after FAS/NFAS frame sync is present, the receiver attempts to synchronize to the 16 frame CRC multiframe. CRC-4 multiframe alignment is attained when at least two correct CRC-4 Multiframe Alignment Signals (MFAS) 001011 binary are detected within 8 ms, and the time between each correct MFAS is 2 ms or multiples of 2 ms. The pulse generated every 16 frames at the appropriate backplane multi-frame pulse pin corresponds to the CRC-4 multiframe boundary or to the CAS multiframe boundary, depending on the selection by the user. As a check for spurious frame synchronization, if CRC-4 alignment is not achieved within 8 ms after FAS/NFAS sync, a new search will be initiated for valid FAS/NFAS frame alignment.

7.5.3 CRC Interworking

If ITU G.706 Annex B CRC Interworking is enabled (allowing CRC-4 to non-CRC-4 equipment interworking), the following procedure is used if CRC-4 multiframe alignment is not achieved in a time limit of 100-500 msec:

- Set loss of CRC Multiframe Alignment Indicator.
- Inhibit receive CRC processing.

- Continue to transmit CRC-4 data with both *“E” Bits (REBE bits) set to “0.*

7.5.4 CRC-4 Error Checking

Once CRC-4 multiframe alignment is achieved, CRC-4 error checking may commence (frame alignment monitoring continues). If there is no mismatch between the calculated remainder and the received CRC-4 bits, no CRC error is registered for the checked SMF. If, however, there is a mismatch, a CRC-4 error has occurred and the event will be flagged, a maskable interrupt driven, and recorded in the receiver CRC-4 error counter. The error counter register available to the host is updated every second.

7.5.5 Loss of CRC Multiframe Alignment

(per: ITU G.706, ETSI 300 011 and 300 233)

If basic frame alignment is lost, then CRC multiframe is lost. Optionally, CRC-4 Multiframe alignment is lost if two consecutive CRC MF alignment signals are received with errors. Loss of CRC multiframe is indicated, and causes the generation of a maskable interrupt. This option can be enabled by the user. The default state is disabled.

If a minimum of 915 errored CRC blocks are detected out of a window of 1000, false frame alignment is indicated (loss of frame) and a new search for frame alignment will be started at a point just after the location of the assumed spurious frame alignment signal.

7.5.6 CRC Multiframe Transmission

The CRC multiframe signal is generated by the Tx framer when that mode is enabled. The CRC-4 bits can be sent from the ones calculated in the Tx framer or from the bits received from the backplane side.

In general, the Sif, Sinf, Sa bits and CRC-4 SMF I & II timeslot 0 information can be:

- Generated from the calculated CRC, the provided Si, Sa registers, the provided RAI, and REBE bits from the appropriate register or from the consequent actions module, if enabled.
- Sourced transparently from the system interface to the line.
- A combination of the two above.

Multiframe boundary alignment may come from an external source or from a free-running internal multiframe counter.

7.5.7 CRC-4 Error Insertion

The CRC-4 encoder may be set to insert single or continuous CRC-4 errors by inverting the C1-C4 bits. The Error Injection register allows insertion of either a single CRC error or error insertion at a rate from one to one in a million.

7.5.8 Remote End Block Error (REBE) Operation

Detection:

The REBE (E) bits are indications from the downstream data source that it detected a CRC-4 error in a SMF sent to it by the near end. Normally, the E-bits are set to 1, but when there is a remote end SMF block error (and the remote end is equipped for REBE operation), it is reported by setting the E bit sent back to the near end to 0. Upon receipt of a E bit = 0, the event will be recorded in the receive 12 bit REBE counter.

Transmission:

If the automatic REBE response feature is not enabled, the transmit REBE (E) bits (bit 1 of frames 13 and 15) are set to 1. If REBE automatic response is enabled, and a CRC-4 error is detected in receive SMF I, then the transmit E bit in frame 13 of the next multiframe is set to 0. Similarly, if a CRC-4 error is detected in receive SMF II, then the transmit E bit in frame 15 of the next multiframe is set to 0.

REBE value can be forced by the user or programmed to follow some consequent actions.

7.6 Channel Associated Signaling (CAS) Multiframe

(per: ITU G.704)

7.6.1 Description

CAS Multiframing uses Timeslot 16 to both define signaling multiframe boundaries and to contain individual channel signaling bits. Timeslot 0 usage is identical to FAS/NFAS Doubleframe usage.

The CAS multiframe can be aligned to either the FAS or NFAS frames.

The CAS multiframe is made up of 16 consecutive basic E1 frames (eight double frames) numbered from 0 to 15. Timeslot 16 of frame 0 contains a multiframe alignment signal (MFAS, 0000 binary) in the first 4 bit positions of the timeslot. The remaining 4 bits contain spare bits and an alarm indication. Timeslot 16 in the remaining frames (1-15) contains signaling information for TS 1-15 and TS 17-31.

Table 25 (below) illustrates how sixteen state words are imbedded in TS16. Notice that no signaling is associated with TS0 or TS16, these being overhead time slots and not payload channels.

Table 25. Timeslot 16 CAS Multiframe Structure

Frame Number	Timeslot Sixteen	
	Bits 1 - 4	Bits 5-8
0	0000 MFAS[1]	XYXX[2]
1	ABCD TS1 Signaling ITU CHANNEL 1	ABCD TS17 Signaling ITU CHANNEL 16

NOTES:
1. MultiFrame Alignment Signal.
2. X: Spare Bits; Y: Remote Alarm Indication; 0: No Alarm; 1: Alarm.

Table 25. Timeslot 16 CAS Multiframe Structure

Frame Number	Timeslot Sixteen	
	Bits 1 - 4	Bits 5-8
2	ABCD TS2 Signaling ITU CHANNEL 2	ABCD TS18 Signaling ITU CHANNEL 17
n	ABCD TSn Signaling ITU CHANNEL n	ABCD TS (n+16) Signaling ITU CHANNEL (n+15)
14	ABCD TS14 Signaling ITU CHANNEL 14	ABCD TS30 Signaling ITU CHANNEL 29
15	ABCD TS15 Signaling ITU CHANNEL 15	ABCD TS31 Signaling ITU CHANNEL 30

NOTES:
1. MultiFrame Alignment Signal.
2. X: Spare Bits; Y: Remote Alarm Indication; 0: No Alarm; 1: Alarm.

7.6.2 Operation

The search for the TS16 CAS structure is started when the option is enabled and after basic frame aligned is obtained. CAS alignment is declared when the “0000” pattern is found following a non-0 time slot. The receiver can detect if the CAS multiframe is aligned to the FAS or the NFAS frame. The state of the ‘Y’ bit is used to check for the TS16RAI signal.

7.6.3 Loss of CAS Multiframe

Loss of CAS multiframe is indicated by a maskable indicator. Multiframe alignment loss is reported if two consecutive CAS Multiframe Alignment Signals (MFAS) are received with errors.

Optionally, multiframe alignment loss is reported if all the bits in TS16 are 0s for the period of an entire multiframe. The all 0s option disallows the reception of all 0s used in the signaling bit positions. If alignment is lost due to the all 0s condition, realignment takes place after a valid CAS MultiFrame (MF) is received in TS-16 following a frame in which the TS16 has at least one non-0 bit.

7.6.4 CAS Multiframe Transmission

CAS Multiframe boundary alignment may come from an external source or from an internal multiframe counter. The external sync signal serves to align data on the TX serial interface for insertion into frame 0 of the 16 frame CAS TX multiframe.

The normal multiframe alignment signal consists of all 0s in first 4 bits of TS16 in frame 0 of the CAS multiframe. More than two consecutive erroneous MFAS signals should cause the far end to lose CAS-MF sync.

As shown in Table 29, the X bits are extra bits which accompany the MFAS and the TS 16 remote alarm (Y bit) in TS16 of frame 0. The X bits occupy positions 5, 7 and 8 in TS16, and if the IXF3208 supplies TS16, they may be individually set in the transmit signaling register. The default value for each of the X bits is binary 1.

7.6.5 Alignment to FAS/NFAS

Frame 0 of the transmitted CAS Multiframe (containing the MultiFrame Alignment Signal (MFAS) in timeslot 16) may be aligned to either a FAS or NFAS basic E1 frame.

7.7 Simultaneous CAS and CRC Multiframes

(per: ITU G.704)

In this mode, both CRC and CAS multiframes are present simultaneously. The CAS multiframes are not necessarily synchronized to the CRC-4 multiframes. This mode is enabled simply by simultaneously enabling CAS and CRC multiframing.

7.7.1 Description

This mode of operation allows the concurrent use of both CRC-4 and CAS multiframing. The alignment of the CAS multiframe is independent of the CRC-4 multiframe. Even though the CRC-4 multiframe has a specific sequence (i.e. the C1 bits are in frame 0 and frame 8) frame ‘0’ of the CAS multiframe need only be aligned with either the FAS or NFAS frame word. Therefore, for both FAS and NFAS alignments, frame 0 of the CAS multiframe may be in any of 8 different positions relative to frame 0 of the CRC-4 multiframe. CRC4 and CAS alignment search start after basic frame alignment has been accomplished.

The multiframe pulse delivered to the backplane can be sourced by either the CRC or CAS multiframes. This can be programmed by the user.

7.7.2 Transmission

Both CRC-4 and CAS (TS16) multiframing may be employed simultaneously. The transmit multiframe signal may correspond to either the CAS or CRC-4 multiframe sync pulse. If transmit multiframe is assigned to the CRC-4 multiframe pulse, the CAS multiframe may be aligned to either a FAS or NFAS basic frame. The user can select FAS or NFAS alignment for CAS.

7.8 E1 Alarms

Details are provided in this section for the detection and transmission of the following alarms:

- Red: This alarm indicates loss of receive-side framing. There is no transmitted Red Alarm.
- Remote Alarm Indication (RAI): Indicates a receive-side fault on the far-end and is therefore an indicator of local-side transmit path performance. Typically, a RAI is transmitted by a terminal in response to the detection of red alarm.
- Alarm Indication Signal (AIS): This signal indicates that the remote terminal is off-line and/or undergoing maintenance. Also known as the “Keep-Alive” signal, it is generated to allow

proper clock recovery on lines undergoing maintenance (therefore preventing excess jitter transmission, etc.).

7.8.1 Red Alarm Detection

(per: ITU Q.516)

If an OOF condition persists for a period N or more, the OOF Alarm status bit (RED) goes active and a maskable microprocessor interrupt is generated. The status register flag will clear if no OOF occurrences are detected for a period M. The user can program the value of N and M from 125 µs to 8.19 Seconds.

The Loss Of The Frame (OOF) condition, as well as, the failure (red alarm) are reported in separate bits with change indicator and real time status.

7.8.2 Remote Alarm Indication (RAI)

(per: ITU G.704)

RAI is declared if bit 3 of three consecutive NFAS words equals 1. The alarm is cleared if three consecutive NFAS words contain bit 3=0. The receipt of remote alarm sets the status flag RAI, and generates a maskable processor interrupt.

In the transmit side, RAI can be generated by an user command or as part of a consequent action upon a triggering condition. These triggering receive conditions are defined in the consequent actions section. The remote alarm is sent as long as the triggering receive event is present.

7.8.3 TS16 RAI

(per: ITU G.704)

In CAS multiframe mode, the TS16 remote alarm is transported in bit position 6 in TS16 of frame 0. A binary 0 indicates a normal condition (default), binary 1 denotes TS16 remote alarm.

A TS16 RAI is declared when the TS16 RAI bit is set to one for two consecutive CAS multiframes. An alarm bit and maskable interrupt are generated upon detection. The alarm is cleared when the same bit is equal to zero for two consecutive multiframes.

In the transmit direction, in CAS multiframe mode, the TS16 remote alarm is in bit position 6 in TS16 frame 0. Transmitting a binary 0 indicates a normal condition (default), while sending a binary 1 denotes TS16 remote alarm. The bit may be set manually by writing to the frame 0 TS16 register in the transmit signaling array.

TS16 RAI also may be sent automatically if the receiver automatic alarm response feature is enabled and a triggering event is received by the IXF3208. The triggering event is defined in the consequent actions section.

7.8.4 TS16 AIS

(per: ITU G.775)

When the IXF3208 framer is set to receive CAS multiframe and, if all 1s are received in TS16 for a period of 1 multiframe, then timeslot 16 AIS is declared. This condition sets the flag bit and generates a maskable processor interrupt.

The alarm clears when each of two consecutive multiframe periods contain four or more 0s or when the MFAS signal has been found.

In the transmit direction in CAS multiframe mode, TS16 AIS is a continuous transmission of all 1s in Timeslot 16 for a period of at least 1 multiframe. The IXF3208 may be programmed to send TS16 AIS.

7.8.5 AIS Alarm

(per ITU G.775)

The AIS condition is declared when the incoming signal has two or less zeros in each of two consecutive doubleframe periods (521 bits total). The condition is cleared when each of two consecutive double-frame periods contains three or more zeros or when the frame alignment signal has been found.

The AIS condition as well as the failure (integration of the AIS condition) are reported in separate bits with change indicator and real time status.

In the transmit direction, AIS can be sent by the device commanded by the user or as a consequent action to the reception of an incoming condition.

7.9 Main E1 Indicators

The following table lists the framing indicators supported by the IXF3208. The indicator function is listed, with a cross reference to the description of the function operation.

Table 26. Main E1 Indicators

Indicator	Description
Loss of Frame	"Loss of Basic Frame Alignment (FAS/NFAS)" on page 77
Loss of CRC Multiframe[1]	"Loss of CRC Multiframe Alignment" on page 72
Loss of Signaling (CAS) Multiframe[2]	"Loss of CRC Multiframe Alignment" on page 72
Far End Block Error[3]	"Remote End Block Error (REBE) Operation" on page 72

NOTES:
1. CRC Mode only.
2. CAS Mode only.
3. CRC Mode only.

7.9.1 Loss of Basic Frame Alignment (FAS/NFAS)

(per: ITU G.706)

Loss of FAS/NFAS frame synchronization may be caused by several events. They include:

- Three or more consecutive FAS words that contain single or multiple bit errors.
- Three or more consecutive NFAS words with bit 2 = 0 or three or more consecutive FAS words that contain single or multiple bit errors.

The FAS, or the FAS and NFAS criteria may be used as the basis for loss of synchronization. A maskable interrupt is provided to indicate a loss of frame synchronization. After frame sync is lost, the receiver immediately begins a search for a valid framing pattern, unless automatic resynchronization is disabled.

Loss of frame synchronization can also be detected by the reception of excess CRC errors. See “Loss of CRC Multiframe Alignment” on page 72.

7.9.2 Loss of CRC Alignment

CRC-4 Multiframe alignment is lost if two consecutive CRC MF alignment signals are received with errors. Loss of CRC multiframe is indicated and causes the generation of a maskable interrupt. This option can be enabled by the user. The default state is disabled.

If a minimum of 915 errored CRC blocks are detected out of a window of 1000, false frame alignment is indicated (loss of frame) and a new search for frame alignment will be started at a point just after the location of the assumed spurious frame alignment signal.

7.9.3 Loss of CAS Alignment

Loss of CAS multiframe is indicated by a maskable indicator. Multiframe alignment loss is reported if two consecutive CAS Multiframe Alignment Signals (MFAS) are received with errors.

Optionally, multiframe alignment loss is reported if all the bits in TS16 are 0s for the period of an entire multiframe. The all 0s option disallows the reception of all 0s used in the signaling bit positions. If alignment is lost due to the all 0s condition, realignment takes place after a valid CAS multiframe (MF) is received in TS-16 following a frame in which the TS16 has at least one non-0 bit.

7.9.4 Change of Frame Alignment (COFA)

A COFA condition is reported when the last receiver resynchronization resulted in a change of frame alignment. COFAs indicate that a new bit position has been selected as the valid framing bit location, whereas OOFs indicate that only some percentage of the framing bits are in error. COFAs are always associated with an OOF.

The IXF3208 provides a COFA indication bit in the port status register.

7.9.5 FAS and NFAS Error Counting

In a one second interval, there are 8000 E1 frames, half of which contain FAS words, while the other half contain NFAS words. A FAS error is defined as a FAS word in which bits 2-8 don’t match the binary pattern 0011011, and NFAS errors occur when bit 2 of the NFAS byte is 0. There are FAS and FAS+NFAS error counters available. The error counters do not count errors when the IXF3208 has lost, or is searching for basic FAS/NFAS frame synchronization.

7.9.6 CRC Error Counting

When there is a discrepancy between the expected CRC-4 value and the received one, the CRC error counter is updated. The value of this counter is loaded every second to a host accessible register. The counters are active only when the framer is synchronized to the CRC structure.

7.10 Receiver Resynchronization Control

When an Out Of Frame (OOF) condition is present, the IXF3208 may be programmed to resynchronize automatically (default) or manually. Automatic resynchronization is qualified by an OOF. If automatic resynchronization is disabled, then when the framer gets into OOF, it will stay there until it is able to synchronize.

The receive framer can be manually forced to resynchronize by writing a 0,1 sequence to a bit defined for that purpose. This sequence will cause the framer to go out of frame and search for a new frame sync position.

7.11 Sa/Si Bit Access and Handling

The IXF3208 supports full access to all International Bits (Si) and Spare Bits (Sa_n).

The Si/Sa bits may be serviced by the Si/Sa registers, by the internal FDL controller (only Sa bits), or transparently through the system interface.

7.11.1 Sa/Si Bit Reception and Codewords

- Each Sa-bit and the Sif and Sinf bits have an 8-bit register which is updated each 16 receive frames with the values of the respective Sa or Si bit. The contents of these registers is accessible through the microprocessor port. When the framing mode is CRC4, then this byte is aligned to that multiframe structure. If only CAS multiframe is defined, then the byte is aligned to that structure.
- Any or all of the Sa bits may be selected and passed to the on chip FDL controller which includes an HDLC controllers, where they will be decoded as part of an HDLC message. The message data is accessible through a FIFO in the microprocessor port.
- Codewords, defined as a four bit sequence in the Sa6 bits aligned to the CRC multiframe, are detected. There are 16 bit counters for codewords 0001, 0010 and, 0011 Hex. In addition the line and payload loopback codewords, 1111 Hex and 1010 Hex are detected. They have to be enabled and detected at least 8 consecutive times to take loopback action.

7.11.2 Sa/Si Transmission and Codewords

Host accessible registers hold a byte value for the Sif, Sinf, and Sa bits. The user can select the bits to be sourced from the internal registers (default) or from the backplane in any combination.

Si-bit servicing is not applicable when using CRC-4 multiframing.

The Sif, Sinf and Sa4 to Sa6 bytes are aligned to the CRC4 multiframe. If the CRC4 multiframe is not defined in the Tx direction, then if CAS mode is defined then those bytes are aligned to that multiframe structure. If neither CAS nor CRC4 structures are defined, then the bits are sent in sequence from bit 0 to bit 7 without any further alignment.

7.12 Fractional E1

The IXF3208 provides a simple mechanism to support Fractional E1 operation.

In Fractional E1 mode, the system side can be programed to source gapped clock outputs for both the receive and transmit directions. Gapping is possible at a DS0 level and is programmed in the BPRTSDIS0_31 register. Fractional E1 is enabled by programming the appropriate receive and transmit gap selections and setting the rxgapclken and/or txgapclken bit(s).

Note: Gapped clocks will only be generated when the IXF3208 is the clock source. When the IXF3208 is a clock sink, it requires a continuous, non-gapped clock for correct operation. In this case clock gapping for fractional E1 must be handled externally.

Unframed Mode 8

The IXF3208 provides support for an unframed mode *by* selecting the transparent mode in the Rx or Tx direction. In this mode, the T1 or E1 signal is only line coded/decoded, rate adapted by the elastic stores, and system interface formatted. At the system interface, the notion of framing pulse and time slots is maintained, but there is not any real alignment of the stream to the time slots. The same rates at line and backplane should be used to properly transport the streams from either side.

Signaling 9

This section outlines the methods by which signaling information is conveyed on T1/E1 links.

9.1 Signaling Overview

The IXF3208 provides direct support for the following types of signaling methods:

1. Channel Associated Signaling (CAS). Each channel has its own signaling information. The CAS is implemented differently between T1 and E1, as described below:
   - T1 uses “Robbed-Bit” signaling, in which the LSB in each timeslot of every sixth frame is “borrowed” to convey the signaling information.
   - E1 uses one specific channel (Timeslot 16) to convey the signaling information for all channels.
2. Common Channel Signaling (CCS). A dedicated channel is used to convey signaling information. Example applications which use this include ISDN-PRI (D-Channel), GR-303 and V5.2 Digital Loop Carriers.
3. Transparent. Signaling information is passed transparently (unaltered) through the framer. External means are required to insert and extract signaling information. Example applications which use this include SS7 and MF trunk signaling.

The following means are provided to allow access to the signaling information:

- Transparently in the PCM data presented to the system backplane data port.
- Dedicated system backplane Signaling Ports.
- Microprocessor Interface Registers.

The type of signaling used and the means of access to this signaling information is fully user configurable in the IXF3208 via the port configuration registers.

9.2 Channel Associated Signaling

There are two basic methods of Channel Associated Signaling, Robbed-Bit Signaling used in T1 applications, and Timeslot-16 CAS used in E1 Applications. These methods will be discussed in the following sections.

9.2.1 T1 Robbed-Bit Signaling

T1 Channel Associated Signaling, also known as Robbed-bit Signaling, borrows the least significant bit in every timeslot in frames 6 and 12 in SF/D4. These bits transport signaling information (e.g. on-hook/off-hook, ringing/no-ringing, etc.) for the associated timeslot. The signaling bits borrowed from timeslot N transport the signaling information for timeslot N (where N = 1 to 24). The naming and meaning of each bit depends on the type of signaling being used. The various signaling types and bit naming conventions are presented in Table 27. This table also indicates which signaling types are supported in each framing mode.

Table 27. T1 Robbed Bit Signalling Usage

Signaling Mode	Signaling Bits				Framing Modes		
	A	B	C	D	SF	SLC-96	ESF
None					X	X	X
4-State	X	X			X	X	
9-State	X	X				X[1]	
16-State	X	X	X	X			X

NOTE:
1. SLC-96 9-state signaling mode uses a three level logic system that allows for the A and B bits to take the values of either all ones, all zeroes, or alternating ones and zeroes.

All signaling bits represent binary information, except when nine-state signaling is selected. In nine-state signaling, the two signaling bits provide for a maximum of nine states by using a three level logic system that allows both the A and B signaling bits to take the values of either all ones, all zeros, or alternating ones and zeros. The IXF3208 both encodes and decodes this type of signaling. Four bits are used to represent this information on the dedicated backplane signaling ports and through the processor interface port. The mapping is shown in Table 27. Note that the AB pair is delivered together with the A'B' pair. A toggling in A bit will be shown by A different to A'. A toggling in B bit will be shown by B being different to B'.

Robbed bit signaling can be disabled on a per timeslot basis. This allows for both transparent signaling and clear channel applications.

9.2.2 E1 Channel Associated Signaling

E1 Channel Associated Signaling, also known as Timeslot 16 CAS, transport signaling information in timeslot 16 during frames 1 through 15 of the CAS multiframe. The CAS multiframe structure supports channel associated signaling for 30 of the 32 64 kbps channels in the E1 frame. This structure is shown in Table 25 on page 73.

In E1, all signaling bits represent binary information and the signaling mode is always 16-state signaling.

9.2.3 Per Time Slot Enable

In T1, the IXF3208 allows the user to mark any time slot for transparent signaling or equivalently as a clear channel. A register allows the marking of time slots that do not carry robbed bit signaling. When any of these bits are set to '1' then the corresponding time slot is marked as transparent/clear and robbed bit signaling is not inserted on the transmit side. In the receive side, disabling a bit removes the "signaling change" indication for each of the time slots marked.

In E1 when in CAS mode, the signaling for the 30 channels is transmitted. In Rx direction the user can mark a TS so that the "signaling change" indication for each of the time slots marked is disabled.

9.3 Common Channel Signaling (CCS)

CCS is available in all framing modes for both T1 and E1. In this signaling mode, one or more timeslots are selected to carry signaling data for all other timeslots in the form of an HDLC message. The IXF3208 includes 8 independent HDLC controllers associated to the FDL module, or 24 additional independent HDCL controllers that can be configured for any data rate from 8 Kbps to the entire payload stream. If CCS is desired, then one of these controllers should be assigned to the associated line port and configured to the CCS timeslot(s). The CCS data can then be accessed through the HDLC controller's FIFO by the host processor interface.

9.4 Signaling Access

The IXF3208 provides several methods to access the signaling data: through dedicated backplane signaling ports, in a complete set of signaling registers accessible through the host interface port and transparently in the backplane data streams.

9.4.1 Dedicated System Backplane Signaling Ports

Each backplane port is capable of supporting independent transmit and receive streams. Each stream has data and signaling pins associated, as well as frame and multiframe pulses.

The format of the signaling bits presented to the backplane signaling ports vary according to the signaling mode selected and incorporate the concept of a 4 bit stuff nibble to pad the 4 bit signaling nibble to fill an 8 bit byte. The format of signaling bits presented to the backplane is defined by setting the two Signaling Byte Format Bits (SBFB) as detailed in Table 28 (below).

Table 28. Signaling Byte Format Options

SBFB[1:0]	Signaling Byte[1]
00	SSSS SSSS
01	SSSS ABCD
10	ABCD SSSS
11	ABCD ABCD

NOTES:
1. SSSS as defined by the contents of the Stuff Nibble Definition Register (SNDR). ABCD represents the extracted signaling data.

The value of the stuffing nibble can be defined at the port level or at the DS0 level. When defined at the port level, all the DS0s will use the same stuffing nibble. When defined at DS0 level, each DS0 can carry a different value for stuffing.

9.5 Signaling Processing Options

The IXF3208 supports several signaling processing options: Signaling Freeze and Signaling Debounce, for the information coming from the line side. These features are described in the following sections.

9.5.1 Signaling Freeze

The IXF3208 provides a user selectable signaling freeze capability. This will allow call states to be maintained during brief Out Of Frame (OOF) periods. This function operates as follows:

The signaling bits from two consecutive superframes are collected and buffered internally. Two frames of bits are held in the signaling buffer so signaling integration can be implemented and one frame of bits is held in the output inserters. Once the correct signaling is determined, it is updated in the “stable” region of the debouncing FIFO. From this section, the signaling values are sent to the backplane. Upon detection of OOF, AIS, and LOS, if signaling freeze is enabled, the “stable” section remains unchanged so that the same value will continue to be inserted in their corresponding stream. This condition will continue until the framer achieves frame synchronization and new values are received at least two frames. This will update the stable values.

9.5.2 Signaling Debounce

Signaling debounce can be activated in any signaling mode. This causes the receive signaling buffer to be updated for any channel only if all signaling bits do not change for 2 consecutive multiframes. In SLC-96, the integration period is four twelve-frames multiframes (48 frames).

When debounce is not selected, the operation mode defaults to FIFO. In this case, a three multiframe FIFO is used so that the signaling will start to be output to the backplane only after two full multiframes have been received. The remaining functions like “signaling change” and “freeze” are available.

9.5.2.1 Signaling Force

Signaling can be forced at DS0 level towards the line or the backplane. The user must select the TS to force and set the value. This value will be sent in the selected TS and direction (Tx line or Rx backplane) continuously.

Alarm Handling 10

Alarms are detected and reported via interrupts. Some defects are integrated and the result is designated a failure. These are also reported via interrupts.

The main interrupts provided for both defect and failure conditions are:

LOS	Loss Of Signal (Red Alarm)
AIS	Alarm Indication Signal (Blue Alarm)
OOF	Out Of Frame (Red Alarm)
RAI	Remote Alarm Indication (Yellow Alarm)

In the case of any failure, an integration period is defined to set or clear the condition. The defect indication is set as soon as the event is received.

Other interrupts are provided that reflect detection of anomalies or other events. See the Memory Map Developer's Manual.

Actions are performed under some detected events. The user can program the consequent actions based on certain events.

10.1 Alarm Integration

To declare a failure, the device integrates LOS and AIS by it's internal line decoding circuitry and OOF and RAI by it's internal framing circuit.

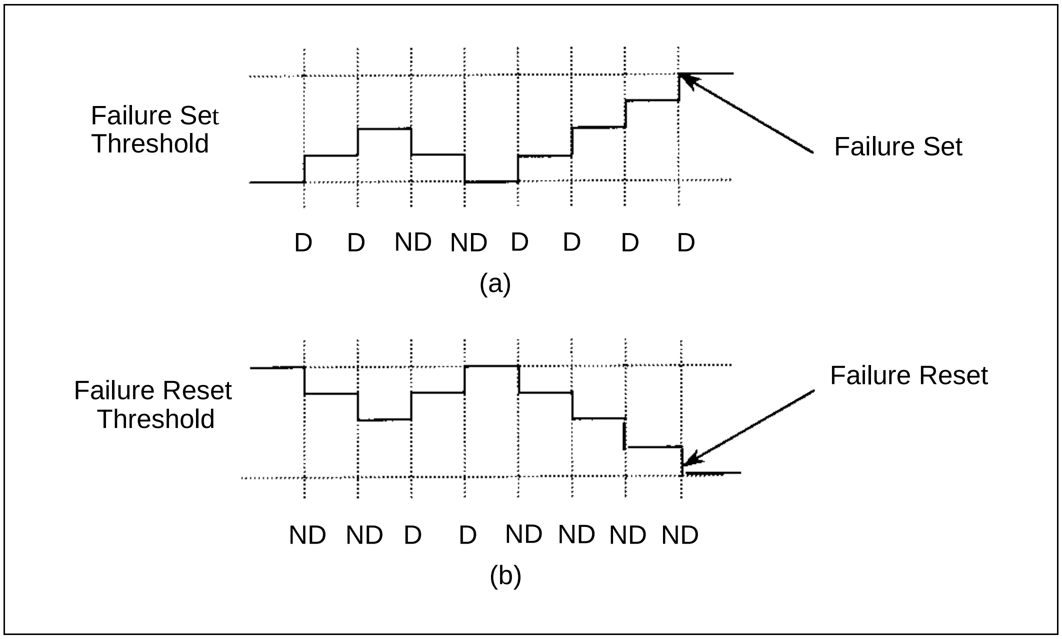
The algorithms used to declare those events are related to the operation mode; T1, E1, J1 and the settings are defined by the user.

The user can define the amount of time that it takes to defect the presence of a failure. Likewise, the user can define the amount of time that it takes to defect the absents of a failure.

The default settings after reset for T1 and E1 are: Set = 2.5 Seconds, Clear = 8.19 Seconds. The user can modify those four values, two for E1 and two for T1 from 125 microseconds up to 8.19 Seconds.

The defect is evaluated in windows of 125 microseconds. When the current state of the failure is "clear" and the defect is found inside of the125 microseconds window, a counter is incremented. If the counter reaches the programmed value, then the "failure set" condition is declared. If before reaching the "set" condition, a window is found with the defect not set, then the counter is decremented by one. In this way some gaps are allowed in the defects.

Figure 11. Set and Clear Counters Behavior



10.2 Alarm Handling

Actions are generated based on the detection of an event. In this case defects and anomalies detected in the receive stream are used to trigger actions that affect the signal going towards the transmit line and the receive backplane streams. In addition, the detection of loop codes can also be used to trigger actions, in this case the setting or removing of loop-backs.

Table 5 shows the actions on the Tx line and Rx backplane sides. Note that actions to perform and priority are both programmable. As an example, AIS and RAI cannot be sent at the same time as a consequent action of LOS. The user should program only one of them. On the other hand, RAI and a codeword can be sent as a consequent action in E1 streams.

- Under out of frame, loss of signal or alarm indication signal conditions, the module sends to the backplane module an AIS/AUXP send indication or user defined pattern indication. The user can select a RAI, AIS or codeword (E1 format) transmission to the line side. When E bits transmission under OOF are enabled, CRC error information will be transmitted.
- Under inter-working condition, the user can select an RAI, AIS or codeword (E1 format) transmission to the line side. E bits might be set.
- Under loss of CAS multi-frame condition the user can select an RAI, AIS or codeword (E1 format) transmission to the line side.
- Under LOS condition and if LOF has not yet occurred, CRC error information will be transmitted.
- If an in-band loop code is detected, the module enable/disable loop indication signal enables or disables the local or payload loopback in the loop module. This signal can be set by hardware (internal in band loop module).

- At any time the host may program any alarm transmission writing the proper values to the module that will send the alarm.

Table 29. Consequent Actions

State on Rx Line	Consequent actions in Tx line	Consequent actions in Rx Backplane
Normal	No action	No action
OOF Out of frame detected in the Rx Framer	Transmit RAI or AIS or AUXP or codeword (E1 mode) E bits can be sent in 0 Sa5 bit value can be defined when sending the codeword (E1) Multiframe AIS can be set (E1)	Send AIS or AUXP or user defined code
LOS Loss Of Signal detected in the line module	Transmit RAI or AIS or AUXP or codeword (E1 mode) E bits can be sent in 0 Sa5 bit value can be defined when sending the codeword (E1) Multiframe AIS or multiframe RAI can be set (E1)	Send AIS or AUXP or user defined code
AIS Alarm Indication Signal detected by the line module	Transmit RAI or AIS or AUXP or codeword (E1 mode) E bits can be sent in 0 Sa5 bit value can be defined when sending the codeword (E1)	Send AIS or AUXP or user defined code
Loss of CRC multi-frame	Transmit RAI or AIS or AUXP E bits can be set to 0. Note: It can be due to the 8ms timer expiring or CRC errors >= 915/320 or after the 400ms timer expires (CRC inter-working)	
CRC4 interworking state	Transmit RAI or AIS or AUXP E bits are set to 0.	

Table 29. Consequent Actions

LOS of CAS multiframe	Send RAI Send Multiframe RAI Send Multiframe AIS	
Reception of Multiframe RAI	Send Multiframe RAI	
Loop up/dn codes	In T1/D4 interrupt mode when the in band pattern 00001 = Activate command is received for 5 ± 0.5 seconds. Then Loop-up is set. The deactivate pattern is 001 also for 5 ± 0.5 seconds. This applies to LLB (per PUB 54016). In T1 ESF mode, BOP sequences will cause LLB or PLB.	

Facility Data Link 11

11.1 Features

- General
- Supports T1, J1 and E1 data link communication
- Per port enable/disable
- Includes an HDLC engine that can be mapped to the overhead bits or to any TS to support Common Channel Signaling (CCS). The HDLC module in the FDL section follows the same operation described for the general HDLC modules.
- E1 specific functions:
  - Supports FAS/NFAS, CRC4 and CAS E1 superframe formats
  - Configurable E1 Sa_n data link bits
- T1 specific functions:
  - Detection/generation of Bit Oriented Codes (BOPs) for T1 ESF and J1-24 streams.
  - Detection/generation of Derived Data Link (DDL) bits for T1 SLC-96
  - T1 ESF PRM detection and transmission

11.2 Functional Description

The FDL module has several sections that handle three types of messages; MOP, On-Chip PRM, BOP, and DDL. The HDLC section is used to detect MOP messages and On-Chip PRM messages. The On-Chip PRM messages are a subset of MOP messages. User-MOP, BOP, and On-Chip PRM can be received in the same data link.

11.3 On-Chip Performance Report Monitoring (PRM)

The On-Chip PRM in a T1 ESF frame is a subset of the complete HDLC LAPD protocol specified in ITU-T Q.921. The frame format is the same, but it uses specific address values. The first three bytes of the On-Chip PRM should be 00111000/00000001/00000011 (MSB to LSB), which is a message from NI or 00111010/00000001/00000011 (MSB to LSB), which is a message from CI.

The information field in a On-Chip PRM message has 8 bytes. The FCS field is of 2 bytes. The On-Chip PRM detector compares the first three bytes of the message and if they match either the NI case or CI case, whatever is programmed by the user, then the 8 information bytes are stored in a register section and an indication is generated.

The on-chip processor reads the On-Chip PRM every second and generates a performance related database. The message is also available for the external host to read.

In the transmission direction, the on-chip processor generates every second, a message that is being sent even if a BOP is currently being sent, that is, the On-Chip PRM has priority over any BOP currently being sent. The BOP will be re-started after the On-Chip PRM is sent. If the external host is sending another MOP using the HDLC FIFO, then the On-Chip PRM is sent only after the HDLC message is completely sent. The external host can take control over the generation of the On-Chip PRM messages by disabling the internal generation of On-Chip PRM.

11.4 Derived Data Link (DDL)

DDL bits are carried by the Fs bits of the SLC-96 superframe format for T1. They conform to the format specified in recommendation TR-TSY-000008 from Bellcore. It is used to transmit control and alarm information. The data link consists of 24 bits that are grouped into the following six fields:

- Concentrator fields (c bits)
- First spoiler field (fixed bits to “0 1 0”)
- Maintenance field (m bits)
- Alarm field (a bits)
- Protection line switching field (s bits)
- Second spoiler field (fixed to ‘1’)

The concentrator field is used to control channel assignment, as well as other functions. The first and second spoiler fields are fixed and used to prevent a wrong framing, due to receipt of an inadvertent signaling framing pattern. The maintenance field is used to control channel and distribution. The alarm field is used to carry alarm information. The protection line switching field is used to control switching of the protection DS1 line.

Derived data link bits are always received when the FDL module is in T1 SLC-96 mode. Information fields are stored in a register section, no further processing is performed.

Table 30. Storing Format for the DDL Bits

Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	C6	C5	C4	C3	C2	C1
2	M3	M2	M1	C11	C10	C9	C8	C7
3	0	0	S4	S3	S2	S1	A2	A1

The DDL bits are stored in three bytes. Once the three bytes have been completely received, they are output to the registers available to the host, in the same format shown in the Table 30 and some status flags updated, reporting that a new DDL message has been received.

The transmission of DDL is done in a similar fashion. There are three bytes available for the external host to write the DDL bits. The FDL module will generate an indication of “new DDL required”. The external host then has 9 ms and one SLC-96 multiframe, to set the values. Once the new DDL is set, it is sent in the next frame. If the host does not change the value of the DDL registers, the same value is sent in every frame.

11.5 Message Oriented Protocol (MOP) HDLC Messages

This module performs the detection of HDLC opening/closing flags (01111110), as well as aborting sequences (1111111). The starting of the HDLC message is declared when a flag is detected and after it a byte different from a flag or an aborting sequence is detected. The closing of the HDLC message is declared when a closing flag (01111110) is detected. At that moment, the received FCS fields are compared with the calculated one. In the transmit direction, it performs the flag insertion, stuffing and CRC generation for the data stored in the FIFO by the user.

11.6 Common Channel Signaling (CCS)

Common channel signaling support is performed by allowing the HDLC section of the FDL module to be mapped to any time slot in the stream. For T1 ESF operation mode, BOP and CCS reception is supported concurrently and for T1 SLC-96 operation mode DDL and CCS is supported concurrently. Note that the HDLC section of the FDL module can be used for this purpose, however, there are also 24 HDLC controllers available to be mapped to any time slot in the HDLC module. The user may also select one of this to handle CCS.

11.7 Bit Oriented Protocol (BOP) Module

A BOP is a sequence of 16 bits that start with eight ones, then 0, then 6 bits that are a code and then another 0: “111111110xxxxxx0”, where “xxxxxx” is a 6-bit BOP code. This module detects sequences of eight consecutive ones and a zero (111111110), then stores the next 6 bits and checks that the last bit is a 0. If that is the case, then a BOP has been received. The BOP is not declared until it has been received N consecutive times, where N is by default 10 and can be programmed by the user from 1 to 15, BOP received indicators are provided. The RAI alarm BOP (00_H) can be handled as a normal BOP, or can be enabled to be declared when 16 consecutive BOP=00Hex have been received.

11.8 Interactions with the Facility Data Link (FDL) Module

A handshake has been defined to interact with the FDL module. The external host has to follow it in order to ensure reliable operation of each section.

11.8.1 Reception of MOP Messages

The reception of the MOP HDLC message follows the same procedure as the one described for the HDLC modules.

There are independent procedures to send MOP, On-Chip PRM, and BOP messages. The transmission of On-Chip PRM or MOP has priority over BOP transmission. Any BOP transmission will be stopped when MOP/On-Chip PRM starts to be transmitted and then the BOP is continued when those messages end.

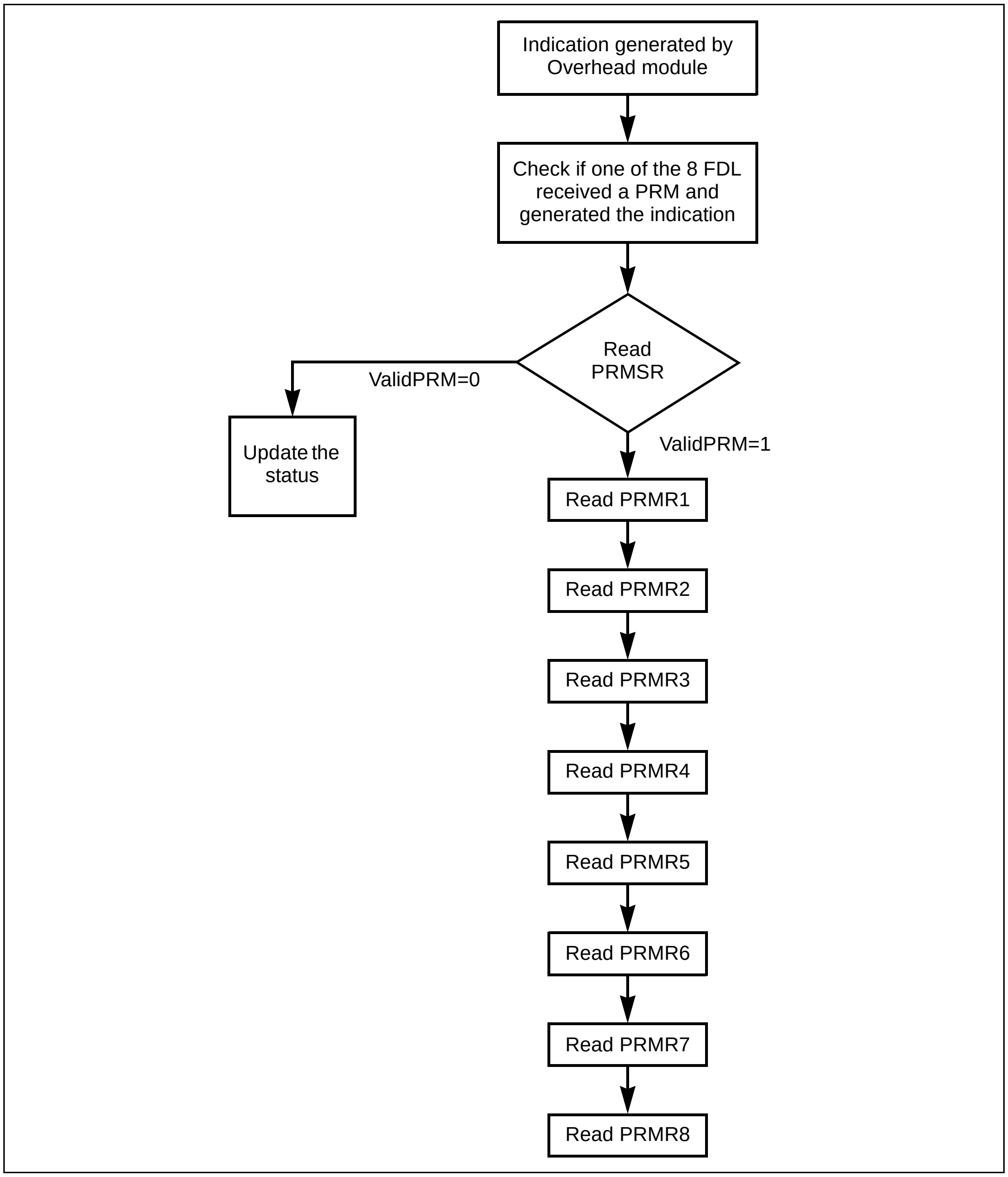
11.8.2 Transmission of a MOP HDLC Message

The transmission of the MOP HDLC message follows the same procedure as the one described for the HDLC modules.

11.8.3 Reception of On-Chip PRM Messages

The user has to enable the detection of the On-Chip PRM and select the three bytes to compare for the message to be recognized as a On-Chip PRM. The default values of those registers are 38/01/03 Hex. When a On-Chip PRM message is detected, an indication is given. Note that the internal CPU will handle the On-Chip PRM unless it is disabled by the user.

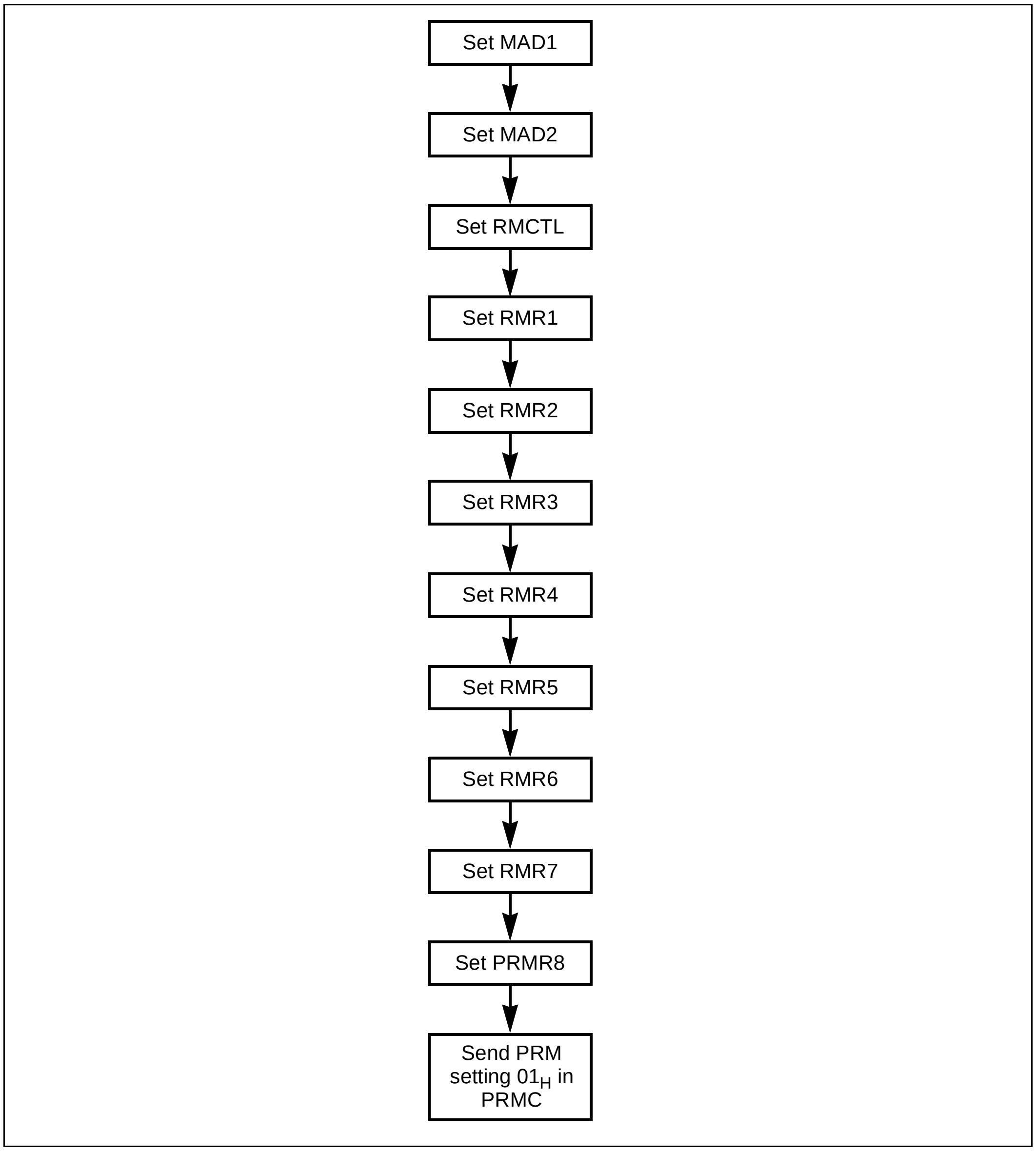
Figure 12. Reception of On-Chip PRM Messages



11.8.4 Transmission of On-Chip PRM Messages

The On-Chip PRM will be generated by the internal Central Processing Unit (CPU) every second. Once the data is generated, it is stored in the transmit section and then sent to the line. The user might select to send the On-Chip PRM from the external host. If that is the case, the eight data registers must be set and the three first bytes and then set the "send PRM" bit. The internal CPU must be commanded not send the PRM, so that the external host has control over those registers.

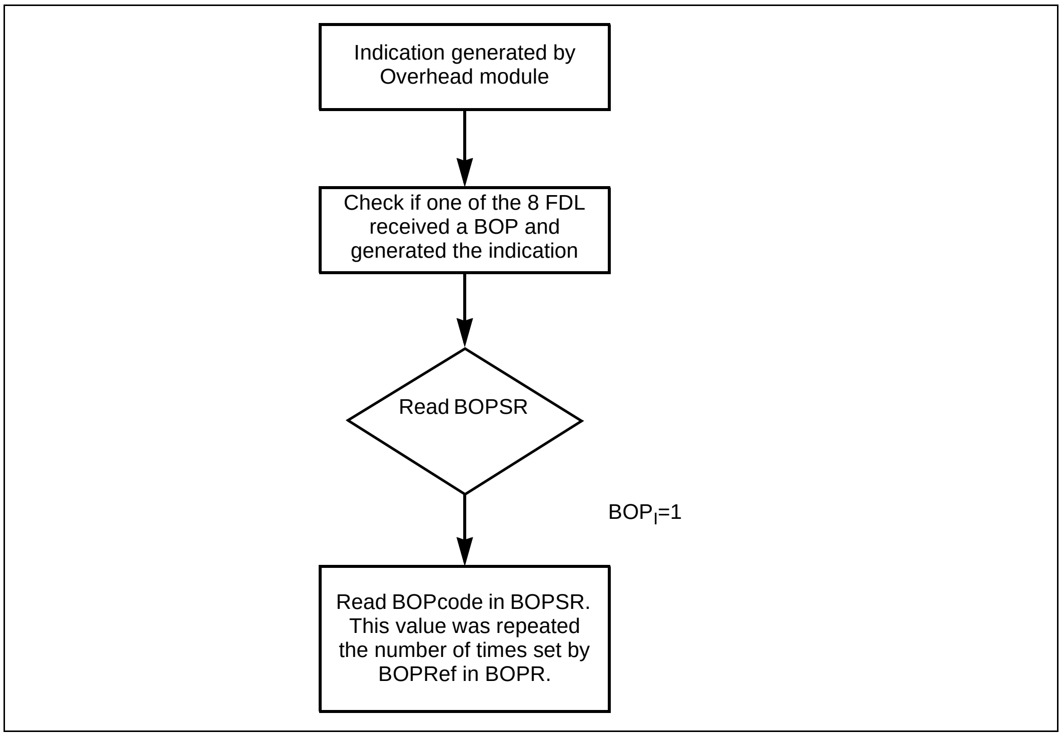
Figure 13. Transmission of On-Chip PRM Messages



11.8.5 Reception of Bit Oriented Protocol (BOP)

Once a BOP is detected to have been present at least N times (1 to 15), as specified by the user, an indication is generated. The user has to check the valid BOP indication and the BOP code. The reception of a BOP code can be checked in continuous mode or with a gap. In continuous mode only when N continuous BOP codes have been received will the BOP code be deemed valid. In the gap mode, if two consecutive BOP codes are detected, then starting at that point a gap of one code is allowed until the counter reaches a count of N. This mode allows for bit errors in the BOP code reception to be supported with a limit of one BOP in error between two good BOP codes detected.

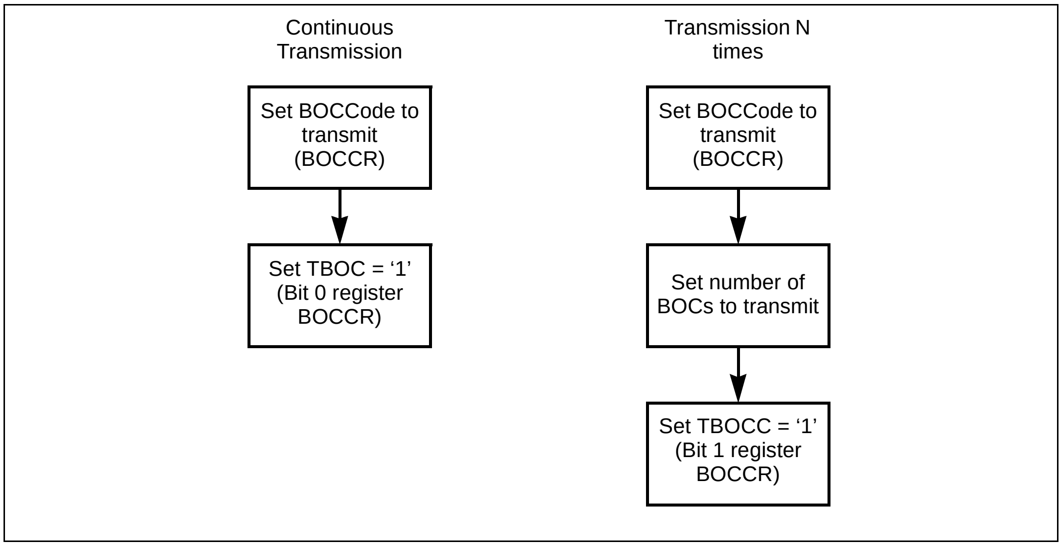
Figure 14. Reception of BOP



11.8.6 Transmission of BOP

BOP transmission can be made in two ways: continuous and by a count reference. The user may select to send a BOP code for a number of times (1 to 65535), or continuous until the sending is removed.

Figure 15. Transmission of BOP



Slip Buffers 12

The slip buffers in this device are always engaged. They can be set to two-frames or minimum delay.

When the mode is selected to minimum delay, the read and write pointers will normally be very close to each other, with an average distance of three time slots. In minimum delay mode, slip operations are indicated but not executed. The indication will mean that an overlap of the pointers has been detected or that the separation has exceeded six time slots. This indication is useful to the user to fine tune the timing settings.

In two frame mode, the operations generated by the slip buffer are:

Slip Repeat:	A frame is repeated
Slip Delete:	A frame is deleted

A re-center process is provided to be performed under host control or whenever a Change Of Frame Alignment (COFA) is detected. The re-center process is performed only on frame boundaries. The Slip buffer waits for the read pointer to be on time slot 0, and then it performs a re-center operation by selecting the best distance between the read and write pointers, depending on the mode. When in two frames mode, the slip buffer will maximize the distance between the read and write pointers and in minimum delay mode, the distance will be minimized. This is done by selecting the proper page for read and write pointers. Two pages are available, each containing one frame.

The re-center process can also be automatically performed whenever a COFA is detected by either the line side or backplane side. This can be enabled by the user. This operation is useful to maintain the pointers separate as much as possible even if change of time slot 0 position happens on either side of the slip buffer. A COFA in the backplane side will be generated if the external device is providing the framing pulse and it’s position is changed.

The slip buffer provides indication of the type of slips happening and maintains information on the number of slips generated in the last second. The counters are updated with the internal one second signal.

The host can also read the distance between pointers at any time. The absolute value is provided.

Backplane Specification 13

13.1 Features

- User defined framed code insertion.
- Unframed AIS and AUXP insertion.
- T1 to E1 channel mapping both in non-fourth time slots and according to ITU-T G.802.
- BERT towards the backplane.
- Serial TDM bus interfaces with fractional streams and stream replication supporting MVIP, H-MVIP, ST, CHI and H.100 at the signal waveform level
- Framing pulse synchronization and data-alignment functions.
- Multiframe pulse propagation to/from the line side through the slip buffers.

13.2 Backplane Interface

The backplane side is connected to the external pins that carry any of the supported bus formats. It is flexible enough to support several bus standards, depending on the chosen set of configuration parameters. The versatility of the backplane module allows easy integration with other devices available in the market.

The backplane side must allow a rate up to 8 times 2.048 Mbps, so that all the eight ports could be output/input in one single serial line. The following formats are supported:

Table 31. Backplane Bus Formats Supported

Bus Format	Complete Name	Source
MVIP H-MVIP	Multi-vendor Integration Protocol High Density MVIP	Global Organization for Multi-Vendor Integration Protocol
H.100 CT Bus	Computer Telephony Bus	Enterprise Computer Telephony Forum
ST-Bus	Serial Telecom Bus	MITEL
CHI (K2, SLD, GCI)	Concentration Highway Interface	AT&T Microelectronics

Channel mapping (T1 to E1), PCM blanking (trunk conditioning), stream replication and AIS insertion are handled by the backplane module.

13.3 Backplane

13.3.1 Supported Bus Standards Description

13.3.1.1 MVIP Bus

The MVIP functionality is described in the following figure. Note that the synchronization pulse is negative and fixed to the first bit of the first TS (TS 0). The signaling byte is “0000ABCD” and it is aligned to each time slot byte. In the Rx direction the data is delivered with the rising edge and the framing pulse is delivered with the falling edge. In the Tx direction, the data is sampled with the falling edge and the framing pulse with the rising edge.

Figure 16. MVIP Delivery (Rx)

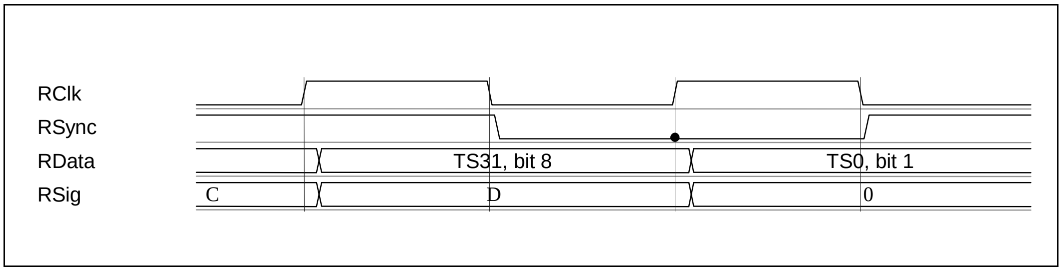
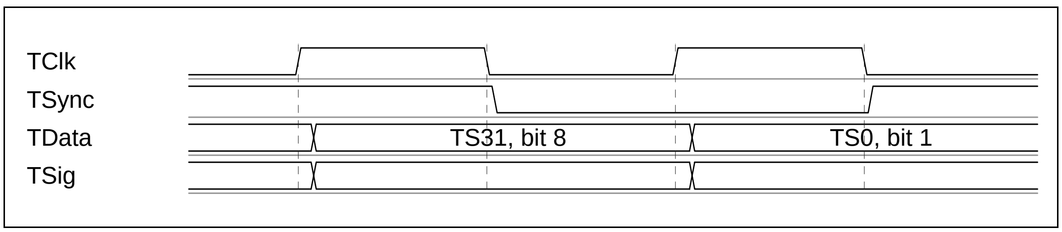
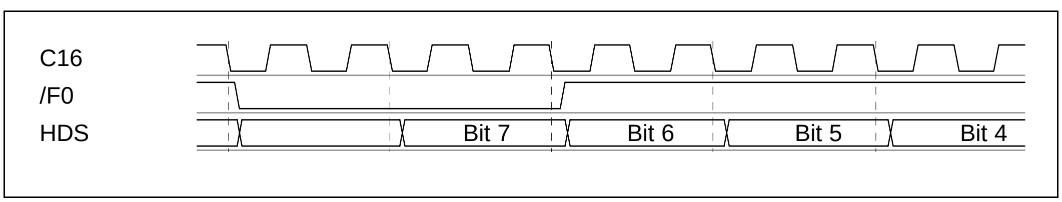


Figure 17. MVIP Sampling (Tx)



The H-MVIP format handles four ports in a single stream. The ports are byte multiplexed. Note that the synchronization pulse is negative, lasts two bit periods and it is fixed to the first bit of the first TS. A 16MHz clock is used, C16 (8 times 2.048 MHz). Note that the data (HDS) and signaling streams are separate. The H-MVIP standard calls for byte interleaving, so that time slot 0 is driven for framer 0, then time slot 0 for framer 1, and so on. Any TS that is not driven should be three stated.

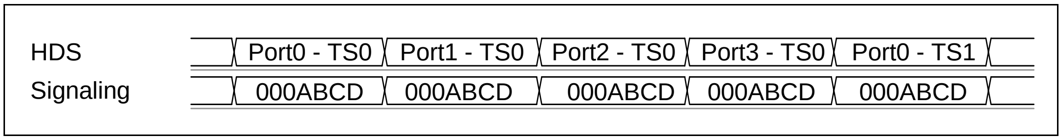
Figure 18. H-MVIP Waveform (Sync-Data)



The data is delivered with the falling edge of C16. The data is sampled with the rising edge of C16, on the second phase.

Each HDS could handle up to four 2.048 Mbps streams, byte interleaved:

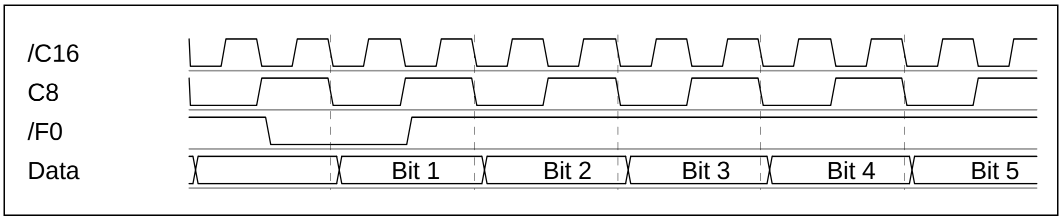
Figure 19. H-MVIP Byte Interleaving



13.3.1.2 H-100 Bus

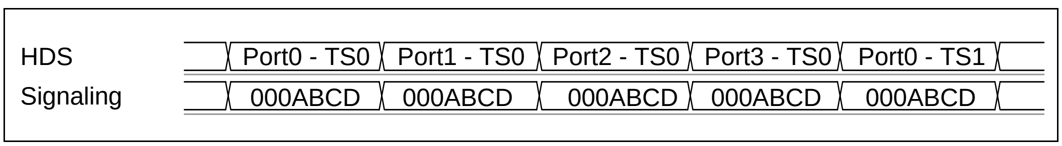
The H-100 functionality is described in the figure. Note that the synchronization pulse is negative and fixed to the first bit (bit 1) of the first TS (TS 0) is used. C16 is a 16 MHz clock signal.

Figure 20. H-100 Waveforms (Sync-Data)



Each Data signal could handle up to four 2.048 Mbps streams, byte interleaved or in any order. There is not any restriction on the mapping. The bus must be considered a 128 TS bus. For a fair delay distribution, a byte-interleaved scheme could be used. The sampling point is on the rising edge of the C16 clock, after the rising edge of the C8 clock. Data is delivered with the rising edge of /C8 (falling edge of C16). Any TS that is not driven should be three stated.

Figure 21. H-100 Byte Interleaving



13.3.1.3 1.544 Mbps ST Bus

The RData/TData bus has 193 bits per frame and each frame is repeated every 125 µs. The signaling byte is “0000ABCD”. The upper nibble has a default value of “0000” but it could be configured with a user-defined value. The edge to sample and deliver data and sync can be programmable. The sync pulse polarity and position can also be programmed. The sync pulse will last one clock cycle.

Figure 22. ST Buses Wave Forms

13.3.1.4 2.048 Mbps ST Bus

The RData/TData bus has 256 bits per frame and each frame is repeated every 125 µs. The signaling byte is “0000ABCD”. The upper nibble has a default value of “0000”, but it could be configured with a user defined value in the Rx direction. The edge to sample and deliver data and sync can be programmable. The sync pulse polarity and position can also be programmed. The sync pulse will last one clock cycle.

13.3.1.5 CHI Bus

The bus requires the data pins to be three state after power-up/reset. The data can be sampled/delivered with either the rising or falling edge of the clock. Also, the sync pulse can be sampled/delivered with either edge. In CHI, the position of the first bit of TS0 can be specified relative to the framing pulse. Some limitations apply, however, the positions are separated by clock transitions. The allowed locations are 3, 4, 5, 6...16, 17, 18.

In one mode of operation, the clock can be run at twice (2x) the data speed. If 2x is selected, the data is driven two clock cycles. In this mode, the data is sampled only on the clock edge defined by the user, any of the four edges available in the bit slot. In the 2x mode, the clock edges to deliver and sample can only have the following values:

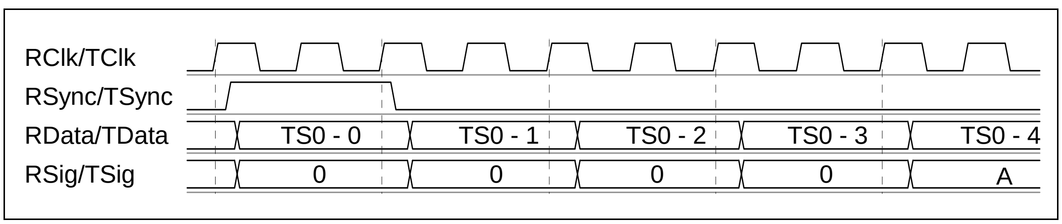
Delivery: 3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28, 31 and 32.

Reception: 6, 7, 10, 11, 14, 15, 18, 19, 22, 23, 26, 27, 30, 31, 34 and 35.

CHI supports the following modes:

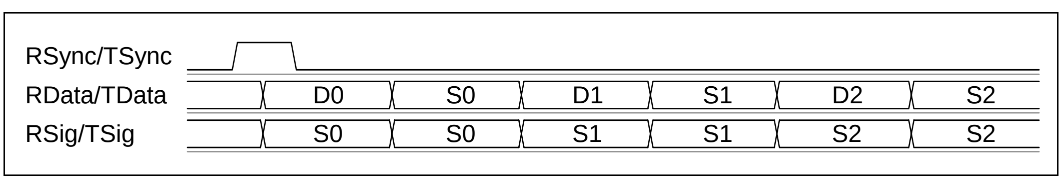
- Data only streams at 1x.
- Data only streams at 2x, 4x.
- Data stream with associated signaling at 2x or 4x.

Figure 23. CHI Bus Data Only Stream at 1x



This structure has 32 TS (256 bits) in a 125 microseconds frame. In this case, data is delivered as one bit every clock cycle. The E1 stream fits completely in this structure. In the case of T1, the 24 time slots are mapped either one-in-four or G.802.

Figure 24. CHI Bus Data Streams with Associated Signaling at 2x



This structure has 32 TS in a 125 microseconds frame. In this case, each TS is of 16 bits, eight of data and eight of signaling.

13.3.2 Byte Replication

This is a feature that allows the replication of a byte in the backplane stream in any of eight possible positions. The user can define replication of 2x, 4x, and 8x. In either case, the user has to define in which of the replicated positions the data is to be driven. In the rest of the positions, the pin is three stated. As an example, if 4x replication is used, then the user can select positions 0, 1, 2 or 3 to be the slot where the data is driven. As an example, if the selected slot is 2, then positions 0,1 and 3 will be three stated. In this way, a higher speed bus can be generated by externally connecting several ports and properly selecting the replication slots. As an example, H-MVIP waveforms could be constructed by selecting 4x replication in ports 2,4,5,6 and connecting them together externally.

13.3.3 Concentration Modes

A mode called “concentration” is supported. In this mode, four and eight channels can be output in one pin. In the 4x mode, the pin associated to port 0 outputs the data related to ports 0,1, 2, and 3. The pin associated to port 4 outputs the data of ports 4, 5, 6, and 7. The data is output in a byte interleaved mode, with the byte of port 0 first, then the byte of port 1, etc.

In the 8x mode, the pin associated to port 0 outputs the data of the eight ports, byte interleaved with port 0 byte first, then the byte of port 1, etc.

The interleaving is done internally to the chip. H-MVIP waveforms could be generated in pins 0 and 4.

13.3.4 Data Mapping

An internal per TS source mapping can be used to engage BERT and HDLC modules in either Rx or Tx direction. In the Rx direction, the mapping is used to determine if the source of a particular channel is to be the data from the line side or the BERT, or any HDLC controller. This data can be the whole byte or just some bits, one to eight. In this way, BERT or HDLC messages can be sent to the Rx backplane pins.

In the Tx direction, the data in the backplane pins can be sent to the BERT or HDLC functions, in addition to the line side. Also, the whole byte or just some bits can be sent to those modules.

13.3.5 Byte Enforcements

This applies to the Rx direction only. All the ports may overwrite their normal data stream with a specific pattern (8 bits). This will allow for functions such as PCM blanking, trunk conditioning, and AIS/AUXP insertion.

13.3.5.1 User Specific Patterns

Upon specific maintenance conditions a framed pattern (all-zeros, all ones, etc.) will be transmitted towards the backplane. The data bytes obtained from the RxSlipBuffer will be substituted by the byte in the user configurable register.

13.3.5.2 AIS or AUXP Insertion

Upon specific maintenance conditions an unframed all-ones or 1:1 code will be transmitted towards the backplane. The data bytes obtained from the RxSlipBuffer will be substituted by this pattern.

13.3.6 T1 to E1 Mappings

Two T1 to E1 mappings are supported channel; channel to channel and G.802.

13.3.6.1 Channel to Channel Mapping

With this method, a 1.544 Mbps signal can be accommodated within the E1 structure in a channel per timeslot basis, where TS0 carries the f-bit information and then whenever TS mod 4 <> 0 a T1 CH is inserted in the E1 stream:

TS0 - F bit, TS1-CH1, TS2-CH2, TS3-CH3, TS4-x, TS5-CH4, TS6-CH5, TS7-CH6, TS8-x, TS9-CH7, TS10-CH8, TS11-CH9, TS12-x, TS13-CH10, TS14-CH11, TS15-CH12, TS16-x, TS17-CH13, TS18-CH14, TS19-CH15, TS20-x, TS21-CH16, TS22-CH17, TS23-CH18, TS2 4-x, TS25-CH19, TS26-CH20, TS27-CH21, TS28-x, TS29-CH22, TS30-CH23, TS31-CH24.

Table 32 shows the mapping between the time slot number (upper row) and the T1 channel. Example: TS1 maps to channel 1. TS5 maps to channel 4, etc.

Table 32. T1 to E1 per Channel Mapping

ts0	ts1	ts2	ts3	ts4	ts5	ts6	ts7	ts8	ts9	ts10	ts11	ts12	ts13		ts18	ts19	ts20	ts21	ts22	ts23	ts24	ts25	ts26	ts27	ts28	ts29	ts30	ts31
fb	ch1	ch2	ch3		ch4	ch5	ch6		ch7	ch8	ch9		ch10		ch14	ch15		ch16	ch17	ch18		ch19	ch20	ch21		ch22	ch23	ch24

T1 CH structure within the E1

13.3.6.2 ITU-T G.802 (Annex B) Mapping

In this method, the 193 bit structure to be accommodated within the E1 structure does not need to have a particular arrangement, such as channels. The 193 bits of an arbitrary 125 µs period of the 1544 kbps signal should be accommodated within a structured 2048 kbps frame.

Table 33 shows the mapping between TS and 193 bits that make up the complete T1 frame.

E1 TS structure

Table 33. T1 to E1 G.802 Mapping

ts0	ts1	ts2	ts3	ts4	ts5	ts6	ts7	ts8	ts9	ts10	ts11	ts12	ts13	ts14	ts15	ts16	ts17	ts18	ts19	ts20	ts21	ts22	ts23	ts24	ts25	ts26	ts27		ts31
fas	120 bits																72 bits									1 bit			

193 bit stream within the E1

In the Rx side case, the device will store the F bit in TS26 bit 0, then channel 1 in TS1, Channel 2 in TS2 up to channel 15 in TS15, then channel 16 is stored in TS17, and so on up to channel 24.

The memory map is organized such that the first global control section contains the information of the whole 8 ports regarding reset, interrupts and status. Each port is mapped such that the user just has to add an offset to a base address to get access to similar information on each port.

Timing Configurations 14

Timing configurations deal with two aspects of the device configuration; clocks and frame pulse selection.

The sources for the clock configurations are:

- Rx line clock
- Rx and Tx backplane clocks
- External clocks from E1x24 or T1x24 pins, divided down to 1x.
- Signal from the PLL whose input is the Rx line clock or Tx backplane clock

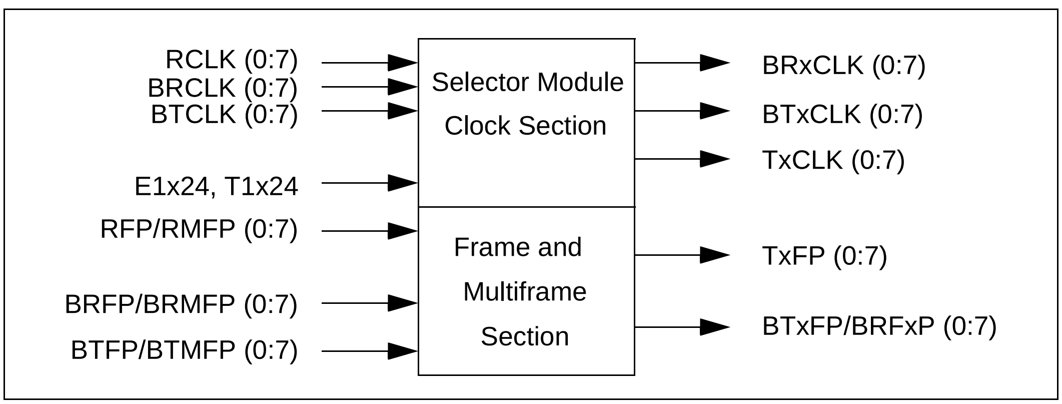
The sources for the framing pulse configurations are:

- Rx line side
- Rx and Tx backplane pins
- Internally generated signals

There are two PLL modules available, one for Rx and one for Tx.

All of the timing information is concentrated in one module, from where it is distributed to all of the other regions.

Figure 25. Inputs and Outputs of the Selector Module



14.1 PLL Modules

There are two PLL modules available; RxPLL TxPLL.

The RxPLL uses the external E1x24 or T1x24 clocks to lock to any of the Rx line clock signals of the eight ports. The output of this module is PLLClkRx.

The TxPLL uses the external E1x24 or T1x24 clocks to lock to any of the Tx system backplane clock signals of the eight ports. The output of this module is PLLClkTx.

The PLL modules divide the reference signal to 8 KHz and perform the adjustments on phase after comparing the 8 KHz_reference and the 8 KHz generated signal. The adjustment is done by shifting the phase by one clock period E1x24 or T1x24.

14.2 External Clocks

There are two pins for external clock sources; E1x24 and T1x24. This allows for clocks 1x, 8x, 16x and 24x base frequencies on T1 or E1.

Those signals are used in two modules; an internal divider to 1x and as the high speed clock for the PLL modules.

The output of the dividers are DivT1 and DivE1.

14.3 Internal Clocks

A couple of internal clocks, ClkIntA and ClkIntB, are generated from the following sources:

- Rx line clocks (eight ports)
- Tx backplane clock (eight ports)
- DivT1
- DivE1

The internal clocks are available to all the Rx and Tx backplane modules and to the Tx line module. The use of the internal clocks is for having a common timing configuration distributed to all the ports.

14.4 Rx Backplane Clock Configuration

The Rx backplane clock can be the input to or output from the device. When selected as an output, the sources are:

- Rx line clock from the same port
- Internal clocks; ClkIntA, ClkIntB
- The output of RxPLL

14.5 Tx Backplane Clock Configuration

The Tx backplane clock can be the input to or output from the device. When selected as an output, the sources are:

- Rx line clock from the same port
- Internal clocks; ClkIntA, ClkIntB
- The output of RxPLL

14.6 Tx Line Clock Configuration

The Tx line clock sources are:

- Rx line clock from the same port
- Tx backplane clock from the same port
- Internal clocks; ClkIntA, ClkIntB
- The output of TxPLL

14.7 One Second Clock Configuration

The internal one-second clock signal can be generated from the following sources:

- Rx line clock from any of the eight ports
- Tx backplane clock from any of the eight ports
- External clocks: T1x24, E1x24

The one second signal is used internally to load registers with performance data such as framing, bit errors, bipolar violations, etc. It is also used to interrupt the internal processor to gather data every second. The one second signal can also be used to enable an interrupt with this same period.

14.8 Reference Clock Configuration

The reference clock is an output to a dedicated pin. The sources are:

- Rx line clock from any of the eight ports

14.9 Rx Backplane Frame Pulse Configurations

The Rx backplane frame pulse can be an input to or output for the device. When selected as an output, the sources are:

- Rx line frame pulse from the same port
- Internal free-running generator using the Rx backplane clock

14.10 Tx Backplane Frame Pulse Configurations

The Tx backplane frame pulse can be an input to or output from the device. When selected as an output, the sources are:

- Rx line frame pulse from the same port
- Internal free-running generator using the Tx Backplane Clock

14.11 Tx Line Frame Pulse Configurations

The Tx line frame sources are:

- Rx line frame pulse from the same port
- Internal free-running generator using the Tx line clock
- Tx backplane pulse from the same port

14.12 Rx Backplane Multi-Frame Pulse Configurations

The Rx backplane frame pulse is an output and is generated from the Rx line multiframe.

14.13 Tx Backplane Multi-Frame Pulse Configurations

The Tx backplane frame pulse is an input from an external device.

14.14 Tx Line Multi-Frame Pulse Configurations

The Tx line frame sources are:

- Rx line multi-frame pulse from the same port
- Internal free-running generator using the Tx line clock
- Tx backplane multi-frame pulse from the same port

14.15 Backplane and Transmit Line Clock Source Selection

This section describes in an schematic form the options to select the clock source for the backplane and transmit line sides. It also shows some examples on how some selections could look like.

Figure 26. Clock Selections

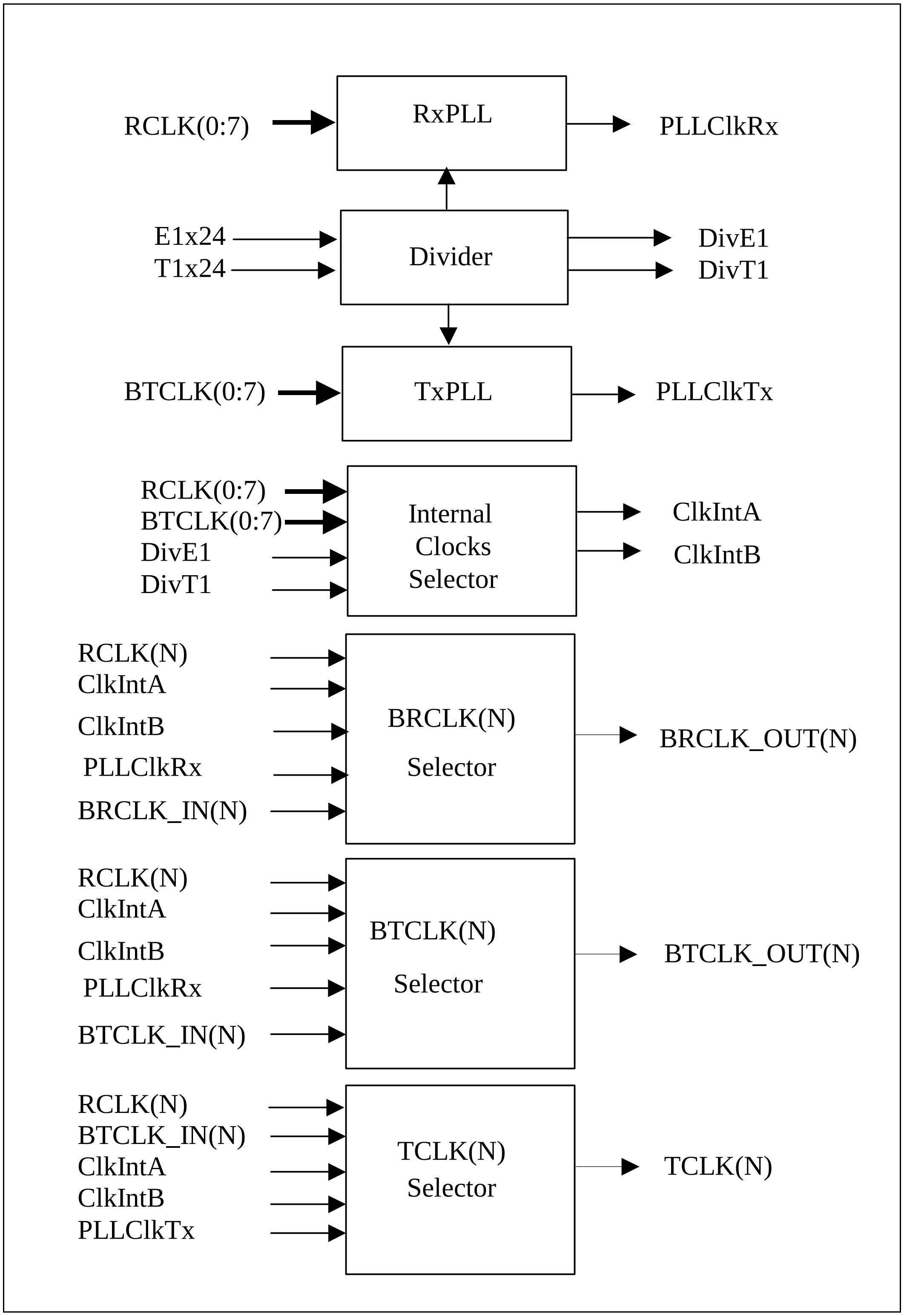
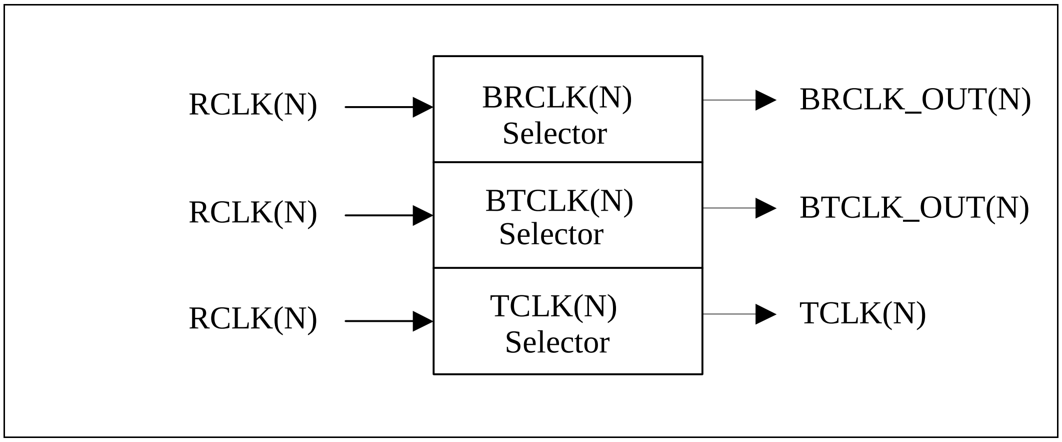
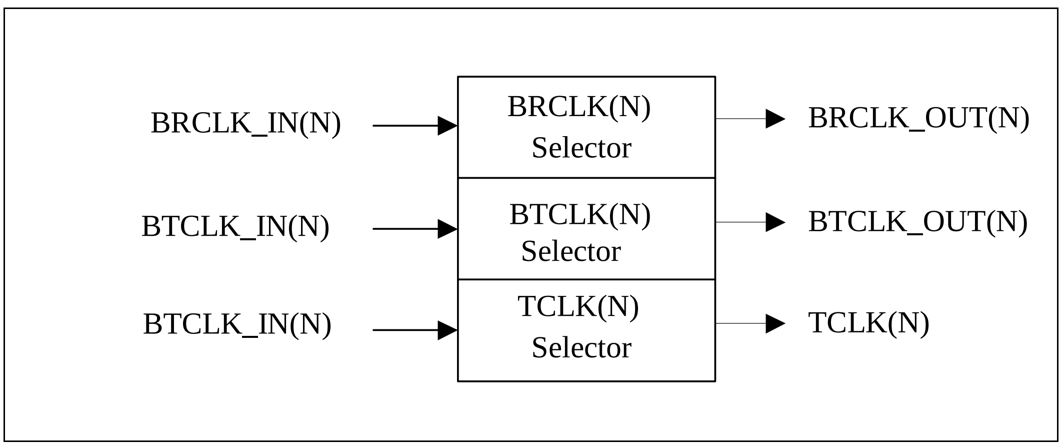


Figure 27. Port N Configuration



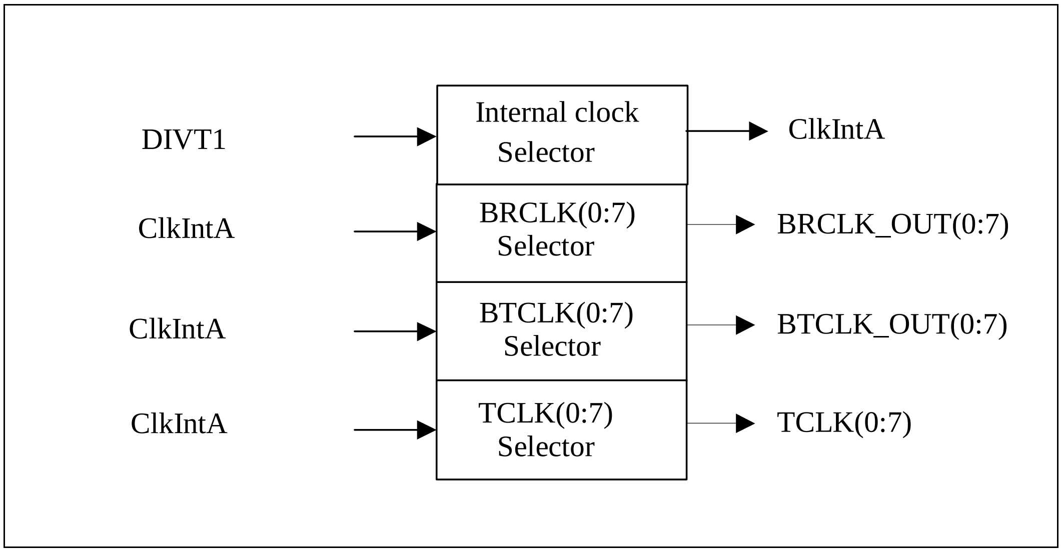
All clocks are driven from the RCLK source. In this case the master timing reference comes from the Line side; Received line clock.

Figure 28. Port N Configuration



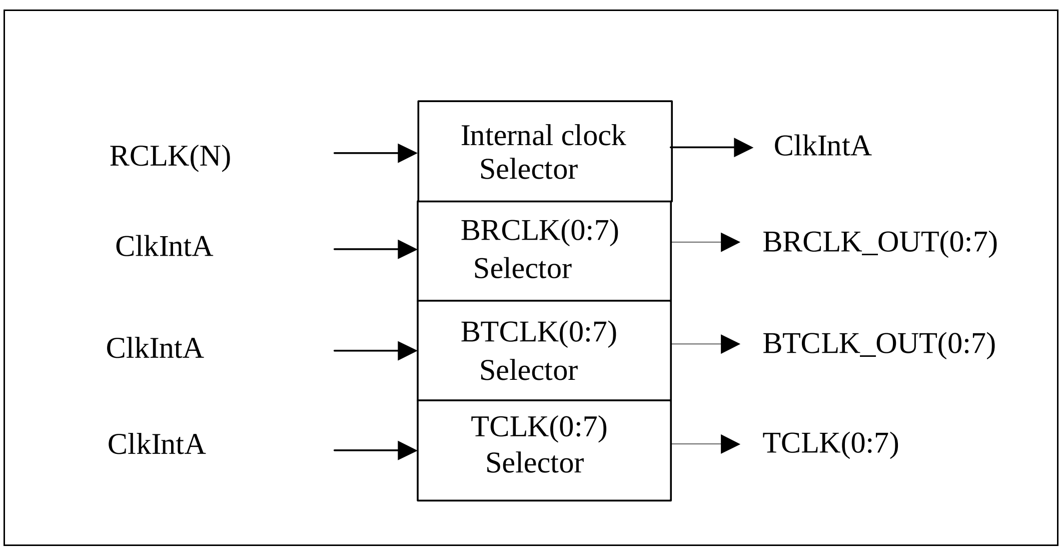
TCLK is generated from BTCLK. BRCLK and BTCLK come from an external source. In this case the master timing source is provided at the backplane pins by an external device

Figure 29. T1 x24 Clock



All clocks are generated from ClkIntA. In this case a local T1x24 clock is the master timing reference. The T1x24 clock frequency can be MxT1, where M=1, 8, 16 or 24.

Figure 30. All Ports with Common Clock



Example of all ports being configured with a common clock source; the line clock from port N. All clocks are generated from ClkIntA. In this case one receive line clock is the master timing reference

LoopBacks 15

There are four types of loopbacks in the device:

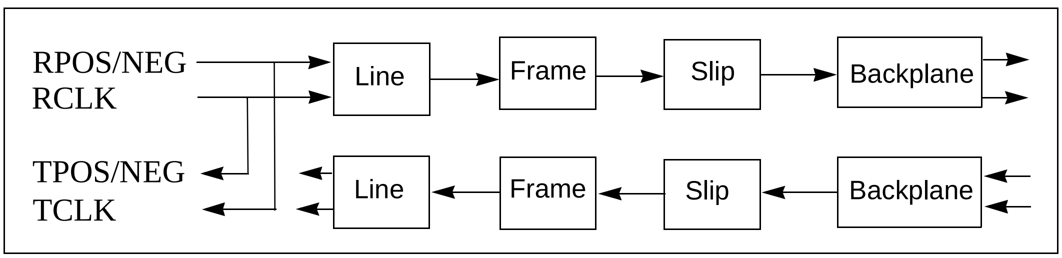
Line Loopback	LLB
Payload loopback	PLB
Digital loopback	DLB
Time slot loopback	TLB

15.1 Line LoopBack (LLB)

The line loopback is performed by returning the data and clock from the receive line pins to the transmit line pins. No processing is done to the data. The LLB behaves like a wire between Rx and Tx line ports.

The data and timing information is all sent to the Rx path in addition to looping it back.

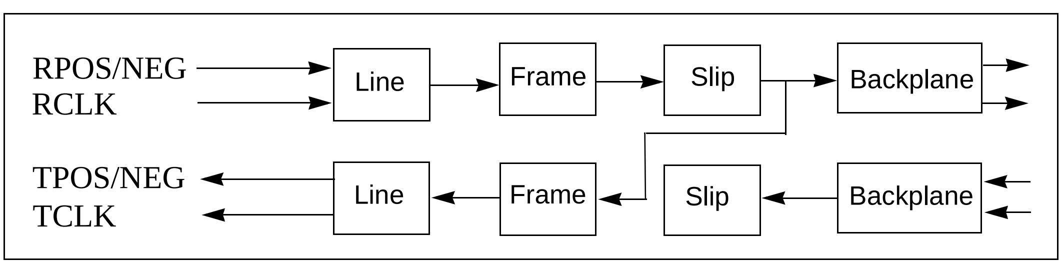
Figure 31. Line Loopback



15.2 Payload LoopBack (PLB)

The payload loopback is performed by returning the payload data from the receive path to the transmit data pins. This is done after coding, framing and storage in the Rx path buffers. Also after framing and coding in the Tx path. Any code violations are removed. The frame structure is re-generated and the data is transmitted using the user programmed clock for the Tx line side.

Figure 32. Payload Loopback

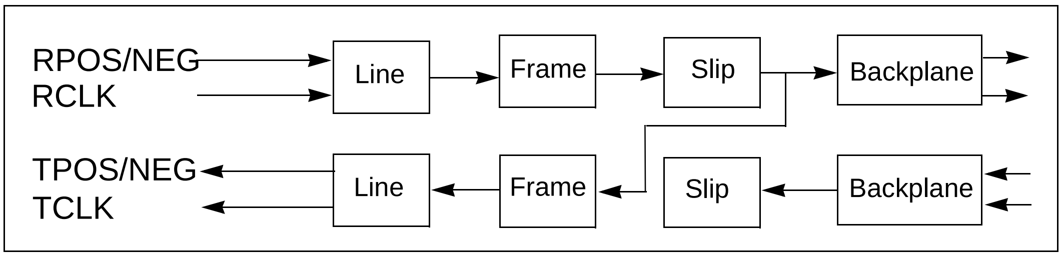


15.3 Time slot LoopBack (TLB)

The time slot loopback is similar to the PLB, with the difference that it is performed on a per time slot basis. Any number of time slots can be selected. The TLB is performed by returning the data from the receive path to the transmit data pins. This is done after coding, framing and storage in the Rx path buffers. Also after framing and coding in the Tx path.

Any code violations are removed. The frame structure is re-generated and the data is transmitted using the user programmed clock for the Tx line side. The user can select any number of TS to be looped back.

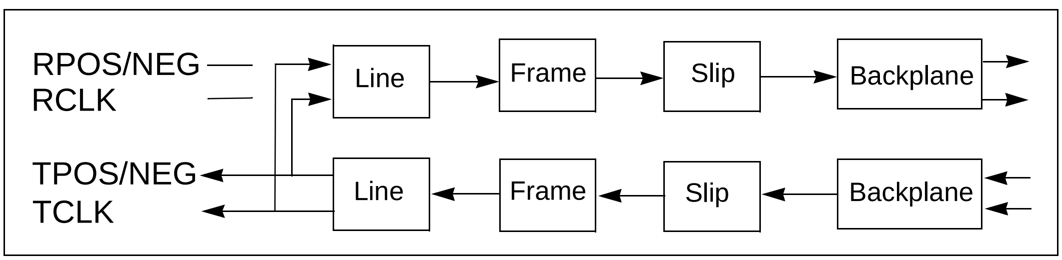
Figure 33. Time Slot Loopback



15.4 Digital LoopBack (DLB)

The digital loopback is performed by returning the data and clock going to the Tx line pins to the Rx line inputs.

Figure 34. Digital Loopback

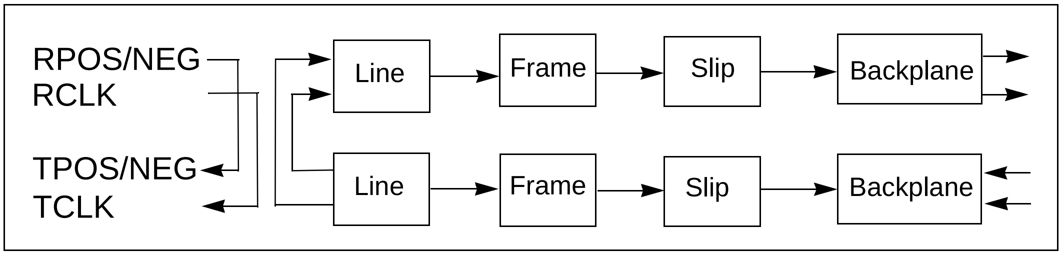


Note: For digital loopback to work properly, the clock source for the Tx line path must be other than the Rx line clock of the same port.

15.5 Dual LoopBacks

The digital loopback and the Line LoopBack (LLB) can be performed at the same time.

Figure 35. Dual Loopback



15.6 Priorities in the Loopbacks

LLB has priority over PLB and TLB.

PLB has priority over TLB.

DLB has priority over PLB and TLB.

LLB and DLB can be set at the same time.

Bit Error Rate Tester (BERT) 16

The Bit Error Rate Tester (BERT) module can be used to test the whole T1/J1/E1 port or sections of it. This circuitry provides on-chip functions that can be used to test the quality of the links. Up to eight simultaneous tests can be done in multiple time slots and ports. Generation and analysis capabilities are provided and can be used with repetitive or pseudo-random bit sequences (PRBS). Multiple BERT modules are available and can be used in any time slot of any port.

The BERT module has eight pattern programmable generators and analyzers. The generators consist of eight PRBS, eight Digital milliwatt (DmW) and eight Digital Reference Signal (DRS) sections. Each generator or analyzer can be associated to any set time slots in any port. The eight pattern generator/analyzers support pseudo random and repetitive sequences of up to 32 bits. The user must program the TS associated to the selected BERT module.

The analyzer has a programmable threshold to declare in-sync and out-of-sync states. Bit error counters and total bit counters are also provided to calculate bit error rates. Detection of all 0s or all 1s is also supported.

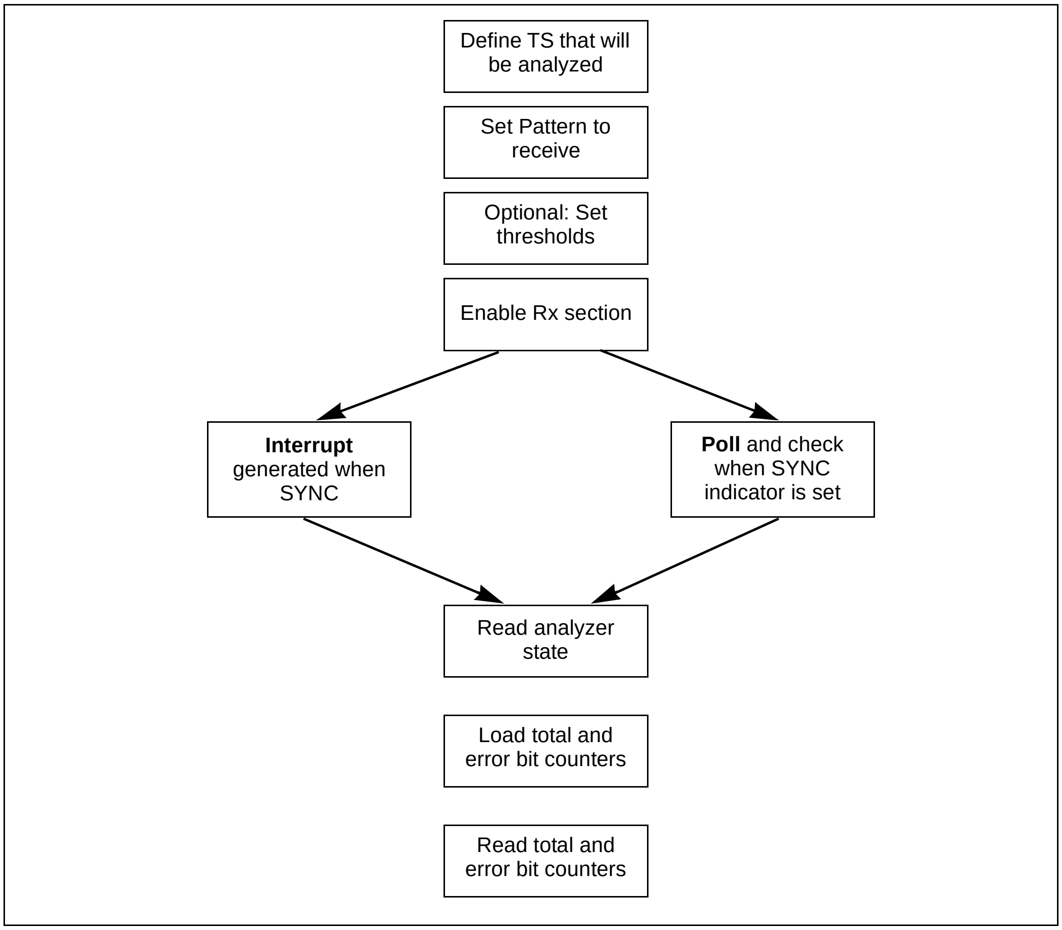
16.1 BERT Analyzer

To use any of the analyzers, the sequence to follow is:

- TS Mapping.
- Associate the selected time slots to the selected BERT analyzer (0 to 7).
- A mask can also be used to select only bits of each time slot.
- BERT configuration.
- Program the receive pattern in the selected BERT module. Set type, length, invert, etc.
- If a change in thresholds is required, set the new thresholds to declare sync and out-of-sync. The default values are:
  64 consecutive bits matching the expected pattern will declare sync.
  Ten or more errors in a window of 100 bits will force out-of-sync.
- Enable the selected analyzer.

At this point, the analyzer is receiving the information. The BERT will generate an indication when synchronization is achieved. The user can then check the error rate by checking the total bit counter and the error bit counters. Note that the maximum count of those counters is 2^{24}, so the host should read them faster than that, in order to avoid overflow of the counters. Assuming the highest rate, 2.048 Mbps, then overflow should be reached after achieving synchronization in around 8 seconds. It is suggested that the host read those counters every second. Note, there is an option that loads the counters automatically ever second (an internal one second pulse). After being loaded, the counters must be read only. Alternatively, the counters can be loaded (commanded by the external host) by setting the LOADC bit. After that, the values are ready in the host accessible total count and error bit counters. The internal counters are re-started when the LOADC bit is set.

Figure 36. BERT Analyzer



Note: The programming of the time slots is done in a region of memory different to the BERT region.

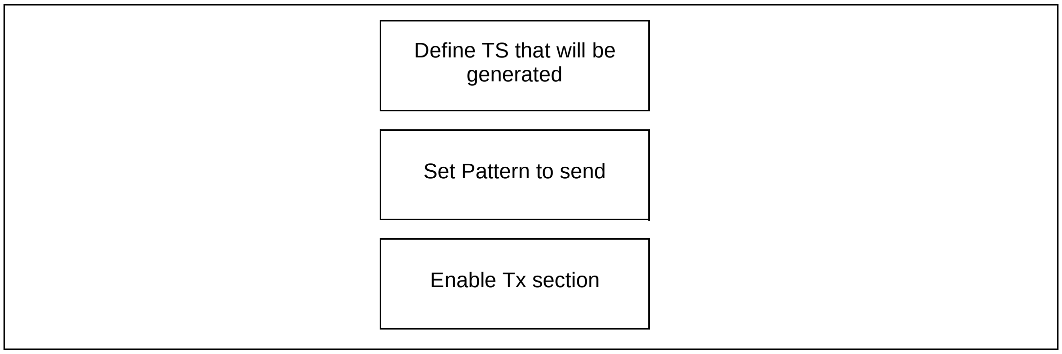
16.2 BERT Generator

To use any of the programmable generators, the sequence to follow is:

- Associate the selected time slots to the selected BERT generator (0 to 7). A mask can also be used to select only certain bits of each time slot.
- Program the pattern to send. Set type, length, invert, etc.
- Enable the selected generator.

At this point the generator is sending the information.

Figure 37. BERT Generator



To use any of the fixed generators, that are DmW or DRS, the sequence to follow is:

- Associate the selected time slots to the selected BERT generator (0 to 7). The pattern will be sent into the whole time slot. Masking bits is not allowed for DRS and DMW codes.
- Program and enable the generator to output A-law or µ-law codes.

Note: The programming of the time slots is done in a region of memory different to the BERT region.

16.3 Supported Patterns

The eight BERT generator/analyzers support Pseudo-Random Bit Sequence (PRBS) and repetitive patterns of up to 32 bits. There are 7 registers that have to be programmed to define the pattern to send/receive.

Reg. Name	Width	Description
PS (0 to 3)	7:0	Pattern configuration
LR	4:0	Pattern length From 00 to 1F Hex. 00 means length of 1. 1F Hex means length of the pattern is 32.
TR	4:0	Pattern Tap. For PRBS only. For repetitive use 00 Hex. From 00 to 1F Hex indicates the bit position where the TAP is located. 0 indicates the first flip flop.
CTR	3:0	Used to define PRBS, QRSS of if the pattern is inverted in the Tx or Rx direction. (0) QRSS 1=It is a PRBS with QRSS circuitry (1) PBRS 0=Repetitive, 1=PRBS (2) INV Rx (3) INV Tx

Table 34. BERT Pattern Selection

Number	Pattern	Ctr	tr	lr	ps3	ps2	ps1	ps0
00	2^3-1	02	00	02	FF	FF	FF	FF
01	2^4-1	02	00	03	FF	FF	FF	FF
02	2^5-1	02	01	04	FF	FF	FF	FF
03	2^6-1	02	04	05	FF	FF	FF	FF
04	2^7-1	02	00	06	FF	FF	FF	FF
05	2^7-1 (T1 LB Activate)	02	03	06	FF	FF	FF	FF
06	2^7-1 (T1 LB Deactivate)	0E	03	06	FF	FF	FF	FF
07	2^9-1	02	04	08	FF	FF	FF	FF
08	2^{10}-1	02	02	09	FF	FF	FF	FF
09	2^{11}-1	02	08	0A	FF	FF	FF	FF
0A	2^{15}-1 (Not Inverted)	02	0D	0E	FF	FF	FF	FF
0B	2^{15}-1 (O.151)	0E	0D	0E	FF	FF	FF	FF
0C	2^{17}-1	02	02	10	FF	FF	FF	FF
0D	2^{18}-1	02	06	11	FF	FF	FF	FF
0E	2^{20}-1 (O.153)	02	02	13	FF	FF	FF	FF
0F	2^{20}-1 (O.151 QRSS)	03	10	13	FF	FF	FF	FF
10	2^{20}-1	02	10	13	FF	FF	FF	FF
11	2^{21}-1	02	01	14	FF	FF	FF	FF
12	2^{22}-1	02	00	15	FF	FF	FF	FF
13	2^{23}-1	02	11	16	FF	FF	FF	FF
14	2^{25}-1	02	02	18	FF	FF	FF	FF
15	2^{28}-1	02	02	1B	FF	FF	FF	FF
16	2^{29}-1	02	01	1C	FF	FF	FF	FF
17	2^{31}-1	02	02	1E	FF	FF	FF	FF
18	All Ones	00	00	00	FF	FF	FF	FF
19	All Zeros	00	00	00	FF	FF	FF	FE
1A	Alternating (101010...)	00	00	01	FF	FF	FF	FE
1B	Double alternating (0011...)	00	00	03	FF	FF	FF	FC
1C	D4 Line LB Deact. (1:3)	00	00	02	FF	FF	FF	FC
1D	1:4	00	00	03	FF	FF	FF	F4
1E	D4 Line LB Act. (1:5)	00	00	04	FF	FF	FF	F0
1F	1:7	00	00	06	FF	FF	FF	81
20	1:8	00	00	07	FF	FF	FF	40
21	1:16	00	00	0F	FF	FF	40	00
22	3:24	00	00	17	FF	44	00	04
23	User Defined	User	00	User	User	User	User	User

HDLC Controller 17

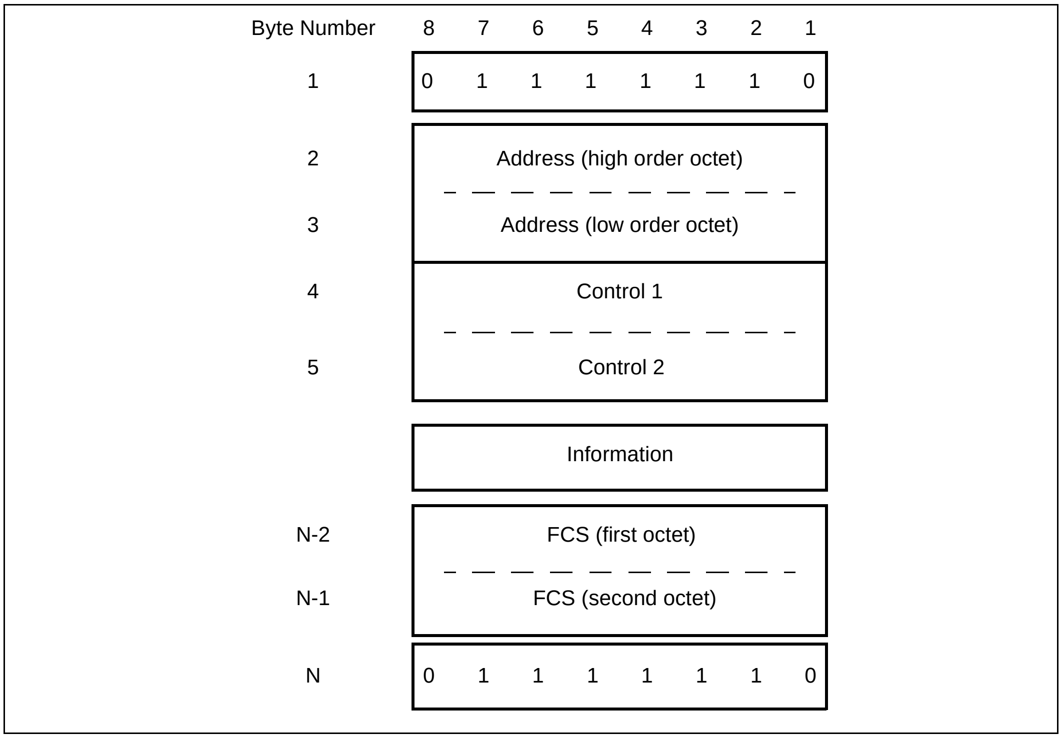
17.1 Features

- Twenty four HDLC modules available
- Each module can be assigned to any port in any combination of TS of the same port
- Sub-rate is supported using a mask to define which bits to use
- Supports all T1, J1 and E1 frame formats
- Two 128 byte FIFOs per module, one for Rx and the other for Tx
- Up to four messages can be stored in each FIFO in either Rx or Tx direction
- Status information is provided for each message and the FIFOs
- Detection/generation of start/end flags for HDLC link messages
- Detection/generation of Frame Check Sequence (FCS) for HDLC link messages
- Zero stuffing/destuffing for HDLC link messages
- Short messages detection (less than 2 bytes)
- Abort character detection and transmission capabilities
- LAPB, LAPD, LAPV5 or transparent operation modes
- Address matching and message filtering support
- Frame Check Sequence (FCS) checking/generation can be enabled/disabled
- In transparent mode, byte alignment is provided
- Messages above the Maximum Frame Length specified are aborted

17.2 Functional Description

Messages are signals conforming to an HDLC protocol, LAPD, LAPB or LAPV5, as defined in ITU-T recommendations Q.921 and G.964. The messages are filtered according to the address field of the HDLC message. The frame format for this protocol is shown in Figure 38.

Figure 38. HDLC Frame Format



All frames must start and end with the flag sequence, consisting of one 0, then six contiguous 1s and finally one 0. The closing flag can also be the opening flag of the next frame, in some applications. The address field identifies the entities establishing the data link. The address field description for LAPD and LAPV5 are shown in Figure 39 and Figure 40.

Figure 39. Address Field Format for LAPD Messages

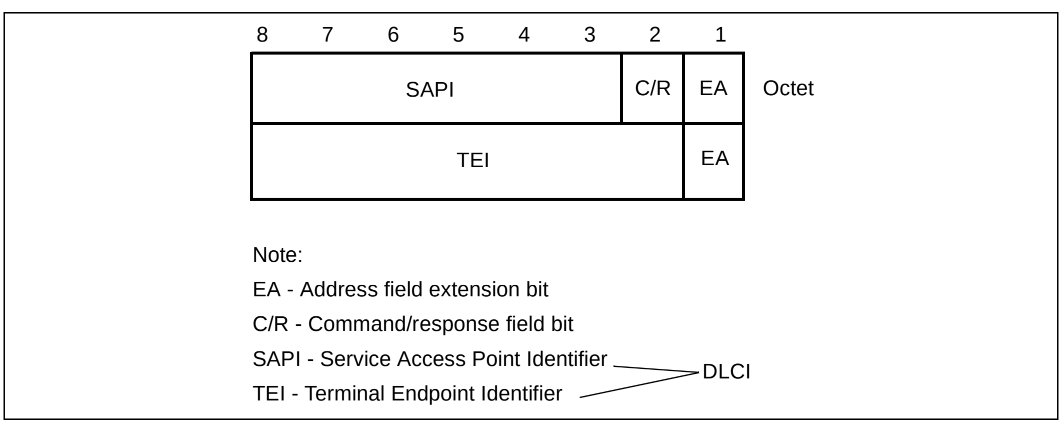


Figure 40. Address Field Format, for a LAPV5 Message

8	7	6	5	4	3	2	1	
EFaddr						C/R 0	EA 0	Octet
EFaddr							EA 1	

Note:
EA - Address field extension bit
C/R - Command/response field bit
EFaddr - Envelop field address

The EA bit indicates the final byte of the address field. If set to one, it indicates that the address field octet is the final octet of the address field. The double octet address field for LAPD operation shall have bit 1 of the first octet set to a 0 and bit 1 of the second octet set to 1. The C/R bit indicates if the message is a command or a response. The SAPI and TEI fields are used to address a point and terminal equipment that is being serviced with the data link procedures. For LAPB messages, the address field is one byte long (the first address byte) and for LAPD and LAPV5 the address field is two bytes long. For LAPV5 messages, the address field is composed of the bits EA, CR and the field EFaddr, which can take values from 0 to 8191, and serves the same purpose as the SAPI and TEI fields.

The control field identifies the type of frame, and whether it is a command or a response. This control field has one or two bytes, depending on the type of frame. The information field (if any) shall consist of an integer number of bytes. The Frame Check Sequence (FCS) is a CRC16 checksum of the data between the opening flag and the FCS field. A deeper description of each field can be found in recommendations Q.921 and G.964 of the ITU-T.

To avoid the situation of opening/closing flags between them, zero stuffing is performed. The zero stuffing procedure consists in the insertion of a 0 when a sequence of 5 consecutive 1s is found in the fields between the opening and closing flag. De-stuffing is done by removing any 0 found after five consecutive 1s in the fields between the opening and closing flag of the frame. An HDLC message is aborted if a sequence of seven or more 1s are received in any of the frame fields.

A new HDLC frame is detected when a flag is received and sequences different from flags or 1s are being received (information bits). A closing flag is detected when information bits are received and a flag sequence is detected. While the HDLC module is receiving information bits, it performs zero destuffing and finally checks the FCS field. The received bytes are stored in a 128-byte FIFO, excluding flags or interframe sequences. Status signals are updated, which indicate if an error was received, the length of the message, or if an abnormal receive termination took place.

The HDLC module can perform address filtering. Four bytes are used to compare the received message address with the expected one; address-low-1, address-low-2, address-high-1, and address-high-2. Address matching can be enabled/disabled in any mode. In LAPB mode only address high 1 and 2 are used for comparison. In LAPD mode the four address bytes are used, such that any combination of address-high and address-low will be received; 1-1, 2-2, 1-2 and 2-1. For LAPV5 mode, the comparison is made only for the two least significant bits of the first address byte (C/R and EA), which must be equal to “0 0” respectively, and for the least significant bit (EA) of the second address byte, which must be equal to “1”. If the comparison matches the expected value, then the entire message is received and processed, otherwise it is discarded.

If the operation mode is configured to be LAPB and the address byte received is all ones, it is taken as a broadcast address and the message is taken as a valid one. If the operation mode is configured to be LAPD and the TEI sub-field of the address field is all 1s, it is taken as a broadcast address and the message is taken to be a valid one. LAPV5 operation mode does not support broadcast addresses.

If transparent mode is configured, then no flag checking, no destuffing, and no FCS checking are performed, that is, all the bytes are sent to the FIFO. Byte alignment can be provided in this mode, such that the data in the time slot is stored aligned in the data byte FIFO. For the transmission side, the bytes stored in the Tx FIFO are sent aligned to the time slot bits. Note that for the alignment to occur, the whole time slot must be used to carry the data.

For the receive side, up to four messages can be stored before being retrieved by the external host. As soon as one message is received, an indication is generated to the host. Reception can continue even if the host has not read the first message. A FIFO of up to four status messages is associated with the data FIFO. Once the host reads the first message, it informs the HDLC module, so that the next status can be presented to the host. As an example, messages of size 32, 16, 54, and 6 bytes could be stored. Note that the limitation is that the total number of bytes should not be more than 128 bytes. The host should read the messages before the data FIFO (128 bytes) or status FIFO (4 status) overflow can occur.

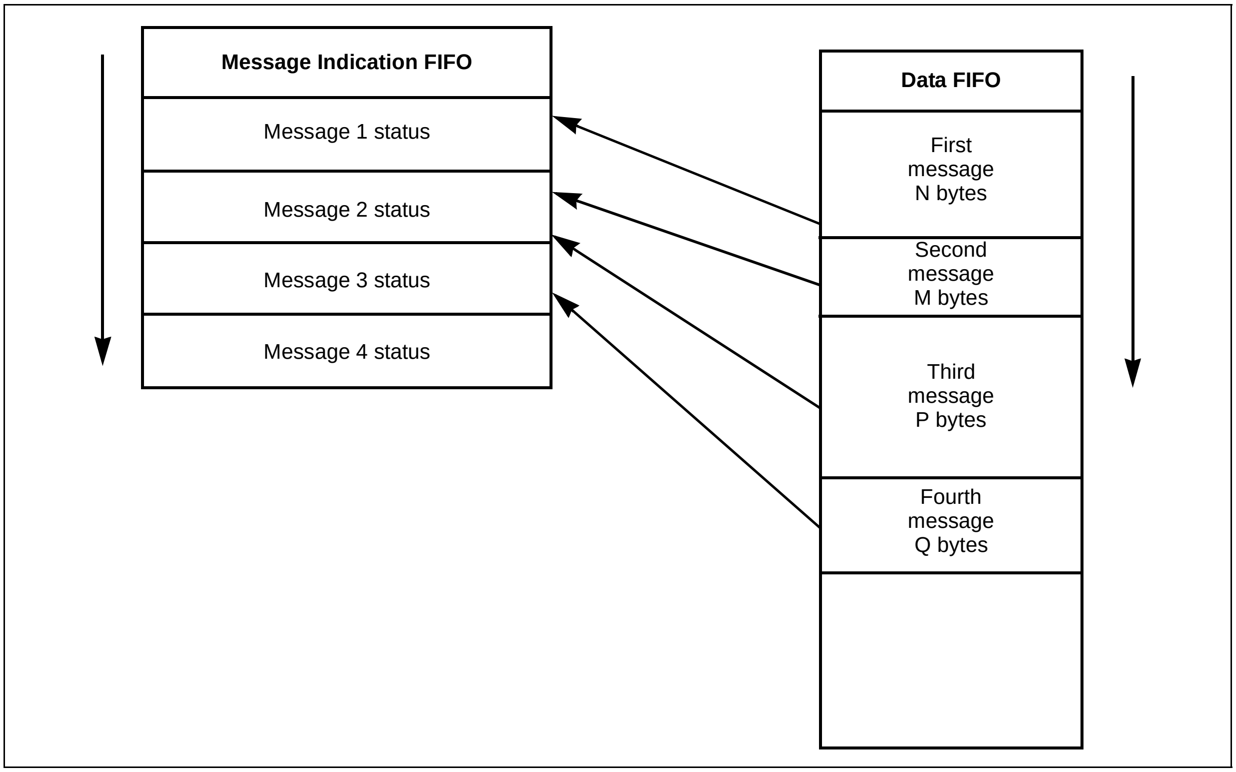
In the transmission side, the host can store up to four consecutive messages, provided the total length is not more than 128 bytes.

The HDLC message reception can be aborted for different causes: a sequence of seven or more consecutive ones is received in the information field, a FIFO overflow or underflow, or the maximum message length parameter is reached. In transmit side, a message can be aborted only if instructed by the user.

17.3 Reception of a Message

Each of the HDLC engines has a 128 byte data FIFO and a 4 status message FIFO. The status message FIFO stores the End Of Message (EOM) or Half indication from the message being received. If another message is received before the previous one is read, then the next location of the status message FIFO is used to store the new status. In this way four back-to-back messages can be received as long as the total message size is below 128 bytes. A half indication is generated when the first 64 bytes of a message are received. Note that if the message is above 64 bytes, then one or more status messages will be half and the last status will be EOM. The status message FIFO, as well as the data FIFO wrap around once they reach the limits.

Figure 41. HDLC Message Reception Process



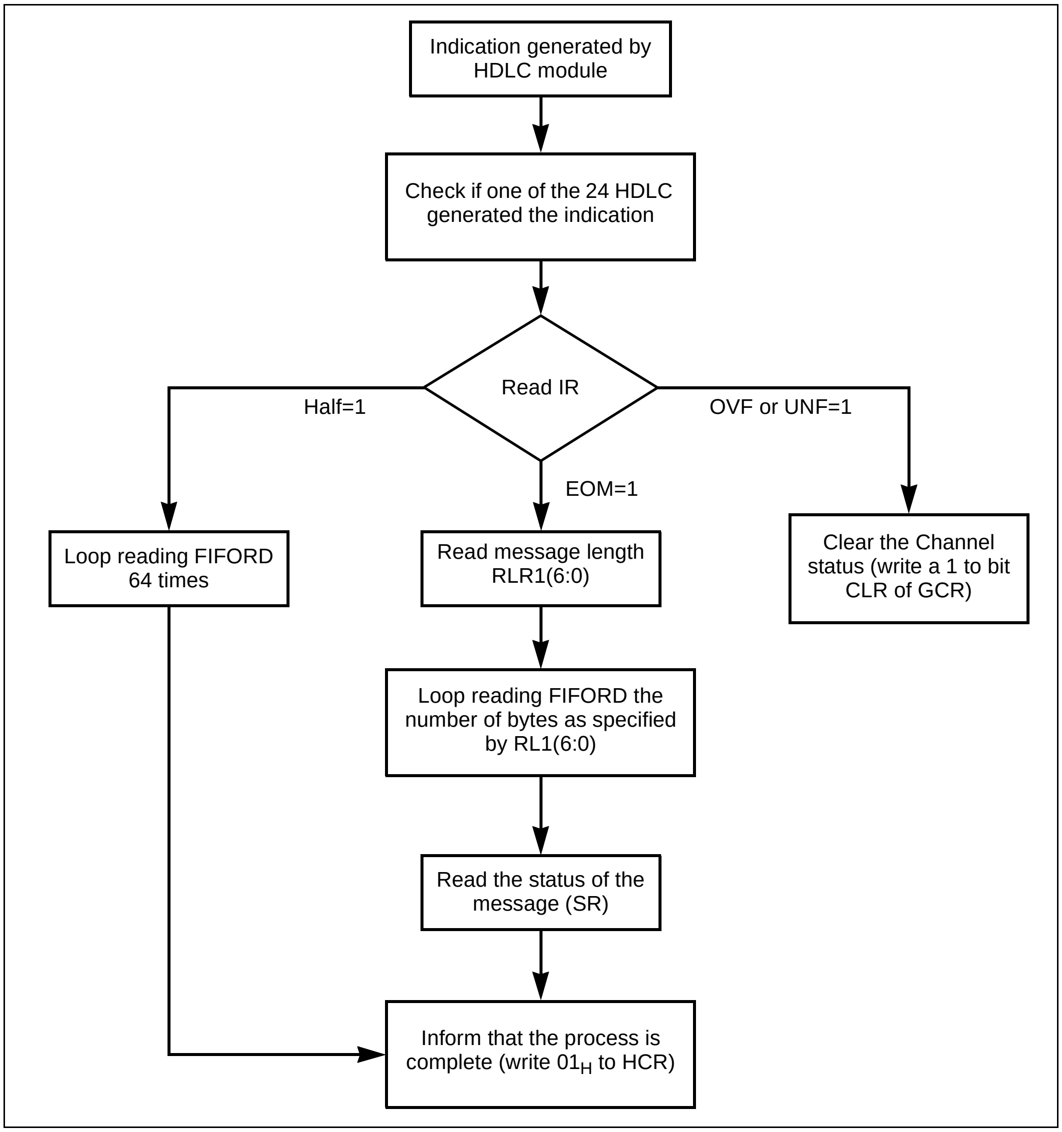
Each indication is used to request service by the external host and generates an interrupt if enabled. The external host can decide to work on interrupt based mechanisms or polling based for which the indication bits can be used.

Once the indication is set (and the interrupt generated), the host must service that indication by checking the HDLC component that generated it.

17.3.1 Reading a Received Message

The external host has to read the status registers and the data FIFO, and then indicate the completion of the service by setting a “process complete” bit in the HDLC module. The way the Rx engine works is that it stores the message bytes in the FIFO until it reaches 64 bytes (HALF) or End Of Message (EOM) and then generates the corresponding indication information.

Figure 42. Reading a Received Message



The EOM is generated when the last byte of the message is received. Half is set when the 64 bytes have been received and it is not EOM. Over Flow (OVF) is generated when the data FIFO is full, 128 bytes, and a new data byte is being received. It is also generated when there are already 4 messages stored in the status message FIFO and a new status is generated. Under Flow (UNF) is generated when the host performs a read data operation when the FIFO is empty.

17.3.2 Steps to Configure the Receive HDLC Path

The configuration process is described in the following section. It is assumed that all the modules have already been configured to the proper format and operation conditions. The following description applies only to HDLC specific functions.

a) Configuration of the HDLC module.

The module must be enabled before starting operations. Configure the module to receive LAPB, LAPD, LAPV, or transparent. If LAPB or LAPD was selected, then program the addresses to match: AddressHigh1, AddressLow1, AddressHigh2, and AddressLow2.

b) Configuration of time slots mapped to the HDLC module.

Assign the TS carrying data to be mapped to the selected HDLC. The TS can be configured to carry plain data (default), HDLC, or BERT data. Any number of TS of the same port can be assigned to the selected HDLC module. TS from different ports are not allowed to be mapped in the same HDLC module.

Note: HDLC data can be received from the line or the backplane.

Define the mask to use in every selected TS. A mask can be used so that sub-rate streams can be supported. Any combination of bits is available. Once the mask is selected, it applies to all the TS in that port.

c) Optionally, enable the interrupt generation for events in the selected HDLC.

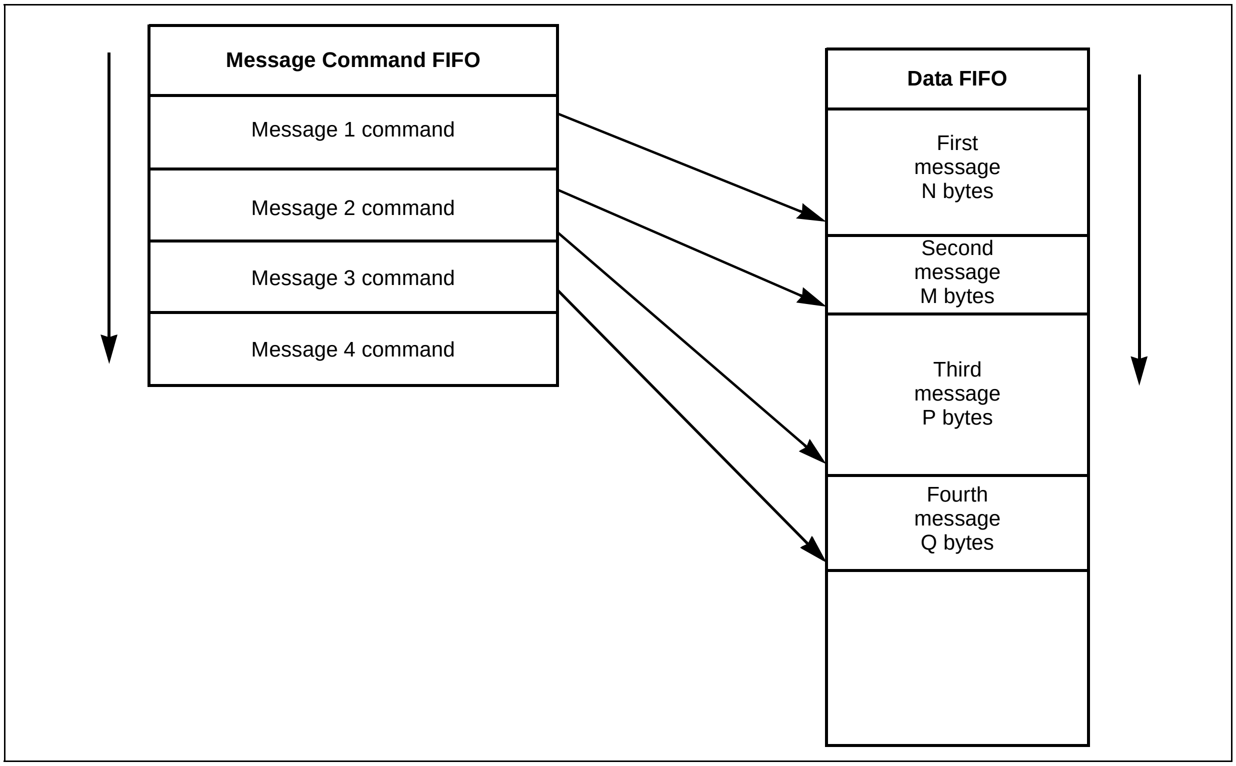
Enable the interrupt of the selected HDLC.

At this point, the HDLC path is configured and messages can be received.

17.4 Transmission of a Message

Each of the HDLC engines has a 128 byte data FIFO and 4-message command FIFO. The message command FIFO stores the End Of Message (EOM) or Half commands from the current message that is to be transmitted. If another message is required to be stored for transmission before the previous one is sent, then the next location of the message command FIFO is used.

Figure 43. HDLC Message Transmission Process



In this way, four back-to-back messages can be stored as long as the total message size is below 128 bytes. Note that if the message is above 64 bytes, then one or more commands will be half and the last one will be EOM. The message command FIFO, as well as the data FIFO, wrap around once they reach the limits.

When 64 bytes are to be transmitted in a message, a “HALF” command is generated. When the end of the message has to be transmitted, the “EOM” command is generated. If the message size is exactly 64 bytes, then only one EOM command is generated.

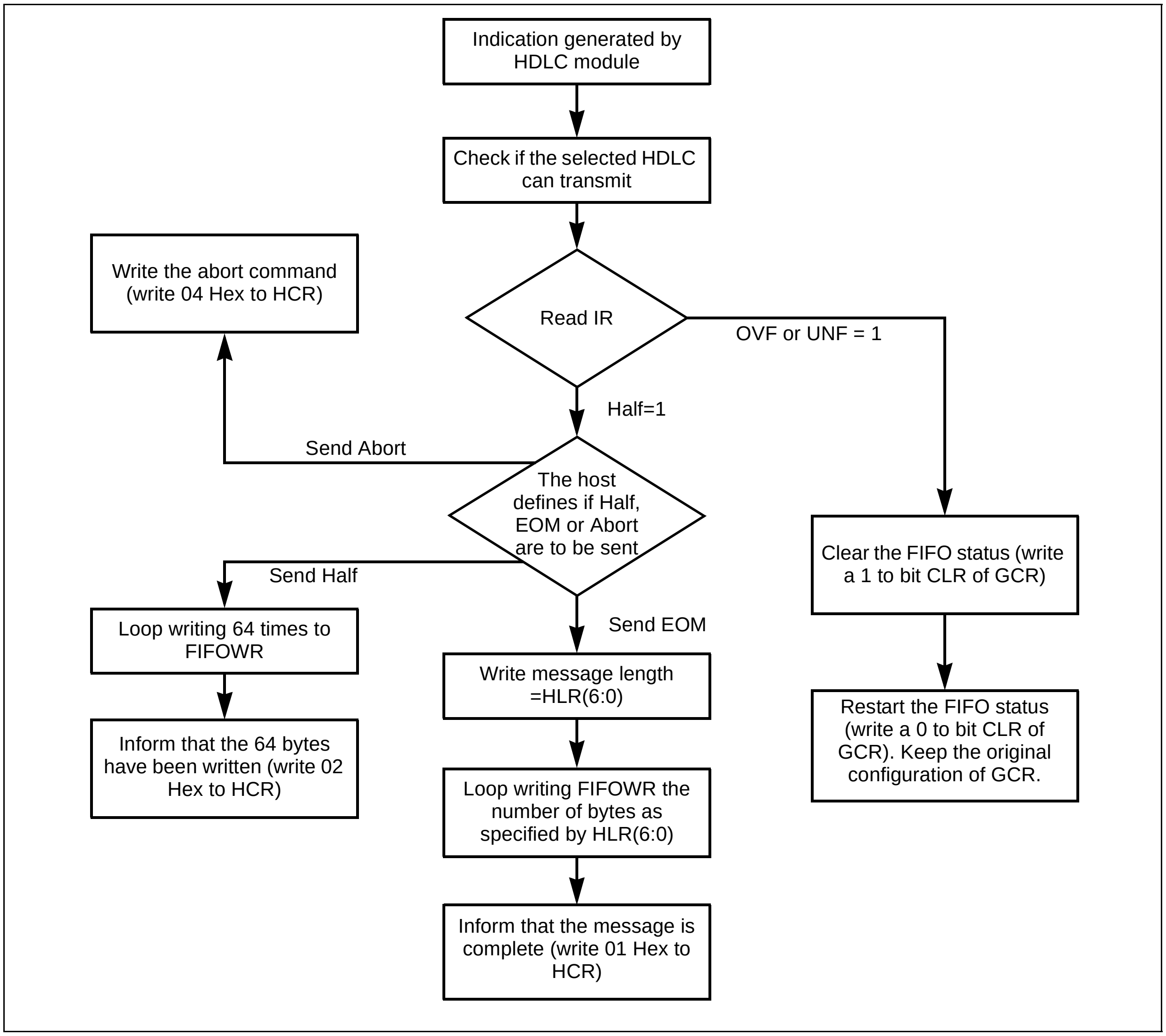
The HDLC module will inform the external host when there are at least 64 bytes available to accept another message to be transmitted. When there are less than 64 bytes or the four message command locations are being used, the HDLC module will not issue any indication. In this case, the host has to wait until a new indication of FIFO availability is given.

17.4.1 Sending a Message

The host must first check that there is space available (at least 64 bytes). Once that is verified, the host can write the message and command the HDLC module to send it. The HDLC module indicates the availability of space by setting the “HALF” indicator bit.

There are two sections the host has to handle; the command register and the indicator and status register. The command register is used by the host to set “HALF” (64 bytes) or “EOM” commands. The indicator register is used by the host to check if there is space available and if the previous commands have been executed. Whenever a command is executed, an indication is given back to the host.

Figure 44. Sending a Message



17.4.2 Steps to Configure the HDLC Transmit Path

The configuration process is depicted in the following lines. It is assumed that all the modules have already being configured to the proper format and operating conditions. The following description applies only to HDLC specific functions.

a) Configuration of the HDLC module.

The selected module must be enabled before starting operations.

b) Configuration of time slots.

Assign the TS carrying data to be mapped to the selected HDLC. The TS can be configured to carry plain data (default), HDLC, or BERT data. Any number of TS of the same port can be assigned to the selected HDLC module. TS from different ports are not allowed to be mapped in the same HDLC module.

Note: HDLC data can be transmitted to the line or to the backplane side.

Define the mask to use in every selected TS. A mask can be used so that sub-rate streams can be supported. Any combination of bits is available. Once the mask is selected, it applies to all the TS in that port.

c) Optionally, enable the interrupt generation for events in the selected HDLC.

Enable the interrupt of the selected HDLC.

At this point the HDLC path is configured and messages can be transmitted.

Performance Monitoring 18

Performance monitoring is achieved by some modules storing anomalies, defect and failure data. An internal processor retrieving the data every second and building the related database. In the case of T1 streams, a On-Chip PRM must be generated every second, also a database is created that contains 15 minute bins. In the case of E1, accumulated results are maintained.

The performance elements will follow the T1.231 standard for T1, and the G.821/G.826 for E1.

Acronyms

AIS	Alarm Indication Signal.
BBER	Background Block Error Ratio.
CSS-P	One or more Controlled Slip (CS) events
CV-L	Code Violations on the line, BPV or EXZ
CV-P	Code Violation on the PATH. FE bit errors in SF or CRC errors in ESF
ES-L	Errored Seconds on the Line. One or more BPV or one or more EXZ or one or more LOS defects in a one second interval
ES-P	For ESF: A count of any: CRC errors, CS events, SEF defects, AIS defects, for SF: FE errors, CS events, SEF defects, AIS defects
ESR	Errored Seconds Ratio.
RAI	Remote Alarm Indication.
SAS-P	SEF/AIS seconds. One or more SEF or AIS defects
SES-L	Severely Errored Seconds on the Line. A one second interval with 1544 or more BPVs plus EXZ (CV-L) or one or more LOS defects.
SES-P	ESF: more than 320 CRC errors or, one or more SEF or AIS defects. SF: Eight or more FE events when Ft and Fs are measured or four FE events if only Ft is measured, or an SEF or AIS event.
SESR	Severely Errored Seconds Ratio.
UAS-P	Count of one second intervals for which the path is unavailable. Unavailable starts on the onset of 10 contiguous SESs. Those 10 SES must be included in the UAS count. Available starts on the onset of 10 contiguous seconds with no SES. Those 10 seconds are excluded from UAS.

18.1 T1 Performance Elements

In order to create the Performance Elements, the firmware needs to get some information regarding the status from the Near and Far ends.

18.1.1 T1 Near End

The performance elements for T1 Near End are:

CV-L, ES-L, SES-L, CV-P, ES-P, SES-P, SAS-P, UAS-P, CSS-P

They have to be stored in:

Current day	Current 24 Hours period
Previous day	Previous 24 Hours period
Current 15 min.	Current 15 minutes interval
Previous 15 min.	Previous 15 minutes interval
31 recent 15 min.	31 most recent intervals before the previous

The 24 hours period start at time 00:00 and keeps counting until 24 hours have elapsed. The current 24-hour data is then stored in the previous 24-hour data and the count is initialized again.

Table 35. Performance Elements T1

Current Day	32 bits
Previous Day	32 bits
Current 15 minutes	16 bits
Previous 15 minutes	16 bits
31 Recent 15 minutes	16 bits

18.1.2 T1 Far End

The performance elements for T1 Far End are:

ES-L, CV-P, ES-P, SES-P, UAS-P, CSS-P, ESA-P, ESB-P, SEFS-P

They have to be stored in:

Current day	Current 24 Hours period
Previous day	Previous 24 Hours period
Current 15 min.	Current 15 minutes interval
Previous 15 min.	Previous 15 minutes interval
31 recent 15 min.	31 most recent intervals before the previous

These elements are calculated based on the On-Chip PRM received.

Note: The bins will be updated with the internal one second signal, even if it is not synchronized with the On-Chip PRM received.

If there is no On-Chip PRM at the one second interval, update the far-end database with the values in ZERO.

18.2 E1 Performance Elements

This will follow the G.821/G.826 recommendations for E1. The counters keep the accumulated value, if maximum is reached, then the state remain on until it is cleared.

18.2.1 E1 Near End

ESR	Errored Seconds Ratio	32 bits
SESR	Severely Errored Seconds Ratio	32 bits
BBER	Background Block Error Ratio	32 bits

The ratio shall be represented in percent values multiplied by $1x10^{-6}$.

For example: 100000000 = 100%, 1000000 = 1%, 100000 = 0.1% and so on.

Additionally, the following variables have been stored to give the user a proper reference:

Time	Total time since the counter was last initialized	32 bits
UAS	Unavailable Seconds Time	32 bits
AvailR	Ratio of available time to unavailable time	32 bits
AvailT	Time since last getting into the available state	32 bits

The Time and AvailT granularity could be in seconds.

G.826 parameters can be evaluated during, or at the end of, a measurement period P as follows, taking into account Unavailable Seconds (UAS):

$BBER = cBBE/[(P - UAS - cSES) \times \text{blocks per second}]$

$ESR = cES/(P - UAS)$

$SESR = cSES/(P - UAS)$

18.2.2 E1 Far End

ESR	Errored Seconds Ratio	32 bits
SESR	SeveRely Errored Seconds Ratio	32 bits
BBER	Background Block Error Ratio	32 bits

The ratio shall be represented in percent values multiplied by $1x10^{-6}$.

For example: 100000000 = 100%, 1000000 = 1%, 100000 = 0.1% and so on.

Additionally, the following variables have been stored to give the user a proper reference:

Time	Total time since the counter was last initialized	32 bits
UAS	Unavailable Seconds Time	32 bits
AvailR	Ratio of available time to unavailable time	32 bits
AvailT	Time since last getting into the available state	32 bits

The Time and AvailT granularity could be in seconds.

G.826 parameters can be evaluated during, or at the end of, a measurement period P as follows, taking into account Unavailable Seconds (UAS):

BBER = cBBE/[(P - UAS - cSES) × blocks per second]

ESR = cES/(P - UAS)

SESR = cSES/(P - UAS)

18.3 Generic Elements

There are also some generic elements that apply to both modes (T1 and E1).

CRC, FE, LCV, OOF, CSR, CSL, COFA.

CRC: The number of CRC errors that occur in a one second interval.
FE: The number of F-Bit errors that occur in a one second interval.
LCV: The number of BPVs that occur in a one second interval.
OOF: Increments by one if OOF occurs during the one second interval.
CSR: Increments by one if CSRx occurs during the one second interval.
CST: Increments by one if CSTx occurs during the one second interval.
COFA: Increments by one if COFA occurs during the one second interval.

These elements should be 16 bits long. Note that they are updated every second.

18.4 Performance Elements Database

The database created to save the performance elements is accessible to the host. Near End and Far End parameters are stored.

There are specific memory locations to access the defined parameters. See the Memory Map Developer's Manual for the description of the registers.

18.5 Handling of On-Chip Performance Report Messages (On-Chip PRMs)

The system supports the automatic handling of the ANSI T1.403 On-Chip PRMs.

18.5.1 On-Chip PRM Reception

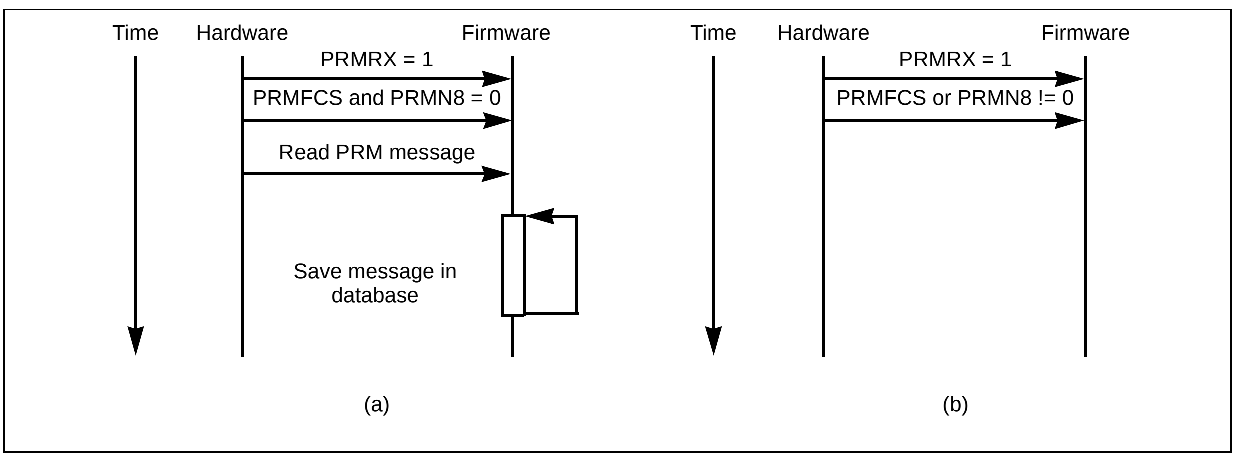
If the PRME bit is enabled, the firmware should continue with the next steps.

1. The firmware shall check for a On-Chip PRM every second. When the PRMRX bit is set in the PRMST register it indicates that there is a On-Chip PRM available.
2. If PRMFCS or PRMN8 is set in the PRMST register indicates that there is an error in the received message, skip the next steps.
3. The firmware reads the values received from the Far End and saves it in the database corresponding to the Far End.

Address 5A0Hex bit is used to enable the firmware to process PRM messages.

The Figure 45 shows the possible scenarios, assuming that the PRME bit has been set.

Figure 45. Rx On-Chip PRM Scenarios



18.5.2 On-Chip PRM Transmission

1. If the PRME bit is enabled, the firmware should continue with the next steps.

2. The firmware will build the new On-Chip PRM to be transmitted every second.
3. The firmware will write the new On-Chip PRM into the transmit On-Chip PRM bytes.
4. Write the TPRM bit to transmit the On-Chip PRM.

Host Interface 19

The host interface consists of a non-multiplexed 16 bit address bus and 8 bit data bus. It supports Intel I486 and Motorola MC68302 and MPC860 asynchronous modes. The pins INT_MOT and MOT_TYPE are used to select the bus type.

Table 36. Configuration Modes of the Host Interface

Mode	INT_MOT	MOT_TYPE
Intel i486	‘1’	‘0’
MPC860	‘0’	‘0’
MC68302	‘0’	‘1’

Table 37. Pin Names Relation Between IXF3208 and Target Processor

IXF3208 Pin name	MPC860 8 bits Pin name	MC68302 8 bits Pin name	I486 Pin name
CS_N	CSx	CSx	CSx
DS_N	OE	LDS	ADS
RW_N	R/W#	R/W#	W/R#
WE_N	WE0	-	CLK
RDY_N	TA#	DTACK#	RDY#
D0	D0	D0	D0
D1	D1	D1	D1
D2	D2	D2	D2
D3	D3	D3	D3
D4	D4	D4	D4
D5	D5	D5	D5
D6	D6	D6	D6
D7	D7	D7	D7
A0	A31	A0	BLE#
A1	A30	A1	A1
A2	A29	A2	A2
A3	A28	A3	A3
A4	A27	A4	A4
A5	A26	A5	A5
A6	A25	A6	A6
A7	A24	A7	A7
A8	A23	A8	A8
A9	A22	A9	A9

Table 37. Pin Names Relation Between IXF3208 and Target Processor

A10	A21	A10	A10
A11	A20	A11	A11
A12	A19	A12	A12
A13	A18	A13	A13
A14	A17	A14	A14
A15	A16	A15	A15

The interrupt pin provided is asserted low and it is asynchronous to the bus interface.

19.1 Access Window

The host interface is a non-multiplexed 16 bit address and 8 bit data bus. A “ready” signal is used to indicate when the transfer can be completed. Since access is to internal registers or RAM, the time taken to complete the transfer varies. The “ready” signal will insert wait states. In case there is no support for wait states by the external host, a mechanism based on an access window is provided that delivers a constant transfer time.

The registers WADDR, WDATA, WCMD and WSTS, at addresses 0004 to 0008 Hex, can be used to indicate the type of transfer, read or write. In a write operation, the host must set up the address in WADDR and the data in WDATA, and then write to WCMD a 00Hex to indicate the write operation. After that, polling the WSTS register for a 01Hex, indicating that the transfer is complete.

For a read operation, the host must set-up the address in WADDR, then write a 01Hex to WCMD to indicate a read operation. After that, polling the WSTS register for a 01Hex, indicating that the transfer is complete. It can then read the resulting data in the WDATA register.

JTAG Boundary Scan 20

20.1 Overview

The IXF3208 supports IEEE 1149.1 compliant JTAG boundary scan. Boundary scan allows easy access to the interface pins for board testing purposes.

20.2 Architecture

The IXF3208 JTAG architecture includes a Test Access Port (TAP) Controller, data registers, and an instruction register. The following paragraphs describe these blocks in detail.

20.3 Test Access Port (TAP) Controller

The TAP controller is a 16 state synchronous state machine controlled by the TMS input and clocked by TCK (see Figure 46). The TAP controls whether the IXF3208 is in reset mode, receiving an instruction, receiving data, transmitting data, or in an idle state. Table 38 describes in detail each of the states represented in Figure 46.

Figure 46. JTAG State Diagram

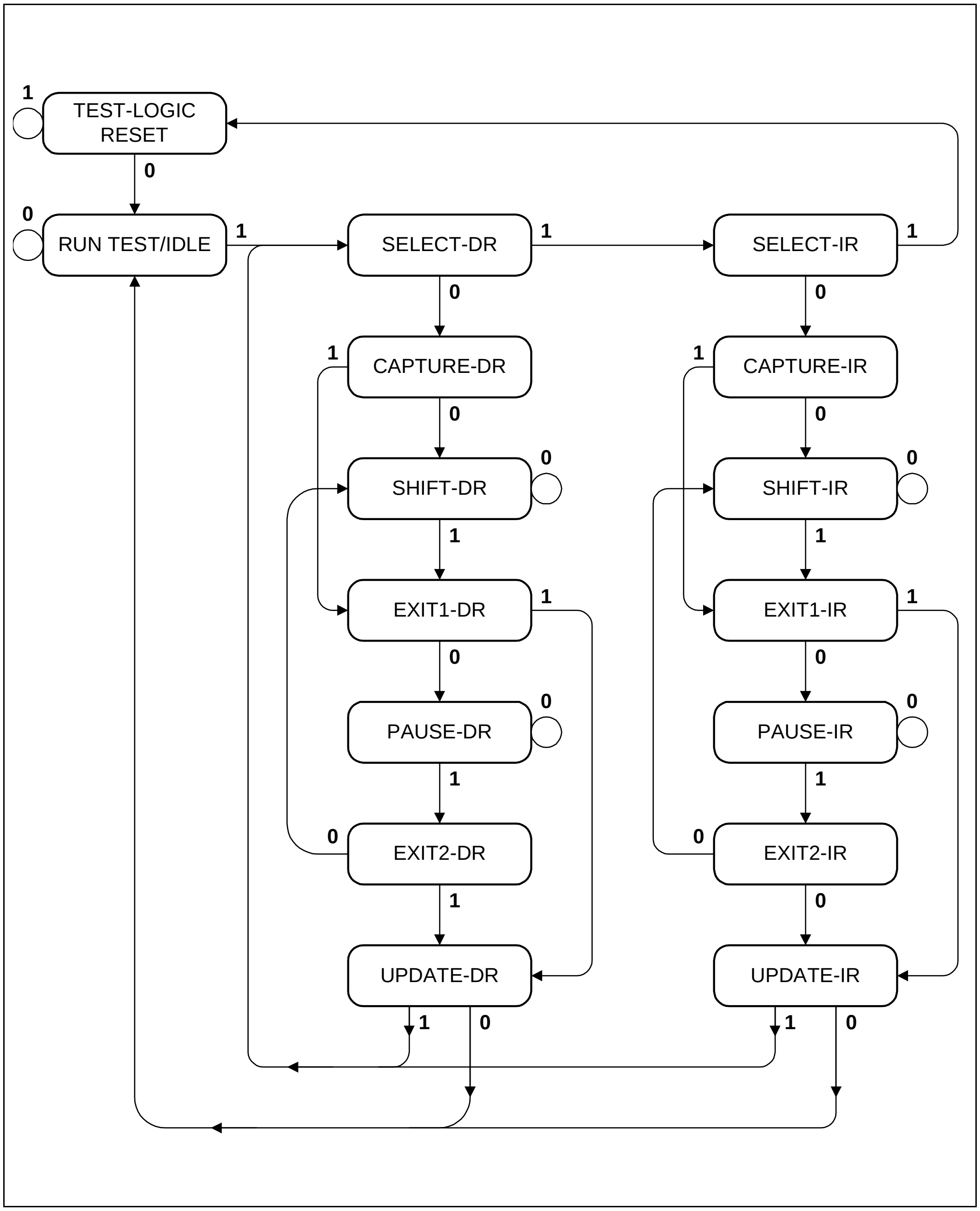


Table 38. TAP State Description

State	Description
Test Logic Reset	In this state, the test logic is disabled. The device is set to normal operation mode. While in this state, the instruction register is set to the ICODE instruction.
Run -Test / Idle	The TAP controller stays in this state as long as TMS is Low. Used to perform tests.
Capture - DR	The Boundary Scan Data Register (BSR) is loaded with the input pin data.
Shift - DR	Shifts the selected test data registers by one stage toward its serial output.
Update - DR	Data is latched into the parallel output of the BSR when selected.
Capture - IR	Used to load the instruction register with a fixed instruction.
Shift - IR	Shifts the instruction register by one stage.
Update - IR	Loads a new instruction into the instruction register.
Pause - IR Pause - DR	Momentarily pauses shifting of data through the data/instruction registers.
Exit1 - IR Exit1 - DR Exit2 - IR Exit2 - DR	Temporary states that can be used to terminate the scanning process.

20.4 JTAG Register Description

The following paragraphs describe each of the registers.

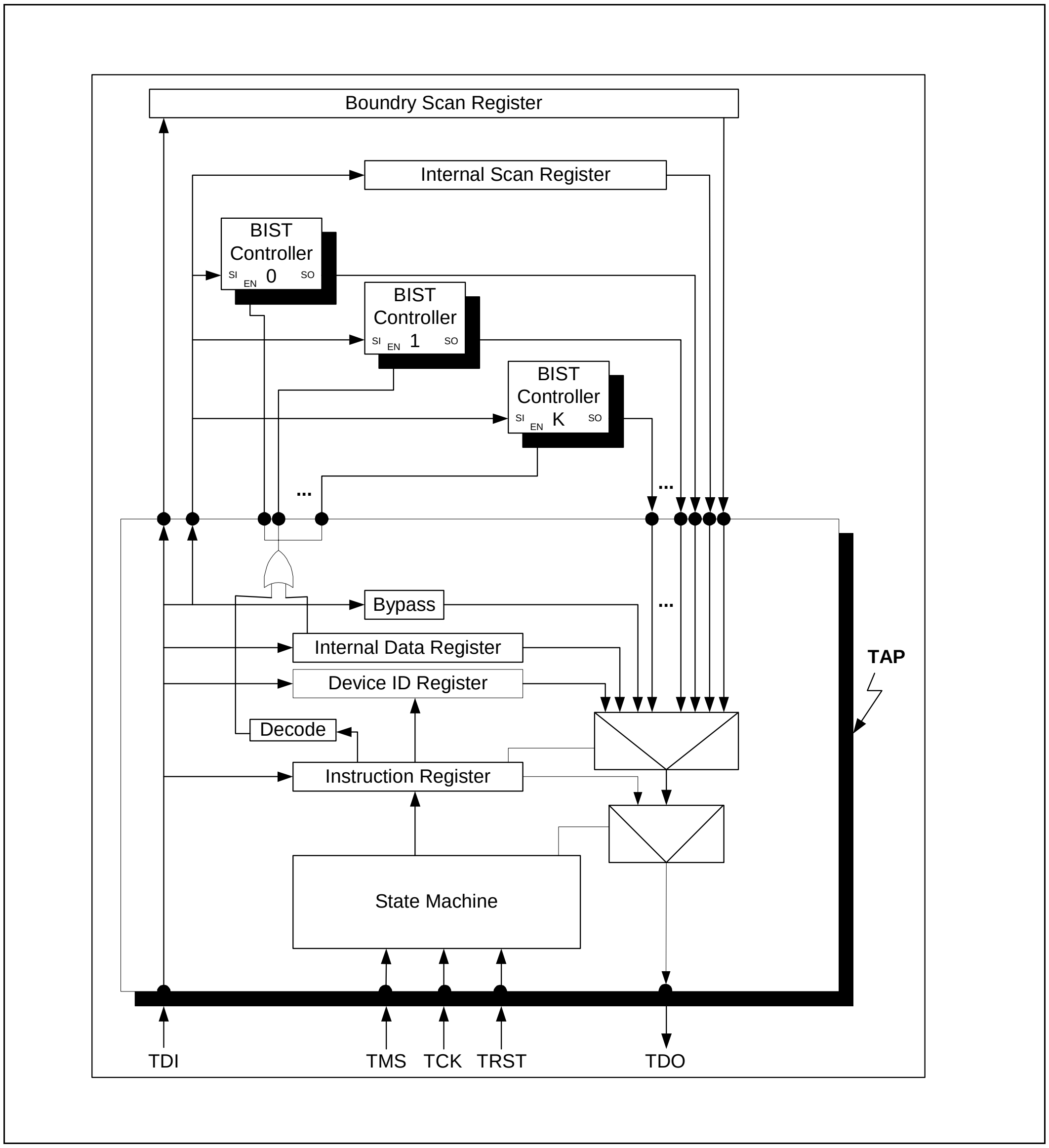
20.5 IEEE 1149.1 TAP Architecture

Figure 47 provides a high-level diagram of this TAP along with its interface to a number of BIST controllers. The TAP contains the following key blocks:

- State Machine
- Instruction register
- Internal data register
- Device ID register
- Bypass register
- Internal scan chain multiplexing logic

The TAP can individually access and enable up to 128 BIST controllers or embedded test functions. You can scan-initialize and enable these controllers or functions either individually or in parallel with one or more other BIST controllers or embedded test functions. The following sections of this chapter provide a detailed description of the TAP blocks, as well as a description of how the TAP controls and interfaces with the BIST controllers and the scan registers on the chip.

Figure 47. High Level Diagram of TAP Architecture



20.6 TAP Controller

The TAP controller contains a Finite State Machine (FSM) that manages access to all the instruction and data registers within the TAP and within the chip. This state machine cycles through the sixteen states illustrated in Figure 47, based on the value present on the *TMS* signal at each subsequent *TCK* clock cycle. Each of these states are described in following the illustration.

The values adjacent to each state transition correspond to the TMS signal. The signal TMS, sampled by the TAP controller on the rising edge of TCK, controls the state transitions.

20.6.1 Test-Logic-Reset

The *Test-Logic-Reset* controller state disables the test logic and resets the instruction TAP ports to *1101...*1, an instruction that selects the device ID register. If the device ID register is not present, *Test-Logic-Reset* selects the bypass register. When the TMS signal remains high for at least five rising edges of the TCK signal, the TAP controller transitions to the *Test-Logic-Reset* controller state.

20.6.2 Run-Test/Idle

The *Run-Test/Idle* controller state retains the last state of the test logic. During this state, the TAP controller can execute an internal test, such as BIST, previously selected by the instruction register.

20.6.3 Select-DR-Scan, Select-IR-Scan

The *Select-DR-Scan* and *Select-IR-Scan* are temporary controller states, which retain the last state of the test logic. During this state, if the *TMS* signal is low, the TAP controller initiates a scan sequence for either the selected test data register or the instruction register.

20.6.4 Capture-DR, Capture-IR

The *Capture-DR* and *Capture-IR* controller states parallel-load data into either a selected test data register or the instruction register on the rising edge of the *TCK* signal.

20.6.5 Shift-DR, Shift-IR

The *Shift-DR* and *Shift-IR* controller states shift either the selected test data register or the instruction register one stage towards its serial output.

20.6.6 Exit1-DR, Exit1-IR

The *Exit1-DR* and *Exit1-IR* are temporary controller states, during which all test data registers and the instruction register retain their previous state. During this state, if the *TMS* signal is high, the TAP controller terminates the scanning process. If the *TMS* signal is low, the TAP controller transitions the selected test data register or instruction register to the corresponding *Pause* controller state.

20.6.7 Pause-DR, Pause-IR

The *Pause-DR* and *Pause-IR* controller states temporarily halt the shifting of either the selected test data register or the instruction register. The TAP controller remains paused until the *TMS* signal goes high.

20.6.8 Exit2-DR, Exit2-IR

The *Exit2-DR* and *Exit2-IR* are temporary controller states, during which all test data registers and the instruction register retain their previous state. During this state, if the *TMS* signal is high, the TAP controller terminates the scanning process. If the *TMS* signal is low, the TAP controller returns either the selected test data register or the instruction register to the corresponding *Shift* controller state.

20.6.9 Update-DR, Update-IR

The *Update-DR* and *Update-IR* controller states transfer data from each shift-register stage into the corresponding parallel output latch on the falling edge of the *TCK* signal.

20.7 Test Data Registers

The test data registers are user-defined scan chains. The five types of test data registers are as follows:

- **Boundary-scan registe**r—an optional test data register used to test either logic inside of the IC or at the board-level interconnect.
- **Device ID registe**r—an optional test data register that provides a unique code to identify the device.
- **Bypass registe**r—a required test data register that is always included in LogicVision's TAP and that shifts data from the test data input port of the TAP to the test data output port of the TAP.
- **Internal scan register**s—optional test data registers that consist of user core logic scan chains and are used to perform scan and logic BIST testing.
- **Internal data registe**r—a LogicVision-specific, optional test data register that supplements the instruction register by providing additional BIST control and result gathering capabilities.

20.7.1 Device ID Register

The optional *device ID* test data register provides a unique code that identifies the device. The *device ID* register contains 32 parallel-in, serial-out shift-register stages that identify the version number, the part number, and the manufacturer of the device. Figure 48 illustrates the structure of the device ID code.

Figure 48. Structure of the Device ID Code

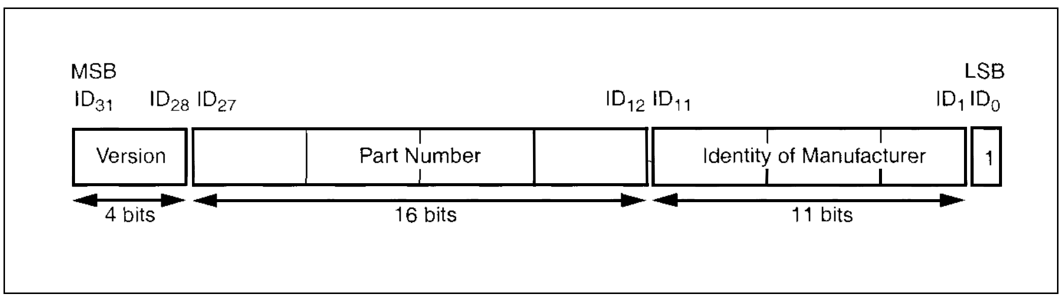


Table 39 describes how the TAP controller states affect the behavior of the device ID register.

Table 39. Behavior of the Device ID Register

During this TAP Controller State	The Device ID Register
Test-Logic-Reset	Retains the last state
Capture-DR	Loads the device ID code
Shift-DR	Shifts the ID towards the tdo TAP port
All other states	Retains the last state

When the *device ID* register is present in a design, the *Test-Logic-Reset* controller state automatically selects this register. If your design does not contain a *device ID* register, the TAP controller selects the *bypass* register. By examining the first bit that the TAP controller shifts out of the device, you can tell whether or not a *device ID* register is present. If the first bit is 0, the device does not include a *device ID* register and the TAP controller selected the *bypass* register instead.

20.7.2 Bypass Register

The required *bypass* test data register, consisting of a single shift-register stage, shifts information from the tdi port to the tdo TAP port without interfering with the normal operation of Framer.

Once selected, the *bypass* register loads a constant logic *0* into the shift-register stage on a rising edge of *TCK* during the *Capture-DR* controller state. Table 40 describes how the TAP controller states affect the shift-register stage.

Table 40. Behavior of the Bypass Register

During this TAP Controller State.	The Device ID Register.
Test-Logic-Reset	Retains the last state
Capture-DR	Loads the device ID code
Shift-DR	Shifts the ID towards the tdo TAP port
All other states	Retains the last state

The *bypass* register also provides a one-cycle delay between the tdi TAP port and the tdo TAP port. During a board-level test, the *bypass* register reduces the access time to the test data registers on Framer.

20.8 Ports for Required External Test Pins

IEEE 1149.1 requires five dedicated test pins, *TC*K, *TD*I, *TD*O, *TM*S, and TRST, to which the TAP signals *TC*K, *TD*I, *TD*O, *TM*S, and *TRST* connect. This subsection discusses the TAP ports that correspond to these TAP signals. The Assemble tool connects the *tc*k, *td*i, *td*o, *tm*s, and *trst* TAP ports to the respective test pins *TC*K, *TD*I, *TD*O, *TM*S, and *TRS*T.

20.8.1 TCK

The tck TAP controls the following actions:

- Sampling the *TDI* and *TMS* TAP signals
- Updating the *TDO* TAP signal

The TAP controller samples the *TDI* and *TMS* TAP signals on the rising edge of the *TCK* TAP signal and updates the *TDO* TAP signal on the falling edge of TCK. The test clock has the following properties:

- Single phase
- Free-running frequency range from 0 to 10 MHz (as hard coded in the BSDL file)

20.8.2 TDI TAP

The tdi TAP is the serial input for the instruction register and the test data registers. The TAP controller samples *tdi* on the rising edge of the *TCK* TAP signal.

20.8.3 TDO TAP

The tdo TAP is the serial output for the instruction register and the test data registers, and is at high-impedance except during shifting. The TAP controller updates *tdo* on the falling edge of the *TCK* TAP signal.

20.8.4 TDO Enable TAP

The tdo Enable TAP connects to the enable port of the *tdo* pad. This signal goes low one full clock cycle before valid data is output to the *td*o, and remains low until one clock cycle after the last bit is available on *td*o.

20.8.5 TMS TAP

The *tms* TAP controls the finite state machine (FSM). The TAP controller samples *tms* on the rising edge of the *TCK* TAP signal. For more information, refer to the “TAP Controller” section.

The trst TAP connects to the external pin TRST, an active-low, asynchronous reset for the TAP controller. When the *TRST* TAP signal is low, the TAP controller immediately enters the *Test-Logic-Reset* state.

20.9 Reserved Instructions

The IEEE 1149.1 specification includes a number of reserved instructions. Table 41 lists the bit assignments for the default 16-bit instruction register that corresponds to the reserved instructions. Set all extended instruction register bits to logic one for all instructions listed below, except for the *“0” EXTEST* instruction.

Table 41. IEEE 1149.1 Reserved Instructions

Instruction[15:0]	Reserved Instruction
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	BYPASS
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	EXTEST
1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 0 0	EXTEST
1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0	SAMPLE/PRELOAD

Table 41. IEEE 1149.1 Reserved Instructions

Instruction[15:0]	Reserved Instruction
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	IDCODE
1 1 1 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1	HIGHZ
1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1	CLAMP

20.9.1 Boundary Scan Register (BSR)

The BSR is a shift register that provides access to all the digital I/O pins. The BSR is used to apply and read test patterns to/from the device. Each pin is associated with a scan cell in the BSR register. Bidirectional pins or three statable pins require more than one position in the register. Table 42 shows the BSR scan cells and their functions. Data into the BSR is shifted in LSB first.

Table 42. Boundary Scan Register (BSR)

Bit #	Pin Name	Pin Number	I/O
236	EN1	-	-
235	tpos[7]	2	0(1)
234	tclk[7]	3	0(1)
233	rneg[6]	5	I(S}
232	rpos[6]	6	I(S)
231	rclk[6]	7	I{S)
230	tneg[6]	8	0{1)
229	tpes[6]	9	0(1)
228	tc!k[6]	10	0(1)
227	sysclk	13	I(S)
226	web	22	I(S)
225	csb	23	I(S)
224	metetype	25	I(S)
223	address[15]	27	I(S)
222	address[14]	28	I(S)
221	address[13]	29	I(S)
220	address[12]	30	I(S)
219	address[il]	3i	I(S)
218	address[10]	32	I(S)
217	address[9]	33	I(S)
216	address[8]	34	I{S)
215	address[7]	35	I(S}
214	address[6]	36	I{S)
213	address[5]	37	I(S)
212	address[4]	38	I(S)
211	address[3]	39	I(S)
210	address[2]	40	I(S)
209	address[l]	41	I(S)
208	address[O]	42	I(S)
207	EN2		
206	data[O]	46	IO(S,1)
205	data[l]	47	IO(S,1)

Table 42. Boundary Scan Register (BSR)

Bit #	Pin Name	Pin Number	I/O
204	data[2]	48	IO(S,1]
203	data[3]	49	IO(S,1)
202	data[4]	52	IO(S,1)
201	data[5]	53	IO(S,1)
200	data[6]	54	IO(S,1)
199	data[7]	55	IO(S,1)
198	tclk[1]	56	O{1)
197	tpos[1]	57	O(1)
196	Eneg[1]	58	O(1)
195	rcik[1]	59	I(S)
194	rpos[1]	60	I(S)
193	rneg[1]	61	I(S)
192	tclk[0]	63	0(1)
191	EN3		
190	tpos[0]	65	O(1)
189	tneg[0]	66	0{1)
188	rclk[0]	67	I(S)
187	rpos[0]	68	I{S)
186	rneg[0]	69	I{S)
185	refclk	75	0(1)
184	elx24	76	I(S)
183	ulx24	77	I{S)
182	resetb	80	I
181	arctmsb	81	I{S)
180	arctde	82	O{1)
179	scanen	85	I(S)
178	testenb	86	I(S}
177	tristb	87	I
176	tdrin	89	I(S}
175	tdreut	90	0(1}
174	quad	105	I(S)
173	btsig[T]	107	I(S)
172	btmfp[7]	108	I(S}
171	EN4		
170	btfp[7]	109	IO(S,1)
169	btdata[71]	110	I(S)
168	EN5		
167	btclk[7]	111	IO(S,1)

Table 42. Boundary Scan Register (BSR)

Bit #	Pin Name	Pin Number	I/O
166	EN6		
165	brsig[7]	112	0(1)
164	EN7		
163	brm~p[7]	113	0(1)
162	EN8		
16l	brfp[7]	114	IO(S,1)
160	EN9		
159	brdata[7]	115	0(1)
158	EN10		
157	brclk[7]	116	IO(S,1)
156	rneg[3]	121	I(S)
155	rpos[3]	122	I{S)
154	rclk[3]	123	I{S)
153	tneg[3]	124	0(1)
152	tpos[3]	125	0(1)
151	tclk[3]	126	0(1}
150	rneg[2]	129	I(S)
149	rpos[21	130	I(S}
148	rclk[2]	131	I(S)
147	ENll		
146	tneg[2]	132	0(1)
145	tpos[2]	133	0(1)
144	tclk[2]	134	0(1)
143	ENI2		
142	intb	135	0(1)
141	EN13		
140	rdyb	136	0(1)
139	dsb	137	I(S)
138	rwb	138	I(S)
137	intelmet	139	I(S)
136	btsig[6]	143	I(S)
135	btmfp[6]	144	I(S)
134	EN14		
133	btfp[6]	145	IO(S,1)
132	btdata[6]	146	I(S)
131	EN15		
130	btclk[6]	147	IO(S,1)
129	EN16		

Table 42. Boundary Scan Register (BSR)

Bit #	Pin Name	Pin Number	I/O
128	brsig[6]	148	0(1)
127	EN17		
126	brmfp[6]	149	0(1}
125	EN18		
124	brfp[6]	i50	IO(S,1)
123	ENi9		
122	brdata[6]	151	O(1)
121	EN20		
120	brclk[6]	152	IO(S,1)
119	btsig[5]	155	I(S)
118	btmfp[5]	156	I{S)
11'7	EN21		
116	btfp[5]	157	IO(S,1)
115	bidara[5]	158	I(S)
114	EN22		
113	btclk[5]	159	IO(S,1
112	EN23		
111	brsig[5]	160	O(1)
110	EN24		
109	brmfp[5]	161	0(1}
108	EN25		
107	brfp[5]	162	IO(S,1)
106	EN26		
105	brdata[5]	163	O(1)
104	EN27		
103	brclk[5]	164	IO(S,1)
102	btsig[4]	166	I{S)
101	btmfp[4]	167	I(S)
100	EN28		
99	btfp[4]	168	IO(S,1)
98	btdata[4]	169	I(S)
97	EN29		
96	btclk[4]	170	IO(S,1}
95	EN30		
94	brsig[4]	171	O(1)
93	EN31		
92	hrmfp[4]	172	O(1)
91	EN32		

Table 42. Boundary Scan Register (BSR)

Bit #	Pin Name	Pin Number	I/O
90	hrfp[4]	173	IO(S,1)
89	EN33		
88	brdata[4]	174	O{1)
87	EN34		
86	brclk[4]	175	IO(S,1)
85	tclk[53	185	O(1)
84	tpos[5]	186	0(1)
83	tneg[5]	187	O(1)
82	rclk[5]	188	I(S)
81	rpes[5]	189	I(S)
80	rneg[5]	190	I(S)
79	tclk[4]	192	0{1)
78	EN35		
77	~pos[4]	193	O~i}
76	tneg[4]	194	0(1)
75	rclk[4]	195	I(S)
74	rpes[4]	196	I(S}
73	rneg[4]	197	I(S}
74	rpes[4]	196	I(S}
73	rneg[4]	197	I(S}
72	btsig[3]	202	I{S
71	btmfp[3]	203	I(S)
70	EN36		
69	btfp[3]	204	IO(S,1)
68	btdata[3]	205	I(S}
67	EN37		
66	btclk[3]	206	IO(S,1)
65	EN38		
64	brsig[3]	207	O(1)
63	EN39		
62	brmfp[3]	208	O(1)
61	EN40		
60	brfp[3]	209	IO(S,1)
59	EN41		
58	brdata[3]	210	O(1)
57	EN42		
56	brclk[3]	211	IO(S,1)
55	btsig[2]	216	I(S)

Table 42. Boundary Scan Register (BSR)

Bit #	Pin Name	Pin Number	I/O
54	btmfp[2]	217	I(S)
53	EN43		
52	btfp[2]	218	IO(S,1)
51	btdata[2]	2]9	I(S)
50	EN44		
49	btclk[2]	220	IO(S,1)
48	EN45		
47	brsig[2]	221	0(1)
46	EN46		
45	brmfp{2]	222	0(1)
44	EN47		
43	brfp[2]	223	IO(S,1)
42	EN48		
41	brdata[2]	224	O(1)
40	EN49		
39	brclk[2]	225	IO(S,1)
38	btsig[1]	227	I(S)
37	btmfp[1]	228	I(S)
36	EN50		
35	btfp[1]	229	IO(S,1)
34	btdata[1]	230	I(S)
33	EN51		
32	btclk[1]	231	IO(S,1
31	EN52		
30	brsig[1]	232	O(1)
29	EN53		
28	brmfp[1]	233	O(1)
27	EN54		
26	brfp[1]	234	IO(S,1
25	EN55		
24	brdata[1]	235	0(1)
23	EN56		
22	brclk[1]	236	IO(S,1
21	btsig[0]	239	I(S)
20	btmfp[0]	240	I(S)
19	EN57		
18	btfp[0]	241	IO(S,1)
17	btdata[©]	242	I(S)

Table 42. Boundary Scan Register (BSR)

Bit #	Pin Name	Pin Number	I/O
16	EN58		
15	btclk[0]	243	IO(S,1)
14	EN59		
13	brsig[0]	244	0(1)
12	EN60		
11	brmfp[0]	245	0(1)
10	EN61		
9	Drfp[0]	246	IO(S,1)
8	EN62		
7	brdata[0]	247	O(1)
6	EN63		
5	brclk{0]	248	IO(S,1)
4	meg [7]	253	I(S)
3	rpos [7]	254	I(S)
2	rclk[7]	255	I(S)
1	tneg[7]	256	0(1)

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Note: The minimum and maximum values in Tables 44 to 45 represent the performance specifications of the IXF3208 and are guaranteed by test, except where noted by design.

Table 43. Absolute Maximum Ratings

Parameter	Sym	Min	Max	Unit
DC supply Core (reference to GND)[1]	Vcc	-0.5	TBD	V
DC supply I/O (reference to GND)[1]	VCCIO	-0.5	TBD	V
Input voltage, any digital pin	VIN	GND -0.5	VccIO +0.5	V
Input current, any pin	IIN	-10	+10	mA
Storage temperature	TSTG	-65	+150	°C
Thermal Resistance, junction to ambient, PBGA[4]	θJA	30C/W	38C/W	°C/W
ESD voltage, any pin[2,3]	VIN	----	2,000	V
Caution: Operation at these limits may permanently damage the device. Normal operation at these extremes not guaranteed. 1. TGND and GND must not differ by more than 0.3 V during operation. 2. Human body model. 3. This is a design target and not a product specification. 4. Jedac Standard 2S2P Board.				

Table 44. Operating Conditions

Parameter	Sym	Min	Typical	Max	Unit
DC supply Core (reference to GND)	V_{CC}	1.62	1.8	1.98	V
DC supply I/O (reference to GND)	V_{CCIO}	2.97	3.3	3.63	V
Input voltage, any pin	V_{IN}	GND -0.3 V	–	VCC +0.3 V	V
Storage Temperature	T_{STG}	-65	–	150	° C
Operating Current (Core)	ICC_{CORE}	–	118	150	mA
Operating Current (I/O)	ICC_{IO}	–	76	100	mA
Operating Temperature	T_{OPA}	-40	+25	+85	° C
Caution: Operation at these limits may permanently damage the device. Normal operation at these extremes is not guaranteed.					

Table 45. DC Characteristics

Parameter	Sym	Min	Max	Unit	Test Conditions
High Level Input Voltage	V_{IH}	2.0	$V_{CC}IO$	V	
Low Level Input Voltage	V_{IL}	0	0.8	V	
High level output voltage	V_{OH}	2.4	–	V	-2.0 mA
Low level output voltage	V_{OL}	–	0.4	V	2.0 mA
Input leakage current	I_{LL}	-1.0	1.0	µA	
Input pull up current - RESETB TRISTB, TMS, TDI, TRSTB	I_{LL}	-15	-26	µA	
Input pull up current - TCK	I_{LL}	-78	-130	µA	
Three-state leakage current (all outputs)	I_{3L}	-1.0	1.0	µA	

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22.1 Receive Timing Diagrams

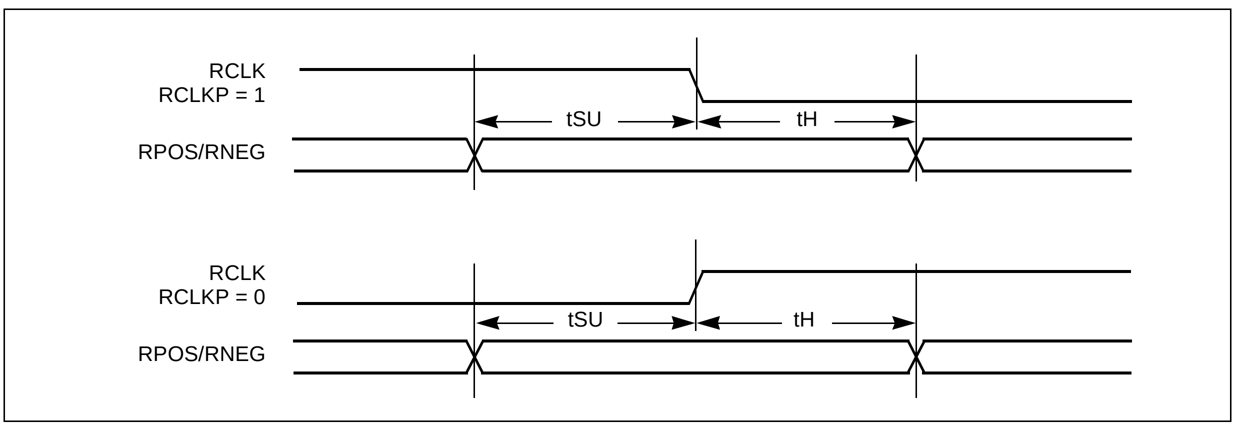
Table 46. Receive Timing Characteristics for T1 Operation

Parameter	Symbol	Min	Typ	Max	Unit
T1 Receive clock frequency	RCLK	-	1.544	-	MHz
T1 Receive clock duty cycle	RCLKd	40	50	60	%
RPOS/RNEG to RCLK setup time	t_{SU}	4	-	-	ns
RCLK to RPOS/RNEG hold time	t_H	8	-	-	ns
NOTE: 1. Typical figures are for design aid only, not guaranteed and not subject to production testing.					

Table 47. Receive Timing Characteristics for E1 Operation

Parameter	Symbol	Min	Typ	Max	Unit
E1 Receive clock frequency	RCLK	-	2.048	-	MHz
E1 Receive clock duty cycle	RCLKd	40	50	60	%
RPOS/RNEG to RCLK setup time	t_{SU}	4	-	-	ns
RCLK to RPOS/RNEG hold time	t_H	8	-	-	ns
NOTE: 1. Typical figures are for design aid only, not guaranteed and not subject to production testing.					

Figure 49. Receive Clock Timing Diagram



22.2 Transmit Timing Diagrams

Table 48. Transmit Timing Characteristics for T1 Operation

Parameter	Symbol	Min	Typ	Max	Unit
T1 Transmit clock duty cycle	TCLKd	40	50	60	%
T1 Transmit clock period	t_{PW}	-	648	-	ns
T1 Transmit clock pulse width High	t_{PWH}	260	324	388	ns
T1 Transmit clock pulse width Low	t_{PWL}	260	324	388	ns
TCLK to TPOS/TNEG delay	t_D	3	-	9	ns

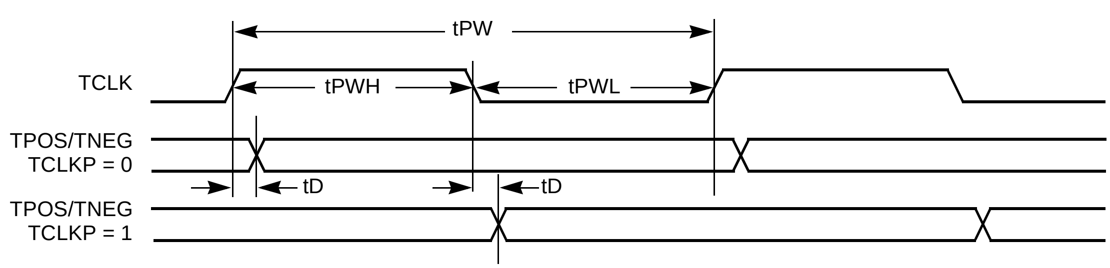
NOTE:
1. Typical figures are for design aid only, not guaranteed and not subject to production testing.
2. TCLK duty cycle widths will vary according to extent of received pulse jitter displacement. Max and Min TCLK duty cycles are for worst case jitter conditions.
3. Worst case conditions guaranteed by design only.

Table 49. Transmit Timing Characteristics for E1 Operation

Parameter	Symbol	Min	Typ	Max	Unit
E1 Transmit clock duty cycle	TCLKd	40	50	60	%
E1 Transmit clock period	t_{PW}	-	488	-	ns
E1 Transmit clock pulse width High	t_{PWH}	195	244	293	ns
E1 Transmit clock pulse width Low	t_{PWL}	195	244	293	ns
TCLK to TPOS/TNEG delay	t_D	3	-	9	ns

NOTE:
1. Typical figures are for design aid only, not guaranteed and not subject to production testing.
2. TCLK duty cycle widths will vary according to extent of received pulse jitter displacement. Max and Min TCLK duty cycles are for worst case jitter conditions.
3. Worst case conditions guaranteed by design only.

Figure 50. Transmit Clock Timing Diagram



System Interface Timing 23

23.1 Receive Timing Diagrams

Table 50. Receive Timing Characteristics for T1 Operation

Parameter	Symbol	Min	Typ	Max	Unit
T1 Receive clock frequency (when BRCLK is an input)	BRCLK	1.544	1.544	12.352	MHz
T1 Receive clock duty cycle	BRCLKd	40	50	60	%
T1 Receive clock period (when BRCLK is an output)	t_{PW}	-	648	-	ns
T1 Receive clock pulse width High (when BRCLK is an output)	t_{PWH}	260	324	388	ns
T1 Receive clock pulse width Low (when BRCLK is an output)	t_{PWL}	260	324	388	ns
BRFP to BRCLK setup time (when BRFP is an input)	t_{SU}	10	-	-	ns
BRCLK to BRFP hold time (when BRFP is an input)	t_{H}	3	-	-	ns
BRCLK to BRFP delay (when BRFP is an output)	t_{D}	0	-	15	ns
BRCLK to BRMFP delay	t_{D}	0	-	22	ns
BRCLK to BRDATA delay	t_{D}	0	-	15	ns
BRCLK to BRSIG delay	t_{D}	0	-	21	ns

NOTE:
1. Typical figures are for design aid only, not guaranteed and not subject to production testing.

Table 51. Receive Timing Characteristics for E1 Operation

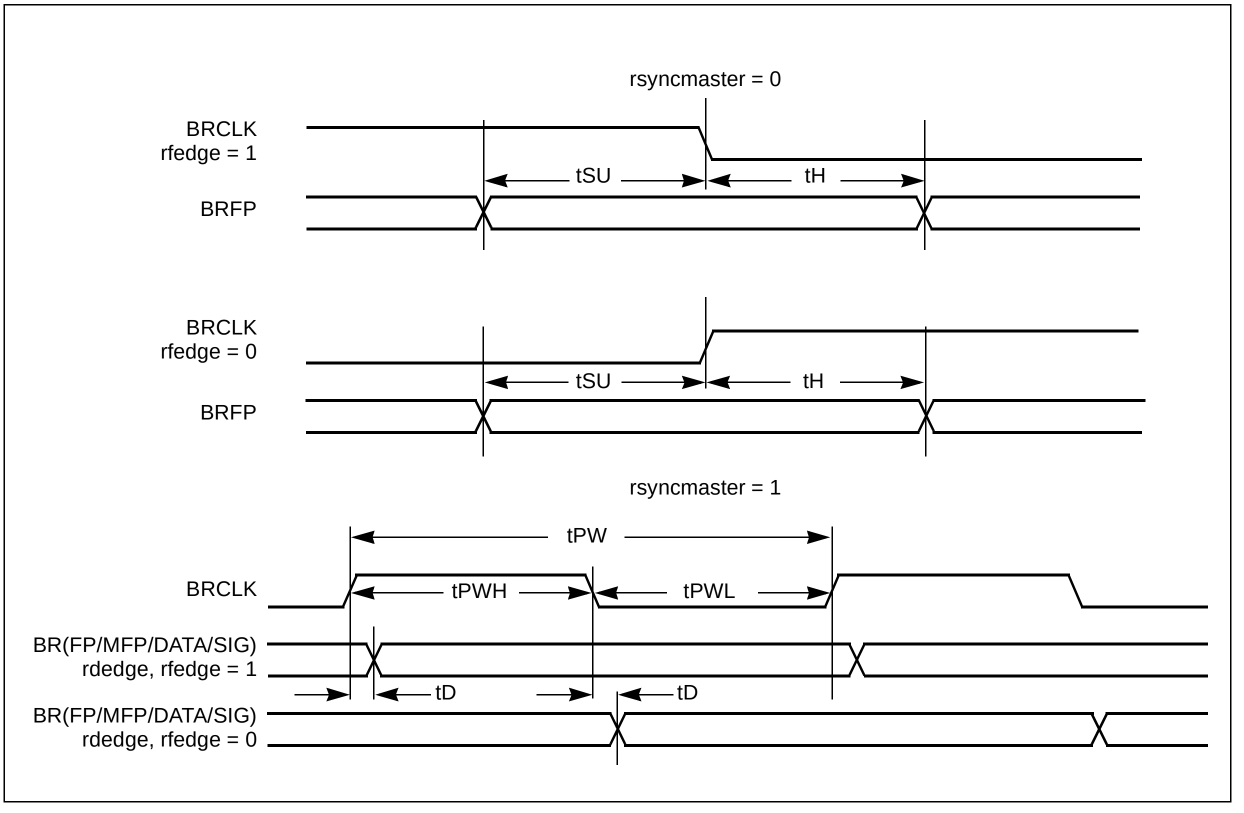
Parameter	Symbol	Min	Typ	Max	Unit
E1 Receive clock frequency (when BRCLK is an input)	BRCLK	2.048	2.048	16.384	MHz
E1 Receive clock duty cycle	BRCLKd	40	50	60	%
E1 Receive clock period (when BRCLK is an output)	t_{PW}	-	488	-	ns
E1 Receive clock pulse width High (when BRCLK is an output)	t_{PWH}	195	244	293	ns
E1 Receive clock out pulse width Low (when BRCLK is an output)	t_{PWL}	195	244	293	ns
BRFP to BRCLK setup time (when BRFP is an input)	t_{SU}	10	-	-	ns
BRCLK to BRFP hold time (when BRFP is an input)	t_{H}	3	-	-	ns
BRCLK to BRFP delay (when BRFP is an output)	t_{D}	0	-	15	ns
BRCLK to BRMFP delay	t_{D}	0	-	22	ns

Table 51. Receive Timing Characteristics for E1 Operation

Parameter	Symbol	Min	Typ	Max	Unit
BRCLK to BRDATA delay	t_D	0	-	15	ns
BRCLK to BRSIG delay	t_D	0	-	21	ns

NOTE:
1. Typical figures are for design aid only, not guaranteed and not subject to production testing.

Figure 51. Receive Clock Timing Diagram



23.2 Transmit Timing Diagrams

Table 52. Transmit Timing Characteristics for T1 Operation

Parameter	Symbol	Min	Typ	Max	Unit
T1 Receive clock frequency (when BTCLK is an input)	BTCLK	1.544	1.544	12.352	MHz
T1 Receive clock duty cycle	BTCLKd	40	50	60	%
T1 Receive clock period (when BTCLK is an output)	t_{PW}	-	648	-	ns
T1 Receive clock pulse width High (when BTCLK is an output)	t_{PWH}	260	324	388	ns
T1 Receive clock pulse width Low (when BTCLK is an output)	t_{PWL}	260	324	388	ns
BTFP to BTCLK setup time (when BTFP is an input)	t_{SU}	11	-	-	ns
BTCLK to BTFP hold time (when BTFP is an input)	t_H	4	-	-	ns
BTCLK to BTFP delay (when BTFP is an output)	t_D	0	-	15	ns
BTMFP to BTCLK setup time	t_{SU}	11	-	-	ns
BTCLK to BTMFP hold time	t_H	4	-	-	ns
BTDATA to BTCLK setup time	t_{SU}	12	-	-	ns
BTCLK to BTDATA hold time	t_H	4	-	-	ns
BTSIG to BTCLK setup time	t_{SU}	12	-	-	ns
BTCLK to BTSIG hold time	t_H	4	-	-	ns

NOTE:
1. Typical figures are for design aid only, not guaranteed and not subject to production testing.

Table 53. Transmit Timing Characteristics for E1 Operation

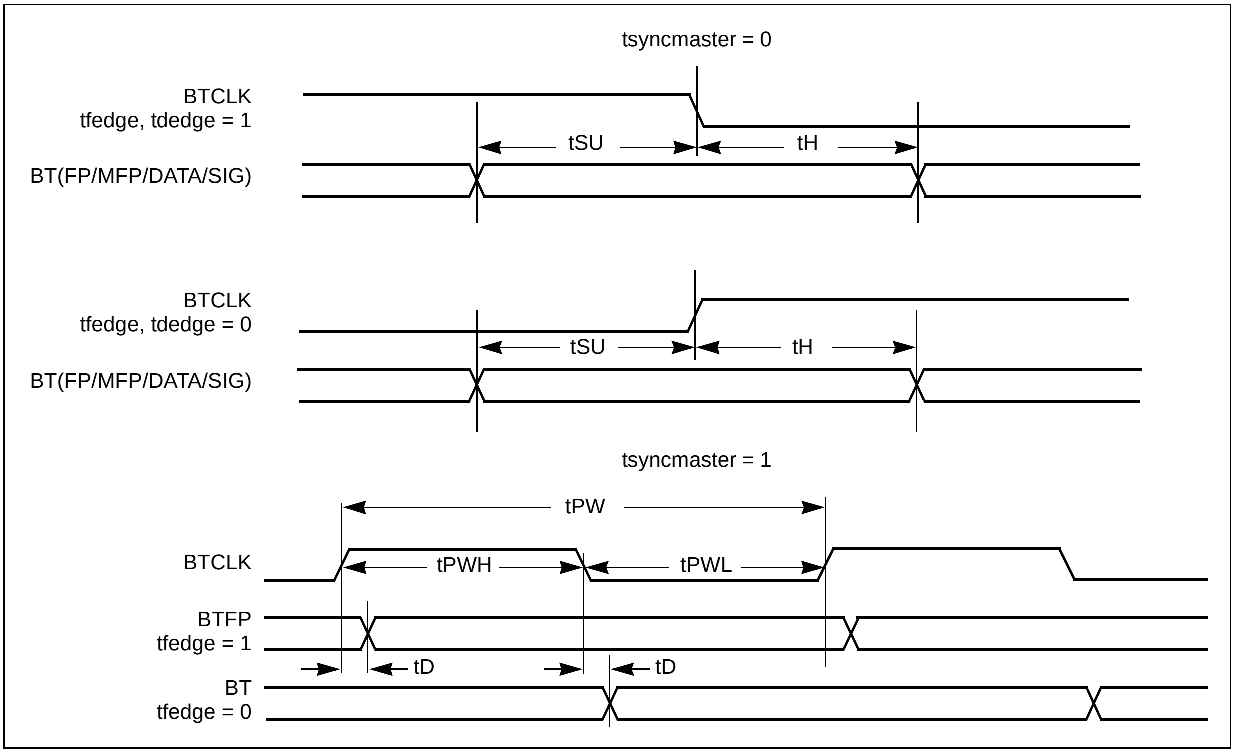
Parameter	Symbol	Min	Typ	Max	Unit
E1 Receive clock frequency (when BTCLK is an input)	BTCLK	2.048	2.048	16.384	MHz
E1 Receive clock duty cycle	BTCLKd	40	50	60	%
E1 Receive clock period (when BTCLK is an output)	t_{PW}	-	488	-	ns
E1 Receive clock pulse width High (when BTCLK is an output)	t_{PWH}	195	244	293	ns
E1 Receive clock out pulse width Low (when BTCLK is an output)	t_{PWL}	195	244	293	ns
BTFP to BTCLK setup time	t_{SU}	11	-	-	ns
BTCLK to BTFP hold time	t_H	4	-	-	ns
BTCLK to BTFP delay	t_D	0	-	15	ns
BTMFP to BTCLK setup time	t_{SU}	11	-	-	ns
BTCLK to BTMFP hold time	t_H	4	-	-	ns
BTDATA to BTCLK setup time	t_{SU}	12	-	-	ns
BTCLK to BTDATA hold time	t_H	4	-	-	ns

Table 53. Transmit Timing Characteristics for E1 Operation

Parameter	Symbol	Min	Typ	Max	Unit
BTSIG to BTCLK setup time	t_{SU}	12	-	-	ns
BTCLK to BTSIG hold time	t_H	4	-	-	ns

NOTE:
1. Typical figures are for design aid only, not guaranteed and not subject to production testing.

Figure 52. Transmit Clock Timing Diagram



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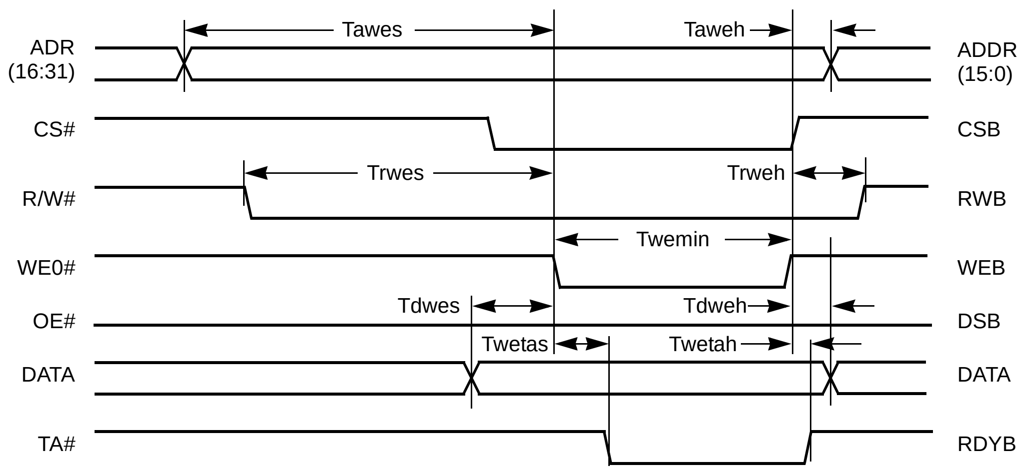
24.1 Timing Diagrams

Figure 53. MPC860 Write Timing



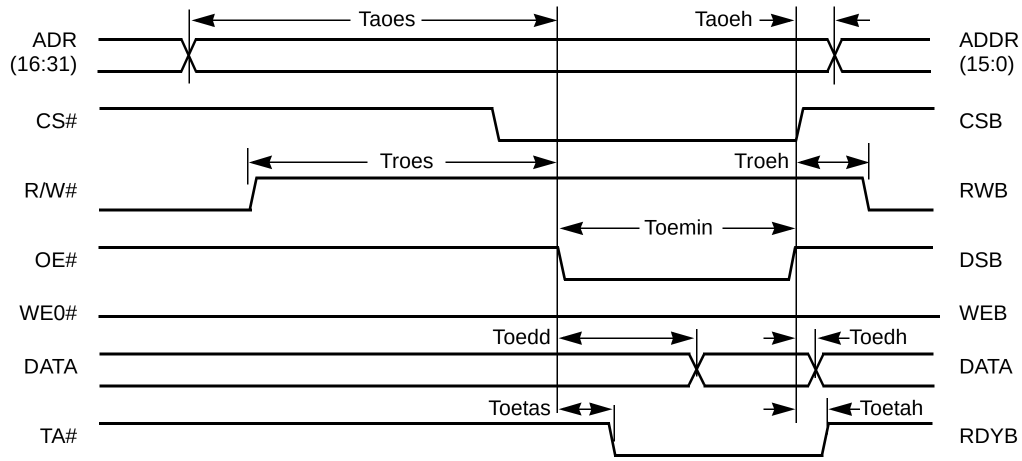
Note: WE timing restrictions apply to CS.

Table 54. MPC860 Write Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Address setup to WE	Tawes	1	-	-	ns
Address hold from WE	Taweh	2	-	-	ns
R/W# setup to WE	Trwes	1	-	-	ns
R/W# hold from WE	Trweh	2	-	-	ns
Data setup to WE	Tdwes	1	-	-	ns
Data hold from WE	Tdweh	2	-	-	ns
WE minimum width	Twemin	90	-	-	ns
WE low to TA asserted	Twetas	90	-	390	ns
WE high to TA inactive	Twetah	9	-	30	ns

NOTE:
1. Typical figures are for design aid only, not guaranteed and not subject to production testing.

Figure 54. MPC860 Read Timing

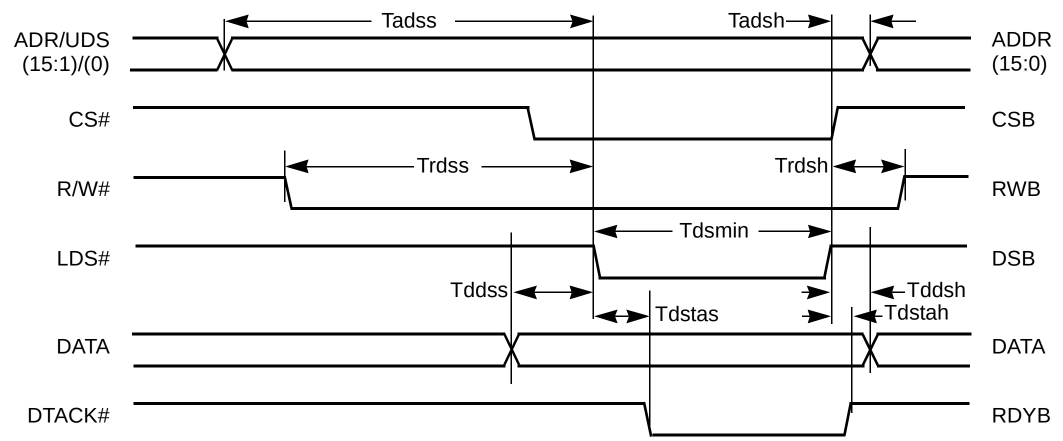


Note: WE timing restrictions apply to CS.

Table 55. MPC860 Read Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Address setup to OE	Taoes	1	-	-	ns
Address hold from OE	Taoeh	2	-	-	ns
R/W# setup to OE	Troes	1	-	-	ns
R/W# hold from OE	Troeh	2	-	-	ns
OE asserted to data valid	Toedd	91	-	-	ns
OE high to data invalid	Toedh	1	-	-	ns
OE minimum width	Toemin	91	-	-	ns
OE low to TA asserted	Toetas	90	-	390	ns
OE high to TA inactive	Toetah	10	-	25	ns
NOTE: 1. Typical figures are for design aid only, not guaranteed and not subject to production testing.					

Figure 55. M68302 Write Timing



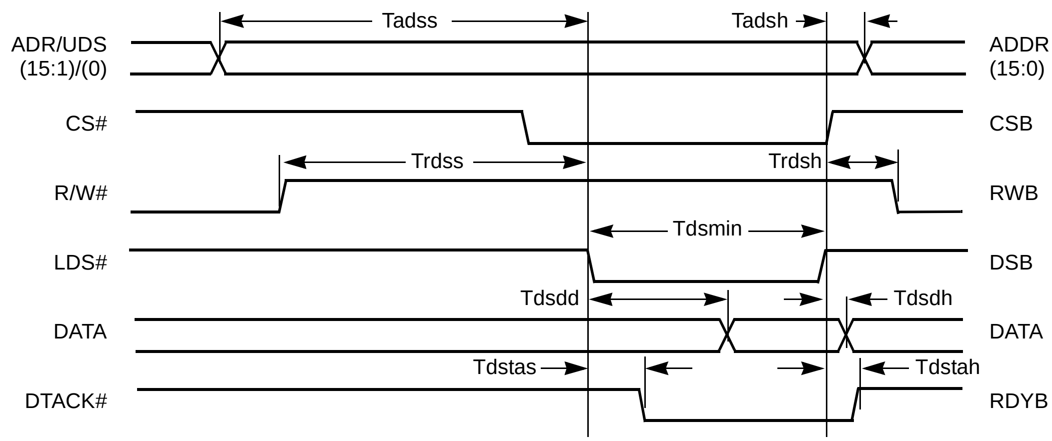
Note: LDS timing restrictions apply to CS.

Table 56. M68302 Write Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Address setup to LDS	Tadss	1	-	-	ns
Address hold from LDS	Tadsh	2	-	-	ns
R/W# setup to LDS	Trdss	1	-	-	ns
R/W# hold from LDS	Trdsh	2	-	-	ns
Data setup to LDS	Tddss	1	-	-	ns
Data hold from LDS	Tddsh	2	-	-	ns
LDS minimum width	Tdsmin	91	-	-	ns
LDS low to TA valid	Tdstas	90	-	380	ns
LDS high to TA invalid	Tdstah	9	-	30	ns

NOTE:
1. Typical figures are for design aid only, not guaranteed and not subject to production testing.

Figure 56. M68302 Read Timing



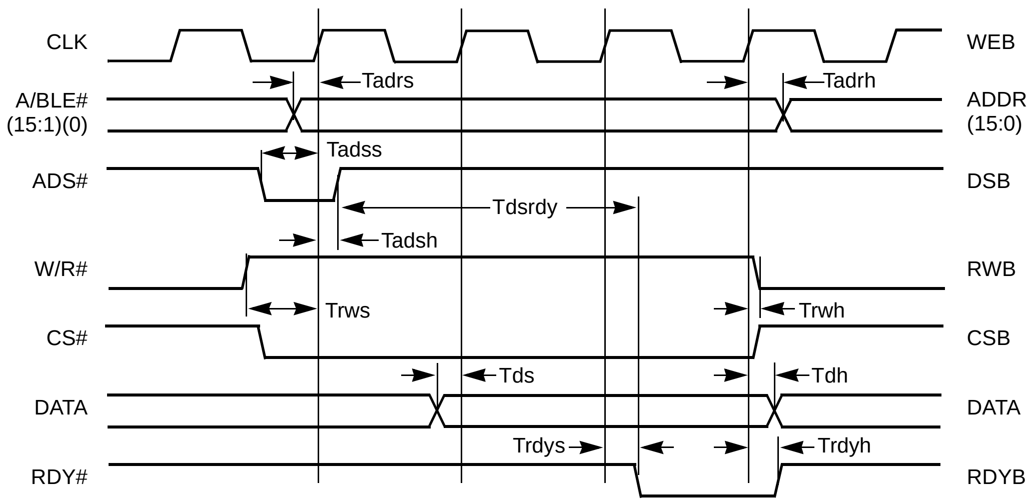
Note: LDS timing restrictions apply to CS.

Table 57. M68302 Read Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Address setup to LDS	Tadss	1	-	-	ns
Address hold from LDS	Tadsh	2	-	-	ns
R/W# setup to LDS	Trdss	1	-	-	ns
R/W# hold from LDS	Trdsh	2	-	-	ns
LDS low to data valid	Tdsdd	91	-	-	ns
Data hold from LDS high	Tdsdh	10	-	-	ns
LDS minimum width	Tdsmin	91	-	-	ns
LDS low to TA valid	Tdstas	90	-	390	ns
LDS high to TA invalid	Tdstah	10	-	25	ns

NOTE:
1. Typical figures are for design aid only, not guaranteed and not subject to production testing.

Figure 57. i486 Write Timing



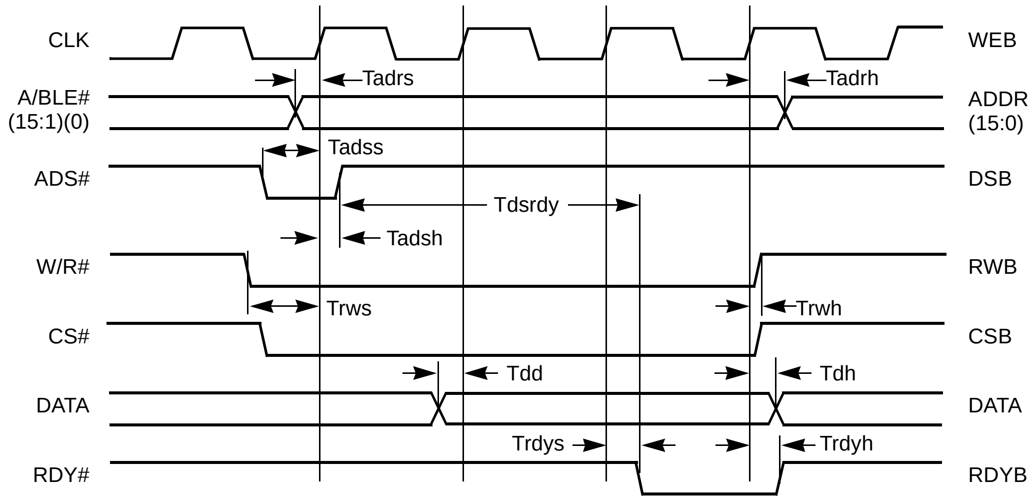
Note: W/R# timing restrictions apply to CS.

Table 58. i486 Write Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
ADS high to RDY# asserted	Tdsrdy	90	-	380	ns
Address setup time	Tadrs	1	-	-	ns
Address hold time	Tadrh	2	-	-	ns
ADS setup time	Tadss	1	-	-	ns
ADS hold time	Tadsh	2	-	-	ns
W/R# setup time	Trws	1	-	-	ns
W/R# hold time	Trwh	2	-	-	ns
Data setup time	Tds	1	-	-	ns
Data hold time	Tdh	2	-	-	ns
CLK to RDY# low	Trdys	5	-	11	ns
CLK to RDY# high	Trdyh	5	-	15	ns

NOTE:
1. Typical figures are for design aid only, not guaranteed and not subject to production testing.

Figure 58. i486 Read Timing



Note: W/R# timing restrictions apply to CS.

Table 59. i486 Read Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
ADS high to RDY# asserted	Tdsrdy	90	-	380	ns
Address setup time	Tadrs	1	-	-	ns
Address hold time	Tadrh	2	-	-	ns
ADS setup time	Tadss	1	-	-	ns
ADS hold time	Tadsh	2	-	-	ns
W/R# setup time	Trws	1	-	-	ns
W/R# hold time	Trwh	2	-	-	ns
CLK to data valid	Tdd	1	-	-	ns
Data hold from CLK	Tdh	2	-	-	ns
CLK to RDY# low	Trdys	5	-	11	ns
CLK to RDY# high	Trdyh	5	-	15	ns

NOTE:
1. Typical figures are for design aid only, not guaranteed and not subject to production testing.

Figure 59. IXF3208 256 Plastic Ball Grid Array (PBGA) Assignment

Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	TPOS7	RNEG7	BRFP0	BT CLK0	BT DATA0	BR DATA1	BT DATA1	BR DATA2	BT DATA2	VSS	BR MFP3	BT DATA3	RPOS4	RCLK4	TPOS4	ALOS5
B	ALOS6	TNE G7	RPOS7	BR DATA0	BR SIG0	BT SIG0	BR MFP 1	BT SIG1	BT CLK2	BT SIG2	BR DATA3	BTFP3	ALOS4	TNEG4	TCLK4	RCLK5
C	RNEG6	TCLK7	RCLK7	ALOS7	BR MFP 0	BR CLK1	BR FP1	BR CLK2	BR SIG2	BT MFP2	BR SIG3	BT MFP3	RNEG4	RPOS5	RNEG5	TNEG5
D	TNEG6	RCLK6	RPOS6	BR CLK0	BT FP0	BR SIG1	BT FP1	BR FP2	BR MFP2	BTFP2	BRFP3	BT SIG3	BT CLK3	TPOS5	TCLK5	TDI
E	SYS CLK	TCLK6	TPOS6	VSS	VSS	BT MFP0	BT CLK1	BT MFP1	VDD_CORE	BR CLK3	VDD_CORE	VSS	TDO	TCK	TMS	TRSTB
F	MTYPE	WEB	CSB	VSS	VDD_IO	VDD_CORE	VDD_IO	VSS	VSS	VDD_IO	VSS	VSS	BR DATA4	BR CLK4	BRFP4	BR MFP4
G	ADR14	ADR15	ADR13	VSS	VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_IO	BTFP4	BT DATA4	BR SIG4	BT CLK4
H	ADR11	ADR9	ADR10	ADR12	VSS	NC_1	VSS	VSS	VSS	VSS	VSS	BR CLK5	BR DATA5	BT MFP4	BT SIG4	BRFP5
J	ADR8	ADR5	ADR7	ADR4	VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_IO	BR MFP5	BT CLK5	BR SIG5	BT DATA5
K	ADR6	ADR0	ADR2	ADR3	VDD_IO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	BT MFP5	BR DATA6	BR CLK6	BT SIG5
L	ADR1	DB0	DB2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE	BT FP5	BT MFP6	BTFP6	BRFP6
M	DB3	DB5	DB6	DB1	VSS	VDD_CORE	VDD_IO	VDD_CORE	VDD_IO	VDD_CORE	VSS	VSS	BR SIG6	BT DATA6	BTSIG6	BR MFP6
N	DB7	TCLK1	RCLK1	DB4	VSS	VSS	VSS	VSS	VSS	VSS	ALOS2	I/M #	BT CLK6	TCLK2	RDYB	RWB
P	TNEG1	RNEG1	TPOS1	ALOS0	E1X24	NC_5	SCAN EN	NC_3	BT MFP7	BR SIG7	BRFP7	RNEG3	TNEG3	DSB	TNEG2	INTB
R	RPOS1	TCLK0	TNEG0	RNEG0	REF CLK	RE SETB	TEST ENB	NC_4	BT SIG7	BT CLK7	BR DATA7	ALOS3	RCLK3	TCLK3	RPOS2	TPOS2
T	ALOS1	TPOS0	RCLK0	RPOS0	T1X24	NC_6	TRI STB	NC_2	BT FP7	BT DATA7	BR MFP7	BR CLK7	RPOS3	TPOS3	RNEG2	RCLK2

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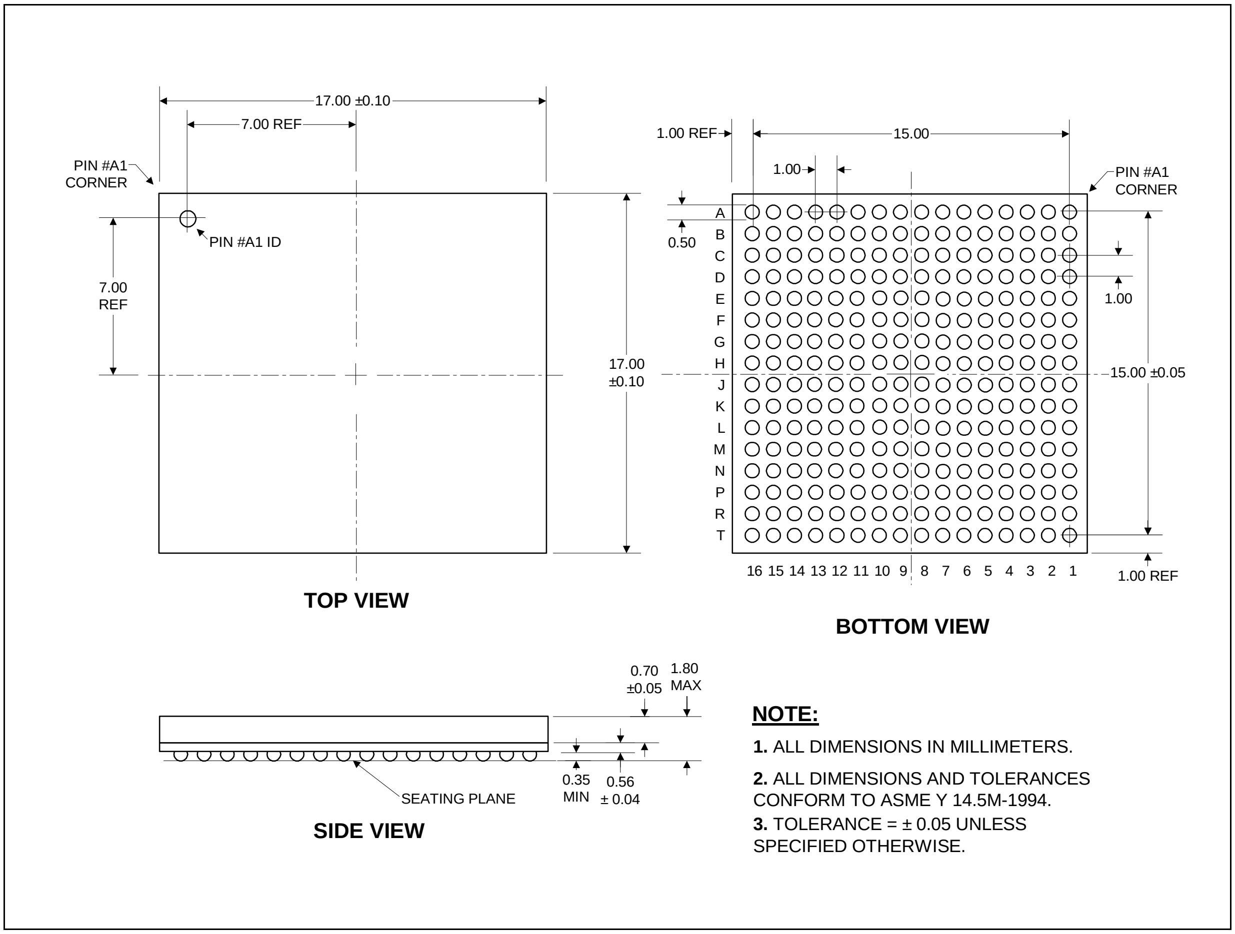
Figure 60. IXF3208 256 PBGA Mechanical Specification



Glossary 27

Term Categories

Term	Term definition
AIS	Alarm Indication Signal
AMI	Alternate Mark Inversion
AUXP	Auxiliary Pattern
B8ZS	Binary Eight Zero Substitution
BBER	Background Block Error Ratio
BEB	Background Error Block
BFA	Basic Frame Alignment
BERT	Bit Error Rate Test
BPV	BiPolar Violation
BSR	Boundary Scan Register
BOP	Bit Oriented Protocol
CAS	Channel Associated Signaling
CCS	Common Channel Signaling
CHI	Concentration Highway Interface
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
COFA	Change Of Frame Alignment
DDL	Derived Data Link
EB	Errored Block
EOM	End Of Message
ES	Errored Second
ESR	Errored Seconds Ratio
EXZ	Excess Zeroes
FAS	Frame Alignment Signal
FCS	Frame Check Sequence
FDL	Facility Data Link
FSM	Finite State Machine
FIFO	First In, First Out
FCS	Frame Check Sequence

GR-303	Generic Requirements-303
HDB3	High Density Bipolar Three
HDLC	High level Data Link Control
IAD	Integrated Access Devices
IMA	Inverse Multiplexing for ATM
IMAP	Integrated Multi-service Access Platform
I/O	In Out
ISDN	Integrated Service Digital Network
JTAP	Joint Test Access Port
LAPB	Link Access Procedure Balanced
LAPD	Link Access Procedure D
LH	Long Haul
LH/SH	Long Haul/Short Haul
LIU	Line Interface Unit
LLB	Line LoopBack
LOF	Loss Of Frame
LOS	Loss Of Signal
MFAS	Multiframe Alignment Signals
MOP	Message Oriented Protocol
Mbps	Megabits per second
MVIP	Multi-Vendor Integration Protocol
NFAS	Not Frame Alignment Signal
NEG	Negative
OVF	Over Flow
OOF	Out Of Frame
PLB	Payload LoopBack
PBGA	Plastic Ball Grid Array
PCM	Pulse Code Modulation
REBE	Remote End Block Error
POS	Positive
PRBS	Pseudo-Random Bit Sequence
PRM	Performance Report Messaging
PTM	Pulse Template Matching
RAI	Remote Alarm Indication
RAM	Random Access Memory

REBE	Remote End Block Error
SAPI	Service Access Point Identifier
SES	Severely Errored Second
SESR	Severely Errored Seconds Ratio
SLC-96	Subscriber Loop Carrier
SH	Short Haul
SF	SuperFrame
TAP	Test Access Port
TDM	Time Division Multiplex
TE1	Terminal Endpoint Identifier
TMS	Test Mode Select
TLB	Timeslot LoopBack
UNF	Under Flow
ZCS	Zero Code Suppression