



## ***LP62S16512-I Series***

### ***512K X 16 BIT LOW VOLTAGE CMOS SRAM***

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#### **Document Title**

**512K X 16 BIT LOW VOLTAGE CMOS SRAM**

#### **Revision History**

<b><u>Rev. No.</u></b>	<b><u>History</u></b>	<b><u>Issue Date</u></b>	<b><u>Remark</u></b>
0.2	Add Product Family and 55ns specification	March 20, 2002	Preliminary
1.0	Change Icc2 from 15mA to 8mA Final version release	May 26, 2003	Final



## LP62S16512-I Series

### 512K X 16 BIT LOW VOLTAGE CMOS SRAM

#### Features

- Operating voltage: 2.7V to 3.6V
- Access times: 55/70 ns (max.)
- Current:
  - Very low power version: Operating: 50mA (max.)
  - Standby: 20μA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 2.0V (min.)
- Available in 48-ball CSP (8×10mm) packages

#### General Description

The LP62S16512-I is a low operating current 8,388,608-bit static random access memory organized as 524,288 words by 16 bits and operates on low power voltage from 2.7V to 3.6V. It is built using AMIC's high performance CMOS process.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Two chip enable input is provided for POWER-DOWN, device enable. Two byte enable inputs and an output enable input are included for easy interfacing.

Data retention is guaranteed at a power supply voltage as low as 2.0V.

#### Product Family

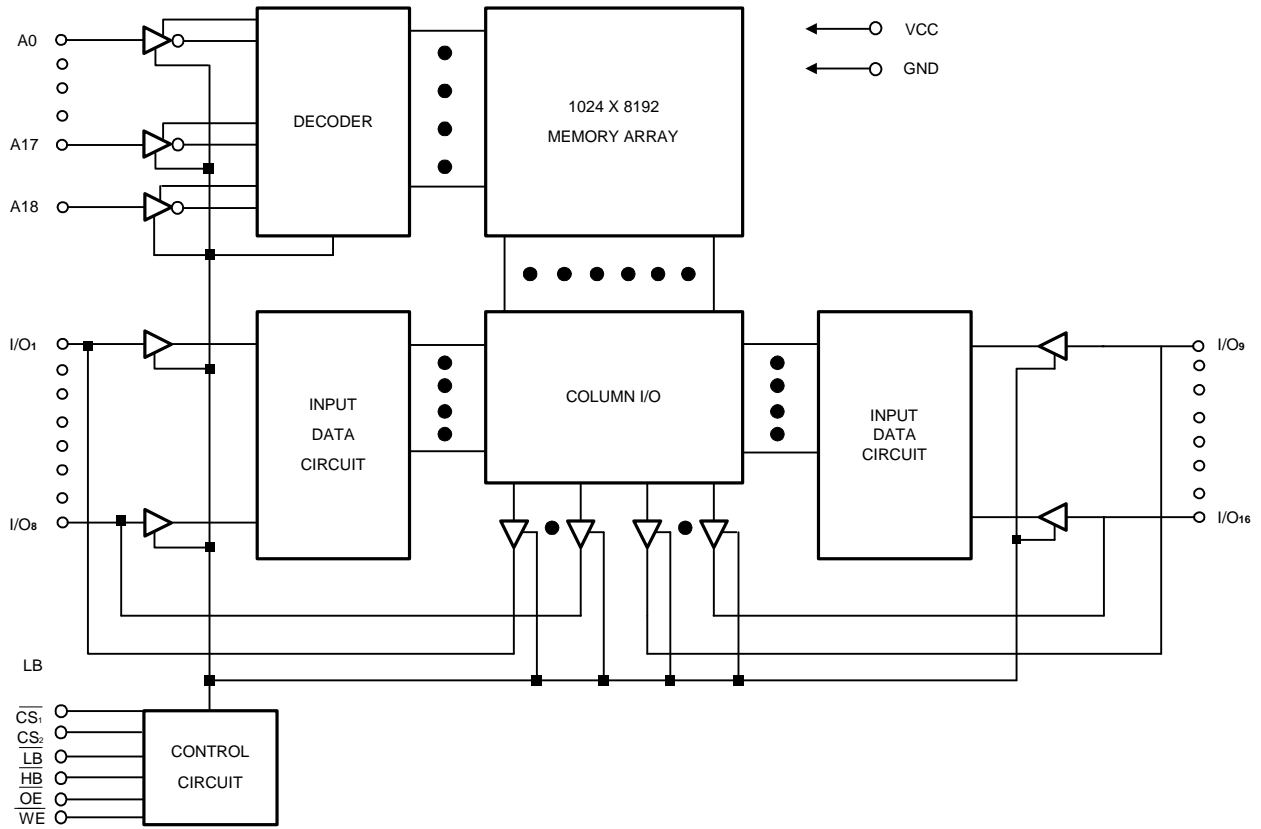
Product Family	Operating Temperature	VCC Range	Speed	Power Dissipation			Package Type
				Data Retention (I <sub>CCDR</sub> , Typ.)	Standby (I <sub>SB1</sub> , Typ.)	Operating (I <sub>CC2</sub> , Typ.)	
LP62S16512	-40°C ~ +85°C	2.7V~3.6V	55ns / 70ns	0.3μA	0.5μA	4mA	48 CSP

1. Typical values are measured at VCC = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.
2. Data retention current VCC = 2.0V.

#### Pin Configurations

##### ■ CSP (Chip Size Package) 48-pin Top View

	1	2	3	4	5	6
A	LB	OE	A0	A1	A2	CS <sub>2</sub>
B	I/O <sub>9</sub>	HB	A3	A4	CS <sub>1</sub>	I/O <sub>1</sub>
C	I/O <sub>10</sub>	I/O <sub>11</sub>	A5	A6	I/O <sub>2</sub>	I/O <sub>3</sub>
D	GND	I/O <sub>12</sub>	A17	A7	I/O <sub>4</sub>	VCC
E	VCC	I/O <sub>13</sub>	NC	A16	I/O <sub>5</sub>	GND
F	I/O <sub>15</sub>	I/O <sub>14</sub>	A14	A15	I/O <sub>6</sub>	I/O <sub>7</sub>
G	I/O <sub>16</sub>	NC	A12	A13	WE	I/O <sub>8</sub>
H	A18	A8	A9	A10	A11	NC

**Block Diagram**


**Pin Description - CSP**

Symbol	Description	Symbol	Description
A0 - A18	Address Inputs	$\overline{\text{HB}}$	Higher Byte Enable Input (I/O <sub>9</sub> - I/O <sub>16</sub> )
$\overline{\text{CS}}_1$ , CS <sub>2</sub>	Chip Enable	$\overline{\text{OE}}$	Output Enable
I/O <sub>1</sub> - I/O <sub>16</sub>	Data Input/Output	VCC	Power Supply
$\overline{\text{WE}}$	Write Enable Input	GND	Ground
$\overline{\text{LB}}$	Byte Enable Input (I/O <sub>1</sub> - I/O <sub>8</sub> )	NC	No Connection

**Recommended DC Operating Conditions**

 (T<sub>A</sub> = -40°C to + 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	2.7	3	3.6	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.0	-	VCC + 0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	+0.6	V
C <sub>L</sub>	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

**Absolute Maximum Ratings\***

VCC to GND .....-0.5V to +4.0V  
 IN, IN/OUT Volt to GND ..... -0.5V to VCC + 0.5V  
 Operating Temperature, Topr .....-40°C to +85°C  
 Storage Temperature, Tstg.....-55°C to +125°C  
 Power Dissipation, Pr..... 0.7W

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics** (TA = -40°C to + 85°C, VCC = 2.7V to 3.6V, GND = 0V)

Symbol	Parameter	LP62S16512-55/70LLI		Unit	Conditions
		Min.	Max.		
$I_{Li}$	Input Leakage Current	-	1	$\mu$ A	$V_{IN} = GND$ to VCC
$I_{Lo}$	Output Leakage Current	-	1	$\mu$ A	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{LB} = \overline{HB} = V_{IH}$ $V_{Io} = GND$ to VCC
$I_{cc}$	Active Power Supply Current	-	5	mA	$\overline{CS1} = V_{IL}$ , $CS2 = V_{IH}$ , $\overline{LB} = V_{IL}$ or $\overline{HB} = V_{IL}$ , $I_{Io} = 0mA$
$I_{cc1}$	Dynamic Operating Current	-	50	mA	Min. Cycle, Duty = 100%, $\overline{CS1} = V_{IL}$ , $CS2 = V_{IH}$ , $\overline{LB} = V_{IL}$ or $\overline{HB} = V_{IL}$ $I_{Io} = 0mA$
$I_{cc2}$		-	8	mA	$\overline{CS1} \leq 0.2V$ , $CS2 \geq VCC-0.2V$ , $\overline{LB} \leq 0.2V$ or $\overline{HB} \leq 0.2V$ $f = 1MHz$ , $I_{Io} = 0mA$
$I_{SB}$	Standby Current	-	1	mA	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{LB} = \overline{HB} = V_{IH}$
$I_{SB1}$		-	20	$\mu$ A	$\overline{CS1} \geq VCC - 0.2V$ or $CS2 \leq 0.2V$ or $\overline{LB} = \overline{HB} \geq VCC-0.2V$ $V_{IN} \geq VCC-0.2V$ or $V_{IN} \leq 0.2V$
$V_{oL}$	Output Low Voltage	-	0.4	V	$I_{oL} = 2.1 mA$
$V_{oH}$	Output High Voltage	2.2	-	V	$I_{oH} = -1.0 mA$

**Truth Table**

$\overline{CS}_1$	$CS_2$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{HB}$	I/O <sub>1</sub> to I/O <sub>8</sub> Mode	I/O <sub>9</sub> to I/O <sub>16</sub> Mode	VCC Current
H	X	X	X	X	X	High - Z	High - Z	I <sub>SB1</sub> , I <sub>SB</sub>
X	L	X	X	X	X	High - Z	High - Z	I <sub>SB1</sub> , I <sub>SB</sub>
X	X	X	X	H	H	High - Z	High - Z	I <sub>SB1</sub> , I <sub>SB</sub>
L	H	L	H	L	L	Read	Read	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
				L	H	Read	High - Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
				H	L	High - Z	Read	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
L	H	X	L	L	L	Write	Write	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
				L	H	Write	High - Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
				H	L	High - Z	Write	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
L	H	H	H	L	X	High - Z	High - Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
L	H	H	H	X	L	High - Z	High - Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>

Note: X = H or L

**Capacitance** (T<sub>A</sub> = 25°C, f = 1.0MHz)

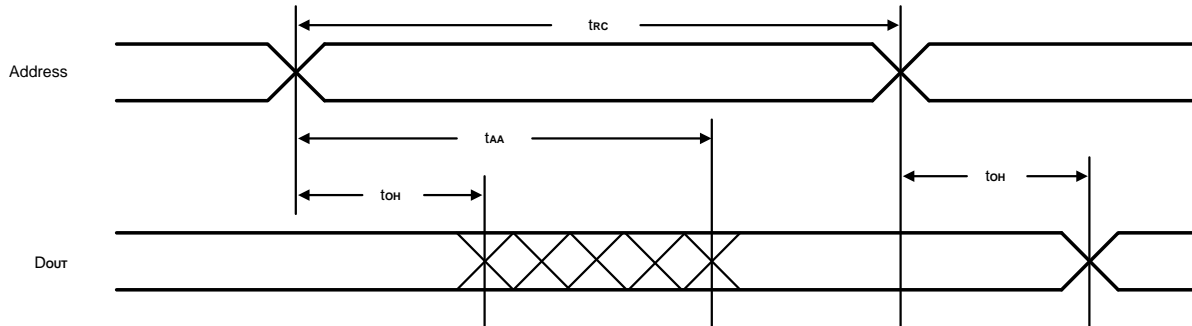
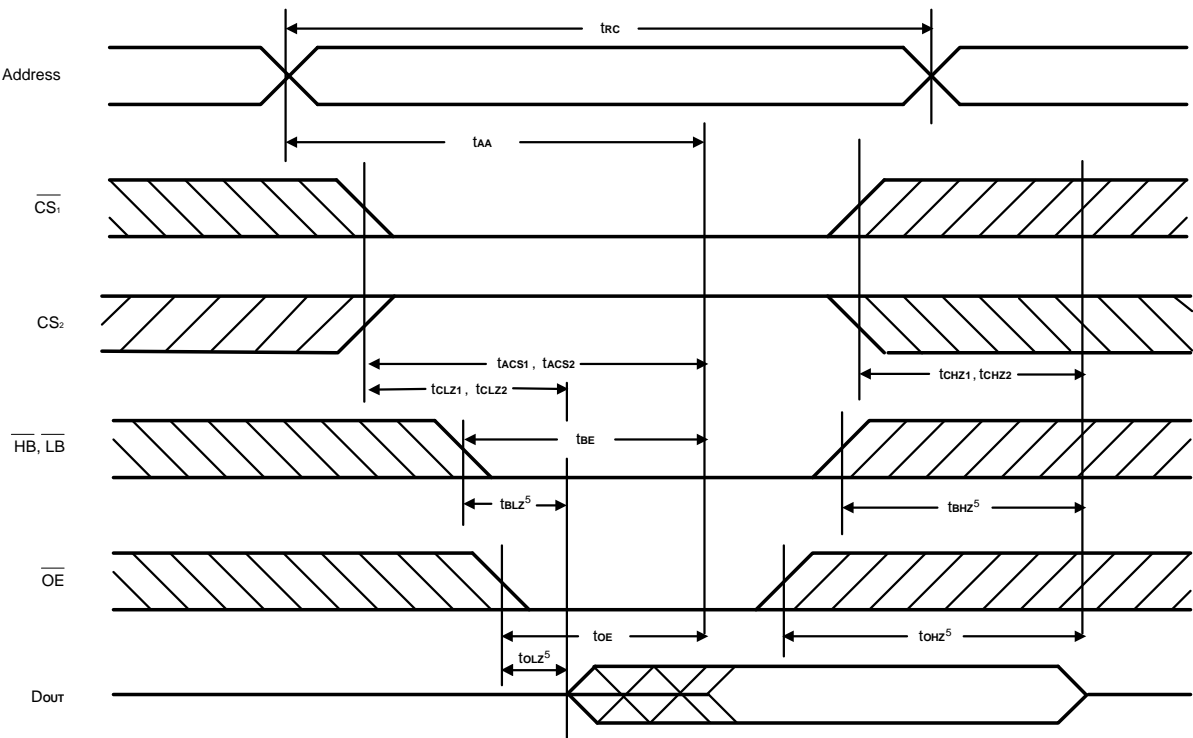
Symbol	Parameter	Min.	Max.	Unit	Conditions
C <sub>IN</sub> *	Input Capacitance		6	pF	V <sub>IN</sub> = 0V
C <sub>I/O</sub> *	Input/Output Capacitance		8	pF	V <sub>I/O</sub> = 0V

\* These parameters are sampled and not 100% tested.

**AC Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$ )

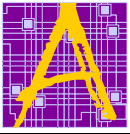
Symbol	Parameter	LP62S16512-55LLI		LP62S16512-70LLI		Unit
		Max.	Min.	Min.	Max.	
Read Cycle						
t <sub>RC</sub>	Read Cycle Time	55	-	70	-	ns
t <sub>AA</sub>	Address Access Time	-	55	-	70	ns
t <sub>Acs1</sub> , t <sub>Acs2</sub>	Chip Enable Access Time	-	55	-	70	ns
t <sub>BE</sub>	Byte Enable Access Time	-	55	-	70	ns
t <sub>OE</sub>	Output Enable to Output Valid	-	25	-	35	ns
t <sub>CLZ1</sub> , t <sub>CLZ2</sub>	Chip Enable to Output in Low Z	10	-	10	-	ns
t <sub>BLZ</sub>	Byte Enable to Output in Low Z	10	-	10	-	ns
t <sub>OLZ</sub>	Output Enable to Output in Low Z	5	-	5	-	ns
t <sub>CHZ1</sub> , t <sub>CHZ2</sub>	Chip Disable to Output in High Z	-	20	-	25	ns
t <sub>BHZ</sub>	Byte Disable to Output in High Z	-	20	-	25	ns
t <sub>OHZ</sub>	Output Disable to Output in High Z	-	20	-	25	ns
t <sub>OH</sub>	Output Hold from Address Change	5	-	5	-	ns
Write Cycle						
t <sub>WC</sub>	Write Cycle Time	55	-	70	-	ns
t <sub>cw1</sub> , t <sub>cw2</sub>	Chip Enable to End of Write	50	-	60	-	ns
t <sub>BW</sub>	Byte Enable to End of Write	50	-	60	-	ns
t <sub>AS</sub>	Address Setup Time	0	-	0	-	ns
t <sub>AW</sub>	Address Valid to End of Write	50	-	60	-	ns
t <sub>WP</sub>	Write Pulse Width	40	-	50	-	ns
t <sub>WR</sub>	Write Recovery Time	0	-	0	-	ns
t <sub>WHZ</sub>	Write to Output in High Z	-	25	-	25	ns
t <sub>DW</sub>	Data to Write Time Overlap	25	-	30	-	ns
t <sub>DH</sub>	Data Hold from Write Time	0	-	0	-	ns
t <sub>OW</sub>	Output Active from End of Write	5	-	5	-	ns

Note: t<sub>CLZ1</sub>, t<sub>CLZ2</sub>, t<sub>BLZ</sub>, t<sub>OLZ</sub>, t<sub>CHZ1</sub>, t<sub>CHZ2</sub>, t<sub>BHZ</sub> and t<sub>OHZ</sub> and t<sub>WHZ</sub> are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

**Timing Waveforms**
**Read Cycle 1<sup>(1, 2, 4)</sup>**

**Read Cycle 2<sup>(1, 2, 3)</sup>**


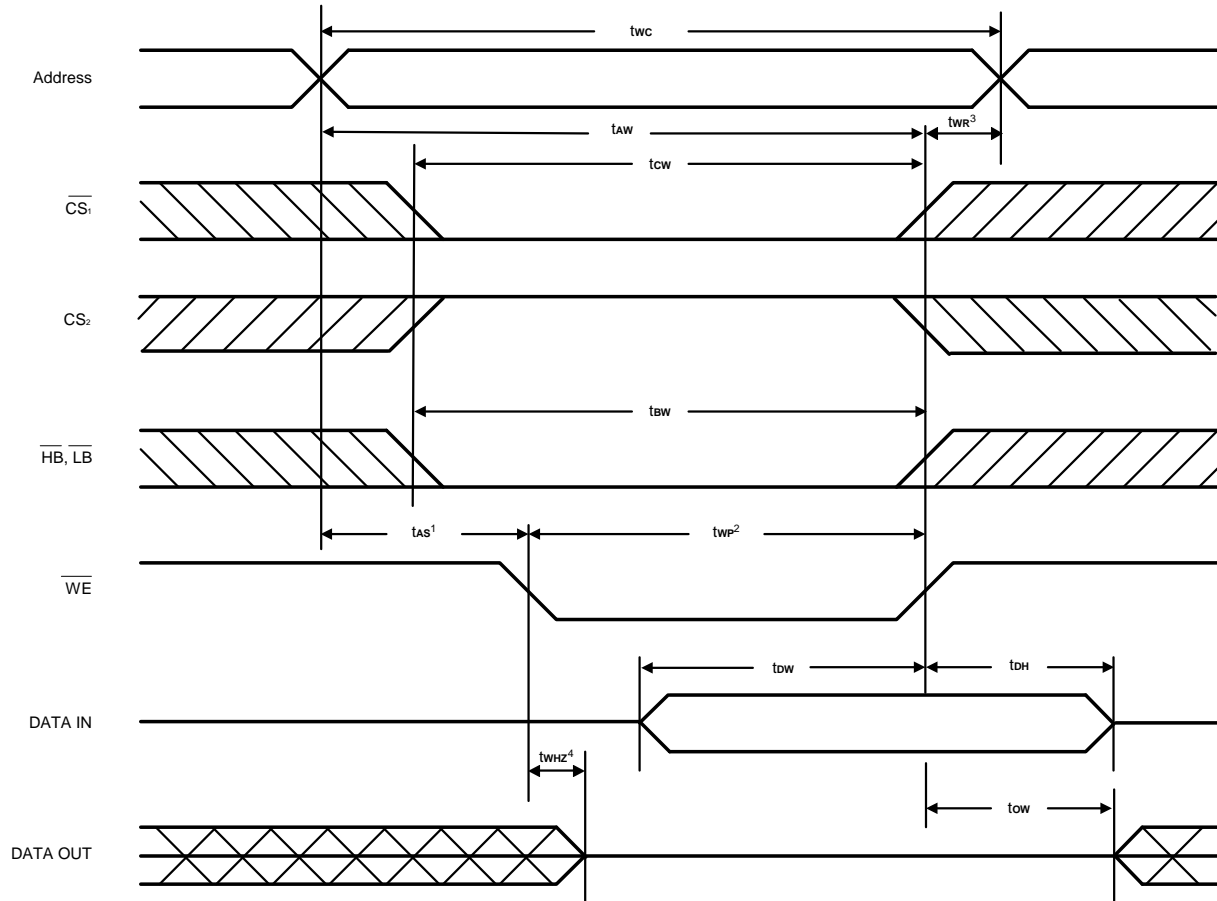
- Notes:
- $\overline{WE}$  is high for Read Cycle.
  - Device is continuously enabled  $\overline{CS}_1 = V_{IL}$ , or  $CS_2 = V_{IH}$ ,  $\overline{HB} = V_{IL}$  and, or  $\overline{LB} = V_{IL}$ .
  - Address valid prior to or coincident with  $\overline{CS}_1$  and ( $\overline{HB}$  and, or  $\overline{LB}$ ) transition low or  $CS_2$  transition High.
  - $\overline{OE} = V_{IL}$ .
  - Transition is measured  $\pm 500mV$  from steady state. This parameter is sampled and not 100% tested.

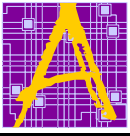




Timing Waveforms (continued)

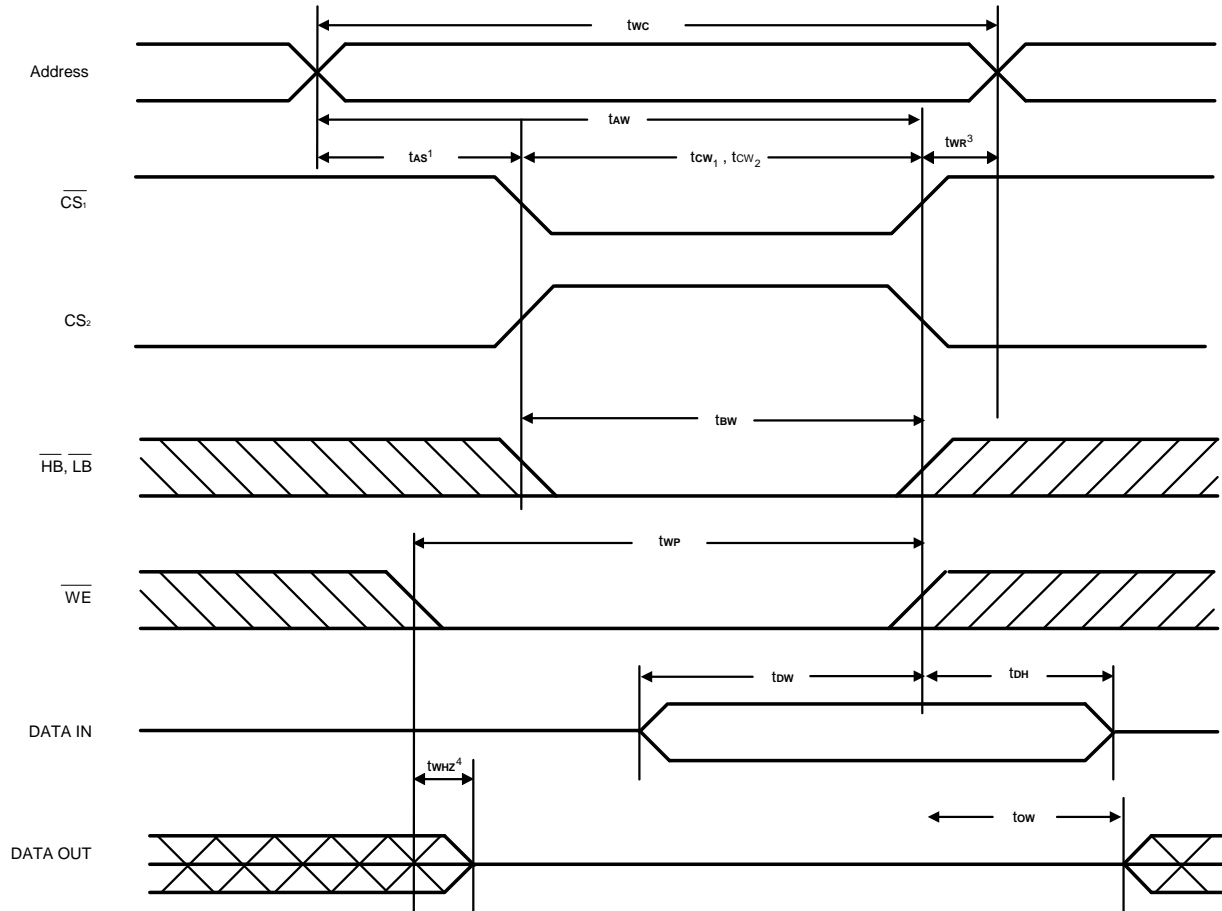
Write Cycle 1  
(Write Enable Controlled)

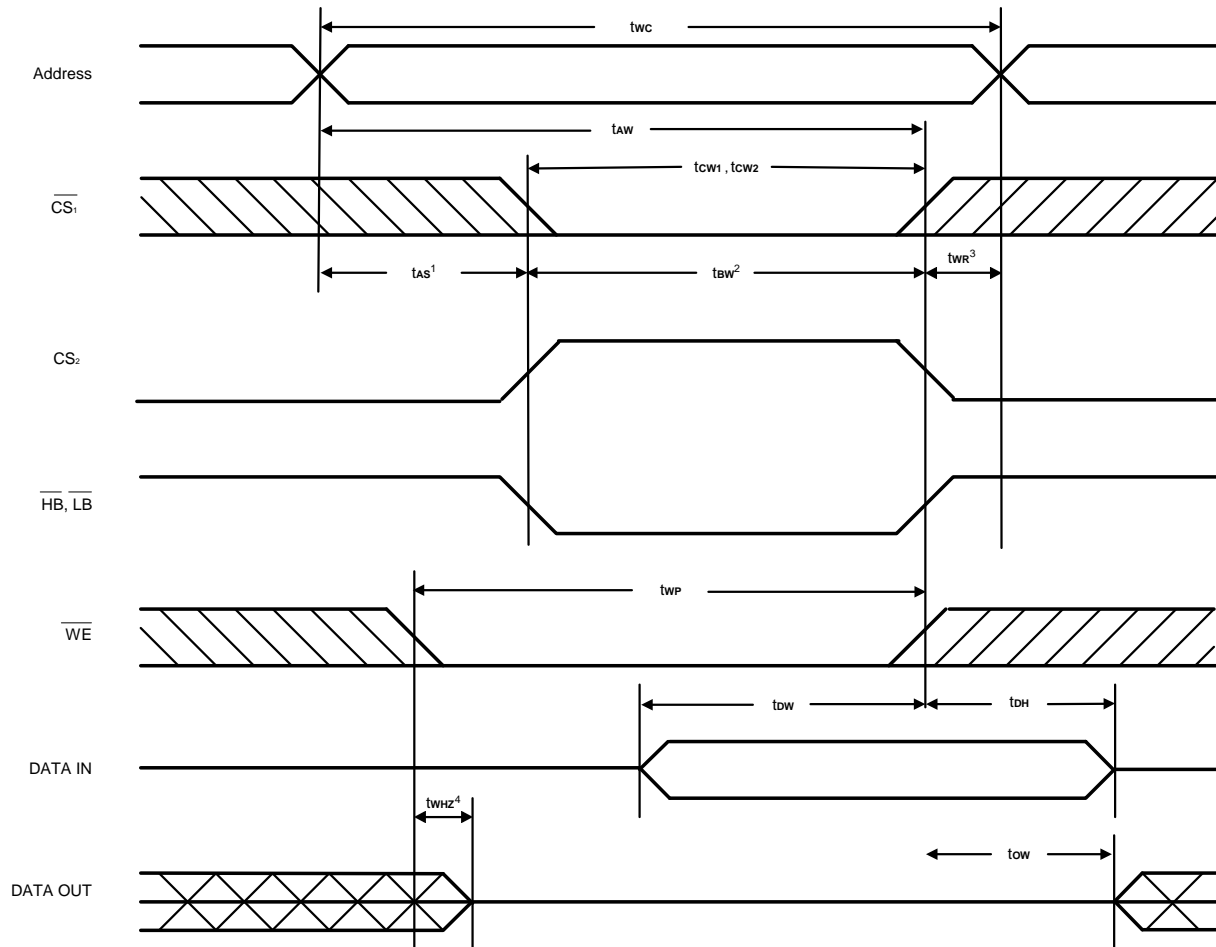




Timing Waveforms (continued)

Write Cycle 2  
(Chip Enable Controlled)

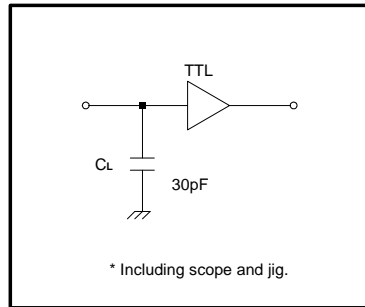
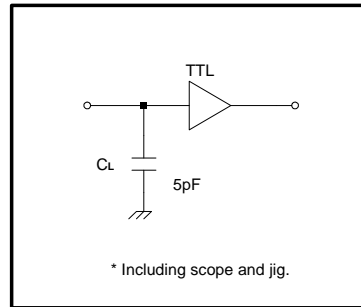


**Timing Waveforms (continued)**
**Write Cycle 3  
(Byte Enable Controlled)**


- Notes:
1.  $t_{AS}^1$  is measured from the address valid to the beginning of Write.
  2. A Write occurs during the overlap ( $t_{WP}, t_{BW}$ ) of a low  $\overline{CS}_1$ ,  $\overline{WE}$  and ( $\overline{HB}$  and , or  $\overline{LB}$ ) or a high  $\overline{CS}_2$ .
  3.  $t_{WR}^3$  is measured from the earliest of  $\overline{CS}_1$  or  $\overline{WE}$  or ( $\overline{HB}$  and , or  $\overline{LB}$ ) going high or  $\overline{CS}_2$  going Low to the end of the Write cycle.
  4.  $\overline{OE}$  level is high or low.
  5. Transition is measured  $\pm 500\text{mV}$  from steady state. This parameter is sampled and not 100% tested.

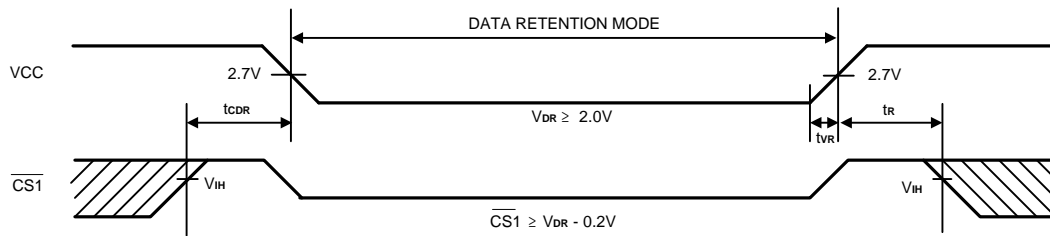
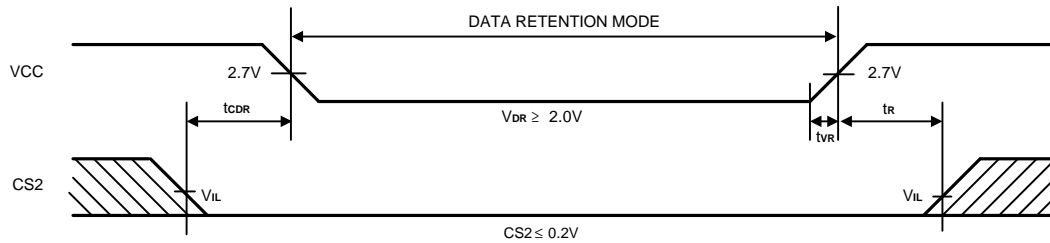
**AC Test Conditions**

Input Pulse Levels	0.4V to 2.4V
Input Rise And Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2


**Figure 1. Output Load**

**Figure 2. Output Load for t<sub>CLZ1</sub>, t<sub>CLZ2</sub>, t<sub>BHZ</sub>, t<sub>BLZ</sub>, t<sub>OLZ</sub>, t<sub>CHZ1</sub>, t<sub>CHZ2</sub>, t<sub>OHZ</sub>, t<sub>WHZ</sub>, and t<sub>OW</sub>**
**Data Retention Characteristics** (T<sub>A</sub> = -40°C to 85°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V <sub>DR</sub>	VCC for Data Retention	2.0	3.6	V	$\overline{CS}_1 \geq VCC - 0.2V$ or $CS_2 \leq 0.2V$ or $\overline{LB} = \overline{HB} \geq VCC-0.2V$
I <sub>CCDR</sub>	Data Retention Current	-	6*	μA	VCC = 2.0V, $\overline{CS}_1 \geq VCC - 0.2V$ or $CS_2 \leq 0.2V$ or $\overline{LB} = \overline{HB} \geq VCC-0.2V$ V <sub>IN</sub> ≥ VCC-0.2V or V <sub>IN</sub> ≤ 0.2V
t <sub>CDR</sub>	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
t <sub>R</sub>	Operation Recovery Time	t <sub>RC</sub>	-	ns	
t <sub>VR</sub>	VCC Rising Time from Data Retention Voltage to Operating Voltage	5	-	ms	

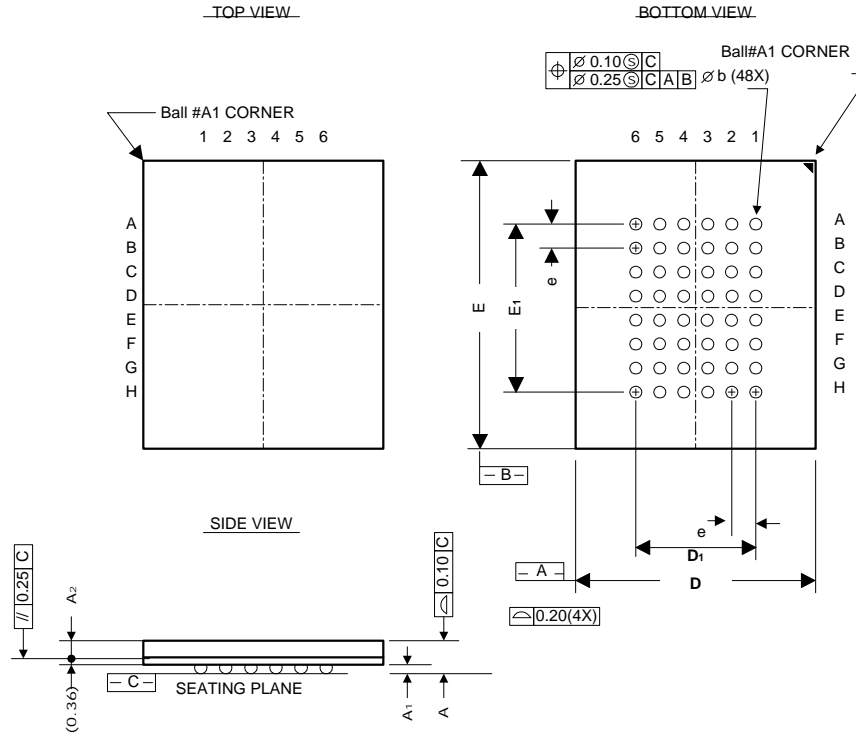
\* LP62S16512-55/70LLI      I<sub>CCDR</sub>: max. 1μA at T<sub>A</sub> = 25°C  
(3μA at T<sub>A</sub> = 0°C to + 40°C)

**Low VCC Data Retention Waveform (1) (CS1 Controlled)**

**Low VCC Data Retention Waveform (2) (CS2 Controlled)**

**Ordering Information**

Part No.	Access Time(ns)	Operating Current Max.(mA)	Standby Current Max.(uA)	Package
LP62S16512U-55LLI	55	50	20	48L CSP
LP62S16512U-70LLI	70	50	20	48L CSP

**Package Information**
**48LD CSP ( 8 x 10 mm ) Outline Dimensions  
(48TFBGA)**

unit: mm



Symbol	Dimensions in mm		
	MIN.	NOM.	MAX.
A	1.04	1.14	1.24
A <sub>1</sub>	0.20	0.25	0.30
A <sub>2</sub>	0.48	0.53	0.58
D	7.90	8.00	8.10
D <sub>1</sub>	---	3.75	---
E <sub>1</sub>	---	5.25	---
e	---	0.75	---
b	0.30	0.35	0.40

**Notes:**

1. THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC MO192 (LOW PROFILE BGA FAMILY).
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM.  
THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
4. BALL PAD OPENING OF SUBSTRATE IS  $\phi$  0.3mm (SMD)  
SUGGEST TO DESIGN THE PCB LAND SIZE AS  $\phi$  0.3mm (NSMD)