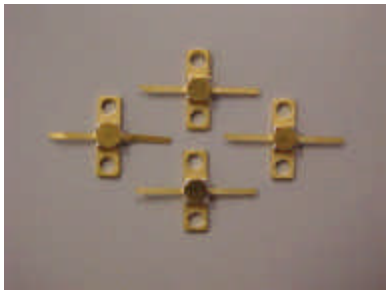
LP750P100

PACKAGED 0.5 WATT POWER PHEMT



- FEATURES
  - ♦ 41 dBm IP3 at 12 GHz
  - ♦ 27.5 dBm P-1dB at 12 GHz
  - ♦ 10.5 dB Power Gain at 12 GHz
  - ♦ 2.5 dB Noise Figure at 12 GHz
  - ♦ 60% Power-Added-Efficiency

- DESCRIPTION AND APPLICATIONS

The LP750P100 is a packaged Aluminum Gallium Arsenide/Indium Gallium Arsenide (AlGaAs/InGaAs) Pseudomorphic High Electron Mobility Transistor (PHEMT), utilizing an Electron-Beam direct-write 0.25 µm Schottky barrier gate. The recessed "mushroom" gate structure minimizes parasitic gate-source and gate resistances. The epitaxial structure and processing have been optimized for reliable high-power/low-noise applications. The LP750 also features Si_3N_4 passivation and is available in die form or in surface-mount packages.

The LP750P100 is designed for medium-power, linear amplification. This device is suitable for applications in commercial and military environments, and it is appropriate to be used as a medium power transistor in SATCOM uplink transmitters, medium-haul digital radio transmitters, PCS high efficiency amplifiers, and WLL systems.

- ELECTRICAL SPECIFICATIONS @ $T_{Ambient}$ = 22 ± 3 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Power @ 1 dB Compression	P_{1dB}	f = 12GHz; V_{DS} = 8V; I_{DS} = 50% I_{DSS}	26.0	27.5		dBm
Power Gain @ 1 dB Compression	G_{1dB}	f = 12GHz; V_{DS} = 8V; I_{DS} = 50% I_{DSS}	9.0	10.5		dB
Maximum Available Gain	MAG	f = 12GHz; V_{DS} = 8V; I_{DS} = 50% I_{DSS}		14.0		dB
Noise Figure	NF	f = 12GHz; V_{DS} = 5V; I_{DS} = 33% I_{DSS}		2.5		dB
Power-Added Efficiency	η	f = 12GHz; V_{DS} = 5V; I_{DS} = 50% I_{DSS}; P_{OUT} = 25dBm		60		%
Output Intercept Point	IP_3	f = 12GHz; V_{DS} = 8V; I_{DS} = 50% I_{DSS}; P_{OUT} = 10dBm		41		dBm
Saturated Drain-Source Current	I_{DSS}	V_{DS} = 2V; V_{GS} = 0V	180		265	mA
Transconductance	G_M	V_{DS} = 2V; V_{GS} = 0V	230	280		mS
Pinch-Off Voltage	V_P	V_{DS} = 2V; I_{DS} = 4mA	-2.0	-1.2	-0.25	V
Gate-Drain Breakdown Voltage Magnitude	$\|V_{BDGD}\|$	I_{GD} = 4mA	12	15		V
Gate-Source Breakdown Voltage Magnitude	$\|V_{BDGS}\|$	I_{GS} = 4mA	12	16		V
Gate-Source Leakage Current Magnitude	$\|I_{GSL}\|$	V_{GS} = -5V		5	45	µA

• RECOMMENDED CONTINUOUS OPERATING LIMITS

Parameter	Symbol	Nominal	Units
Drain-Source Voltage	V_{DS}	8	V
Gate-Source Voltage	V_{GS}	-1.2	V
Drain-Source Current	I_{DS}	0.8 I_{DSS}	mA
RF Input Power	P_{IN}	150	mW
Channel Operating Temperature	T_{CH}	150	°C
Ambient Temperature	T_{STG}	-20/50	°C

Notes: Device should be operated at or below Recommended Continuous Operating Limits for reliable performance.

• ABSOLUTE RATINGS

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	V_{DS}	$T_{Ambient}$ = 22 ± 3 °C		12	V
Gate-Source Voltage	V_{GS}	$T_{Ambient}$ = 22 ± 3 °C		-4	V
Drain-Source Current	I_{DS}	$T_{Ambient}$ = 22 ± 3 °C		200% I_{DSS}	mA
Gate Current	I_G	$T_{Ambient}$ = 22 ± 3 °C		35	mA
RF Input Power	P_{IN}	$T_{Ambient}$ = 22 ± 3 °C		250	mW
Channel Operating Temperature	T_{CH}	$T_{Ambient}$ = 22 ± 3 °C		175	ºC
Storage Temperature	T_{STG}	—	-65	175	ºC

Notes: Even temporary operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.

• APPLICATIONS NOTES & DESIGN DATA

Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site.

• HANDLING PRECAUTIONS

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly and, testing. These devices should be treated as Class 1A (0-500 V). Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

- PACKAGE OUTLINE

dimensions in mils, tolerance = ± 2 mils