TENTATIVE TOSHIBA HYBRID DIGITAL INTEGRATED CIRCUIT

16,777,216-WORD BY 64-BIT SYNCHRONOUS DRAM MODULE

DESCRIPTION

The THLY12N11C is a 16,777,216-word by 64-bit synchronous dynamic RAM module consisting of four TC59SM816CFT/CFTL DRAMs on a printed circuit board.

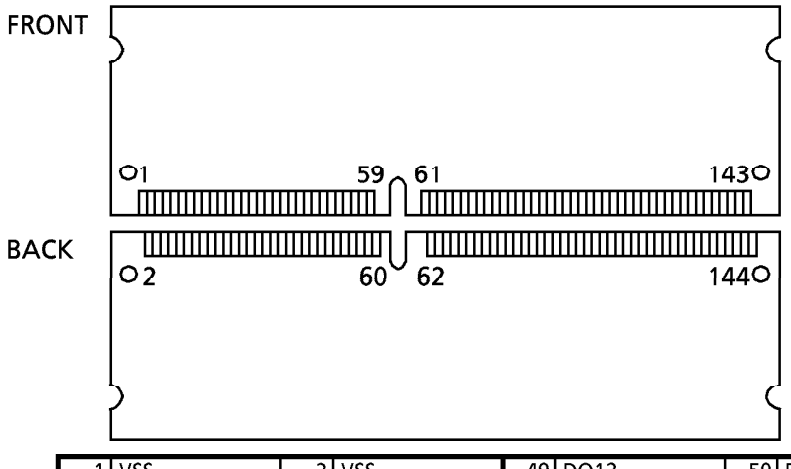
FEATURES

- 16,777,216-word by 64-bit organization

		70/70L	75/75L	80/80L
t_{CK}	Clock Cycle Time (CL = 3)	7 ns	7.5 ns	8 ns
t_{RAS}	Active-to-Precharge Command Period (min)	40 ns	45 ns	48 ns
t_{AC}	Access Time from CLK (CL = 3)	5.4 ns	5.4 ns	6 ns
t_{RC}	Ref/Active-to-Ref/Active Command Period (min)	56 ns	65 ns	68 ns

- Single power supply of 3.3 V ± 0.3 V
- Pipeline architecture
- Auto-Refresh and Self-Refresh capability
- All inputs and outputs LVTTL-compatible
- 8192 Refresh cycles per 64 ms
- Package: 144-pin small-outline DIMM (gold contacts)
- Based on Intel PC100 SOD Rev.1.0
- Based on PC133

PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

A0 ~ A12	Address Inputs
BA0, BA1	Bank Select
DQ0 ~ DQ63	Data Inputs/Outputs
/CS0	Chip Select
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DQMB0 ~ DQMB7	Output Disable / Write Mask
CLK0	Clock Input
CKE	Clock Enable
SDA	Serial Data / Address for PD
SCL	Clock for PD
VDD	Power (+3.3 V)
VSS	Ground
NC	No Connection

1	VSS	2	VSS	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	VDD	102	VDD
7	DQ2	8	DQ34	55	VSS	56	VSS	103	A6	104	A7
9	DQ3	10	DQ35	57	NC	58	NC	105	A8	106	BA0
11	VDD	12	VDD	59	NC	60	NC	107	VSS	108	VSS
13	DQ4	14	DQ36	61	CLK0	62	CKE	109	A9	110	BA1
15	DQ5	16	DQ37	63	VDD	64	VDD	111	A10	112	A11
17	DQ6	18	DQ38	65	/RAS	66	/CAS	113	VDD	114	VDD
19	DQ7	20	DQ39	67	/WE	68	NC	115	DQMB2	116	DQMB6
21	VSS	22	VSS	69	/CS0	70	A12	117	DQMB3	118	DQMB7
23	DQMB0	24	DQMB4	71	NC	72	NC	119	VSS	120	VSS
25	DQMB1	26	DQMB5	73	NC	74	CLK1	121	DQ24	122	DQ56
27	VDD	28	VDD	75	VSS	76	VSS	123	DQ25	124	DQ57
29	A0	30	A3	77	NC	78	NC	125	DQ26	126	DQ58
31	A1	32	A4	79	NC	80	NC	127	DQ27	128	DQ59
33	A2	34	A5	81	VDD	82	VDD	129	VDD	130	VDD
35	VSS	36	VSS	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	VSS	92	VSS	139	VSS	140	VSS
45	VDD	46	VDD	93	DQ20	94	DQ52	141	SDA	142	SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	VDD	144	VDD

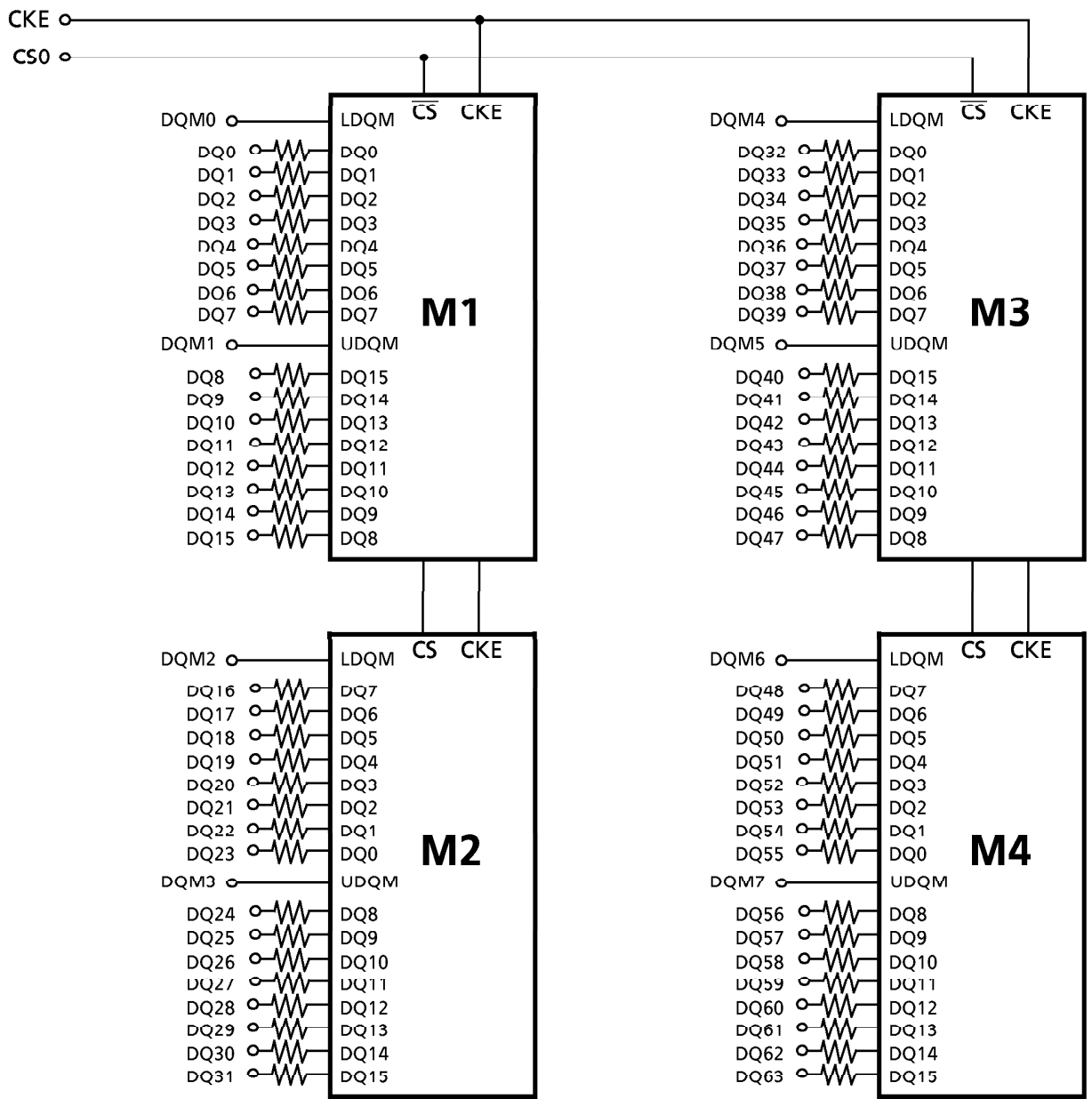
SERIAL PRESENCE DETECT (Rev.1.2B)

Byte Number	Function	70 / 70L		75 / 75L		80 / 80L	
		Entry Value	Entry	Entry Value	Entry	Entry Value	Entry
0	Defines # of Bytes of information Written into Serial Memory by Module Manufacturer Group	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total # of Bytes in SPD Memory Device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental Memory Type (FPM, EDO, SDRAM...) from Appendix A	SDRAM	04h	SDRAM	04h	SDRAM	04h
3	# of Row Addresses on this Assembly	RA0 ~ RA12	0Dh	RA0 ~ RA12	0Dh	RA0 ~ RA12	0Dh
4	# of Column Addresses on this Assembly	CA0 ~ CA8	09h	CA0 ~ CA8	09h	CA0 ~ CA8	09h
5	# of Module Banks on this Assembly	1 Bank	01h	1 Bank	01h	1 Bank	01h
6	Data Width of this Assembly...	x64	40h	x64	40h	x64	40h
7	...Data Width Continuation	x64	00h	x64	00h	x64	00h
8	Voltage Interface Standard of this Assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	SDRAM Cycle Time at Max. Supported CAS Latency (CL), @ CL = X	CL = 3, 7.0 ns	70h	CL = 3, 7.5 ns	75h	CL = 3, 8.0 ns	80h
10	SDRAM Access from Clock @ CL = X	CL = 3, 5.4 ns	54h	CL = 3, 5.4 ns	54h	CL = 3, 6.0 ns	60h
11	DIMM Configuration Type (Non-parity, Parity, ECC)	Non-Parity	00h	Non-Parity	00h	Non-Parity	00h
12	Refresh Rate/Type	7.8 μs/ Self-Refresh	82h	7.8 μs/ Self-Refresh	82h	7.8 μs/ Self-Refresh	82h
13	SDRAM Width, Primary DRAM	x16	10h	x16	10h	x16	10h
14	Error Checking SDRAM Data Width	NA	00h	NA	00h	NA	00h
15	Minimum Clock Delay, Back-to-Back Random Column Addresses	1 CLK	01h	1 CLK	01h	1 CLK	01h
16	Burst Lengths Supported	1, 2, 4, 8, Full page	8Fh	1, 2, 4, 8, Full page	8Fh	1, 2, 4, 8, Full page	8Fh
17	# of Banks on Each SDRAM Device	4 Banks	04h	4 Banks	04h	4 Banks	04h
18	CAS # Latencies Supported	2, 3	06h	2, 3	06h	2, 3	06h
19	CS # Latency		01h		01h		01h
20	WE # Latency		01h		01h		01h
21	SDRAM Module Attributes		00h		00h		00h
22	SDRAM Device Attributes: General		0Eh		0Eh		0Eh
23	Minimum Clock Cycle Time @ CL- X-1	CL = 2, 7.5 ns	75h	CL = 2, 10 ns	A0h	CL = 2, 10 ns	A0h
24	Maximum Data Access Time from Clock @ CL X-1	CL = 2, 5.4 ns	54h	CL = 2, 6.0 ns	60h	CL = 2, 6.0 ns	60h
25	Minimum Clock Cycle Time @ CL X-2		00h		00h		00h
26	Maximum Data Access Time from Clock @ CL X-2		00h		00h		00h
27	Minimum Row Precharge Time	15 ns	0Fh	20 ns	14h	20 ns	14h
28	Minimum Row Active to Row Active Delay	15 ns	0Fh	15 ns	0Fh	20 ns	14h
29	Minimum RAS-to-CAS Delay	15 ns	0Fh	20 ns	14h	20 ns	14h
30	Minimum RAS Pulse Width	42 ns	2Ah	45 ns	2Dh	48 ns	30h
31	Module/Bank Density	128 MB	20h	128 MB	20h	128 MB	20h
32	Command & Address Signal Input Set-up Time	1.5 ns	15h	1.5 ns	15h	2 ns	20h
33	Command & Address Signal Input Hold Time	0.8 ns	08h	0.8 ns	08h	1 ns	10h
34	Data Signal Input Set-up Time	1.5 ns	15h	1.5 ns	15h	2 ns	20h
35	Data Signal Input Hold Time	0.8 ns	08h	0.8 ns	08h	1 ns	10h
36-61	Superset Information (may be used in future)		00h		00h		FFh
62	SPD Revision	Rev. 1.2B	12h	Rev. 1.2B	12h	Rev. 1.2B	12h
63	Check sum for bytes 0 ~ 62	470h	70h	4B9h	B9h	1EE4h	E4h

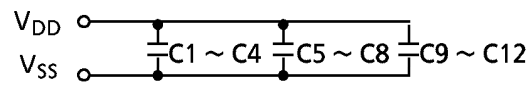
OPTIONAL

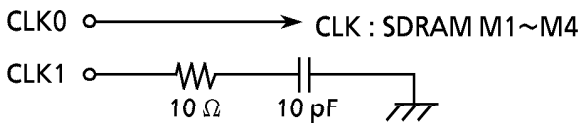
64	Manufacturers JEDEC ID Code (JEP-106E)						
65-71							
72	Place of Manufacture						
73-90	Manufacturer's Part Number						
91-92	Revision Code						
93-94	Date of Manufacture						
95-98	Assembly Serial Number						
99-125	Manufacturer-Specific Data						
126	Reserved	Intel Specification	64h	Intel Specification	64h	Intel Specification	64h
127	Reserved	Intel Specification	87h	Intel Specification	87h	Intel Specification	87h
128-255							

BLOCK DIAGRAM

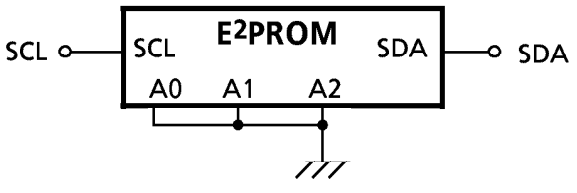


<SDRAM : M1~M4>





<EEPROM>



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	$-0.5 \sim V_{DD} + 0.3$	V	1
V_{OUT}	Output Voltage	$-0.5 \sim V_{DD} + 0.3$	V	1
V_{DD}	Power Supply Voltage	$-0.5 \sim 4.6$	V	1
T_{OPR}	Operating Temperature	$0 \sim 70$	°C	1
T_{STG}	Storage Temperature	$-55 \sim 125$	°C	1
P_D	Power Dissipation	2.7	W	1
I_{OUT}	Short-Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0° ~ 70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	2
V_{IH}	LVTTL Input High Voltage	2.0	–	$V_{DD} + 0.3$	V	2
V_{IL}	LVTTL Input Low Voltage	-0.5	–	0.8	V	2

Note : V_{IH}(max) = V_{DD} + 1.2V for pulse width ≦ 5ns
V_{IL}(min) = V_{SS} - 1.2V for pulse width ≦ 5ns

CAPACITANCE (V_{DD} = 3.3 V, f = 1 MHz, Ta = 0° ~ 70°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT
C_1	Input Capacitance	(A0 ~ A12)	–	35	pF
C_2	Input Capacitance	($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0, BA1)	–	35	pF
C_3	Input Capacitance	(CLK0)	–	45	pF
C_4	Input Capacitance	($\overline{CS0}$)	–	30	pF
C_5	Input Capacitance	(DQMB0 ~ DQMB7)	–	15	pF
C_6	Input Capacitance	(CKE)	–	30	pF
C_{DQ}	I/O Capacitance	(DQ0 ~ DQ63)	–	15	pF

DC CHARACTERISTICS (V_{DD} = 3.3 V ± 0.3 V, Ta = 0° ~ 70°C)

SYMBOL	ITEM		70/70L		75/75L		80/80L		UNIT	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
I_{CC1}	OPERATING CURRENT Active Precharge Command Cycling without Burst Operation (t_{CK} = t_{RC} min)	1-Bank Operation	–	320	–	300	–	280	mA	3
I_{CC2}	STANDBY CURRENT (t_{CK} = min, $\overline{CS}$ = V_{IH}, $V_{IH/L}$ = V_{IH} (min) / V_{IL} (max) Bank: Inactive State)	CKE = V_{IH}	–	160	–	140	–	120	mA	3
I_{CC2P}		CKE = V_{IL} (Power-Down Mode)	–	4	–	4	–	4		
I_{CC2S}	STANDBY CURRENT (CLK = V_{IL}, $\overline{CS}$ = V_{IH}, $V_{IH/L}$ = V_{IH} (min) / V_{IL} (max) Bank: Inactive State)	CKE = V_{IH}	–	40	–	40	–	40	mA	
I_{CC2PS}		CKE = V_{IL} (Power-Down Mode)	–	4	–	4	–	4		
I_{CC3}	NO OPERATING CURRENT (t_{CK} = min, $\overline{CS}$ = V_{IH} (min) Bank: Active State (4 Banks))	CKE = V_{IH}	–	240	–	220	–	200	mA	3
I_{CC3P}		CKE = V_{IL} (Power-Down Mode)	–	40	–	40	–	40		
I_{CC4}	BURST OPERATING CURRENT (t_{CK} = min, $\overline{CS}$ = V_{IH} (min) Read / Write Command Cycling)		–	400	–	380	–	360	mA	3, 4
I_{CC5}	AUTO-REFRESH CURRENT (t_{CK} = min, Auto Refresh Command Cycling)		–	680	–	640	–	600	mA	3
I_{CC6}	SELF-REFRESH CURRENT (Self Refresh Mode, CKE = 0.2 V)	THLY12N11C70,75,80	–	12	–	12	–	12	mA	3
		THLY12N11C70L,75L,80L	–	6.4	–	6.4	–	6.4		
$I_{I(L)}$	INPUT LEAKAGE CURRENT (0 V ≦ V_{IN} ≦ V_{DD}, All Other Pins Not under Test = 0 V)		– 5	5	– 5	5	– 5	5	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} Is Disabled, 0 V ≦ V_{OUT} ≦ V_{DD})		– 5	5	– 5	5	– 5	5	μA	
V_{OH}	OUTPUT LEVEL LVTTL Output H-Level Voltage (I_{OUT} = – 2 mA)		2.4	–	2.4	–	2.4	–	V	
V_{OL}	OUTPUT LEVEL LVTTL Output L-Level Voltage (I_{OUT} = 2 mA)		–	0.4	–	0.4	–	0.4	V	

AC CHARACTERISTICS AND OPERATING CONDITIONS

(V_{DD} = 3.3 V ± 0.3 V, Ta = 0° ~ 70°C) (Notes 5, 6, 10)

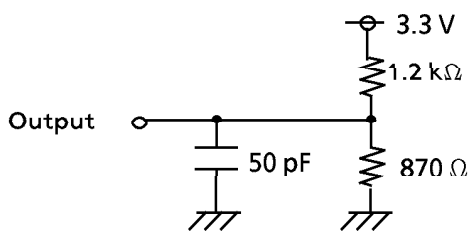
SYMBOL	PARAMETER		70 / 70L		75 / 75L		80 / 80L		UNIT	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Ref/Active-Ref/Active Command Period		56		65		68		ns	8
t_{RAS}	Active- Precharge Command Period		40	100000	45	100000	48	100000		
t_{RCD}	Active-Read/Write Command Delay Time		15		20		20			
t_{CCD}	Read/Write(a) -Read/Write(b) Command Period		1		1		1		cycles	
t_{RP}	Precharge-Active Command Period		15		20		20		ns	
t_{RRD}	Active(a)-Active(b) Command Period		15		15		20			
t_{WR}	Write Recovery Time	CL* = 2	7.5		10		10			
		CL* = 3	7		7.5		8			
t_{CK}	CLK Cycle Time	CL* = 2	7.5	1000	10	1000	10	1000		
		CL* = 3	7	1000	7.5	1000	8	1000		
t_{CH}	CLK High-Level Width		2.5		2.5		3			9
t_{CL}	CLK Low-Level Width		2.5		2.5		3			
t_{AC}	Access Time from CLK	CL* = 2		5.4		6		6		
		CL* = 3		5.4		5.4		6		
t_{OH}	Output Data Hold Time		3		3		3			
t_{HZ}	Output Data High-Impedance Time		3	7	3	7.5	3	8		7
t_{LZ}	Output Data Low-Impedance Time		0		0		0			
t_{SB}	Power-Down Mode Entry Time		0	7	0	7.5	0	8		
t_T	Transition Time of CLK (Rise and Fall)		0.5	10	0.5	10	0.5	10		
t_{DS}	Data-In Set-up Time		1.5		1.5		2			
t_{DH}	Data-In Hold Time		0.8		0.8		1			
t_{AS}	Address Set-up Time		1.5		1.5		2			
t_{AH}	Address Hold Time		0.8		0.8		1			
t_{CKS}	CKE Set-up Time		1.5		1.5		2			
t_{CKH}	CKE Hold Time		0.8		0.8		1			
t_{CMS}	Command Set-up Time		1.5		1.5		2			
t_{CMH}	Command Hold Time		0.8		0.8		1			
t_{REF}	Refresh Time			64		64		64	ms	
t_{RSC}	Mode Register Set Cycle Time		14		15		16		ns	8

* CL is $\overline{CAS}$ latency.

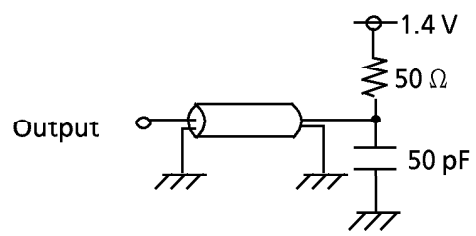
NOTES:

1. Conditions outside the limits listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltages are referenced to Vss.
3. These parameters depend on the cycle rate and their values are measured at the cycle rate obtained using the minimum values of t_{CK} and t_{RC}. Input signals are changed once during t_{CK}.
4. These parameters depend on the output loading. The specified values are obtained with the output open.
5. AC TEST CONDITIONS

Reference Level for Output Signals	1.4 V/1.4 V
Output Load	See the diagram for AC Test Load (B) below
Input Signal Levels	2.4 V/0.4 V
Transition Time (Rise and Fall) of Input Signals	2 ns
Reference Level of Input Signals	1.4 V



AC Test Load (A)



AC Test Load (B)

6. Transition times are measured between the V_{IH} and V_{IL} levels. The transition (rise and fall) of input signals has a fixed slope.
7. t_{HZ} defines the time at which the outputs go open-circuit and are not reference levels.
8. These parameters are specified for a given number of clock cycles and a given operating frequency. The celation-ship between the number of clock cycles, the timing value and the frequency (a clock period) is as follows:

   number of clock cycles = specified timing value / clock period

   (Fractions are rounded up to a whole number.)

9. t_{CH} is the pulse width of CLK measured from the positive edge to the negative edge and referenced to V_{IH} (min). t_{CL} is the pulse width of CLK measured from the negative edge to the positive edge and referenced to V_{IL} (max).
10. Power-up Sequence

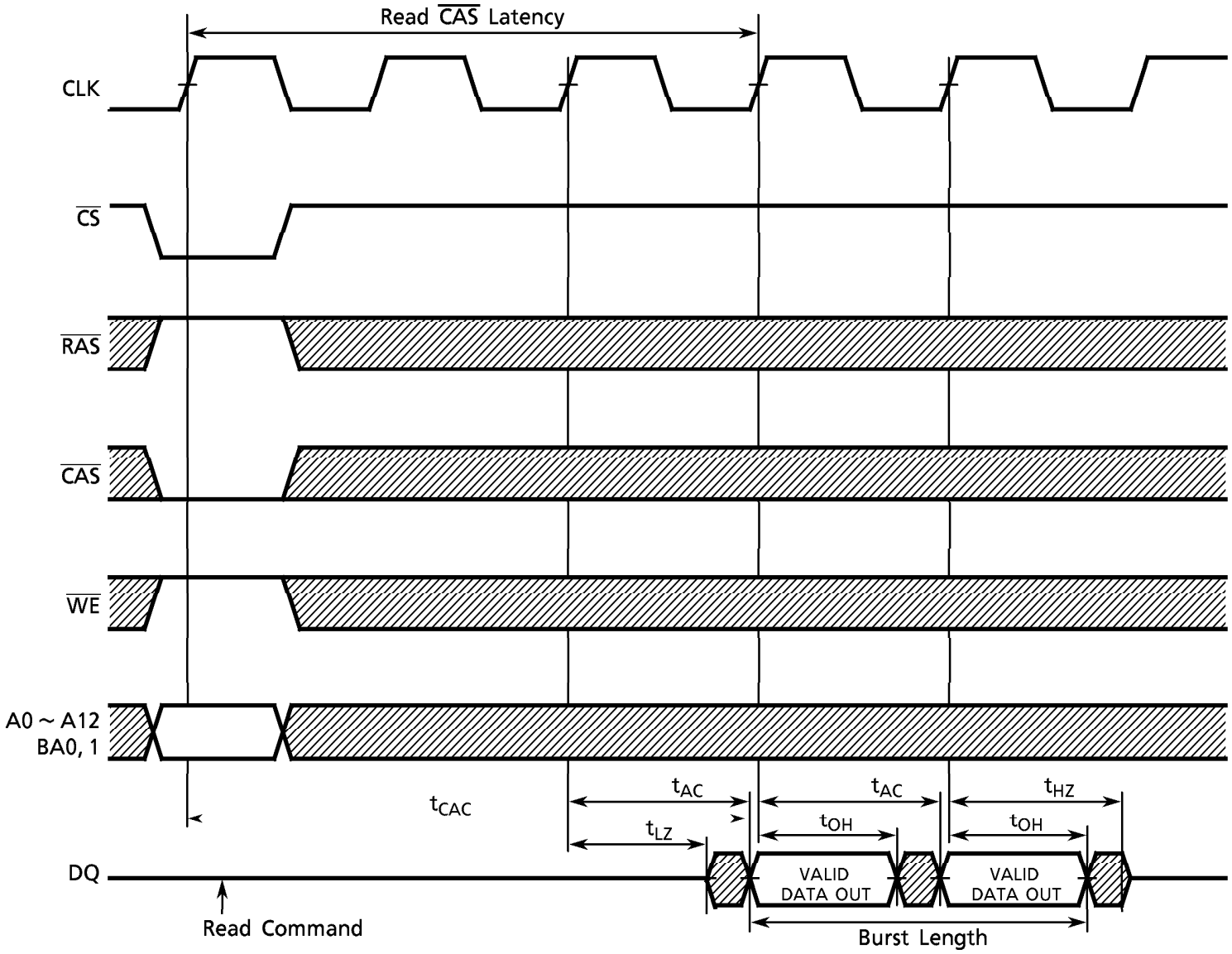
    Power-up must be performed in the following sequence.

    1) Power must be applied to V_{DD} and $V_{DD}Q$ (simultaneously) with all input signals held in the NOP state. The CLK signal must be started at the same time as power is applied.
    2) After power-up a pause of at least 200 μseconds is required. Then, DQMB and CKE must be held High (at the V_{CC} level) to ensure that the DQ output is High-impedance.
    3) Both banks must be precharged.
    4) The Mode Register Set command must be asserted to initialize the Mode register.
    5) An Auto-Refresh operation, consisting of at least eight Auto-Refresh cycles, must be performed.

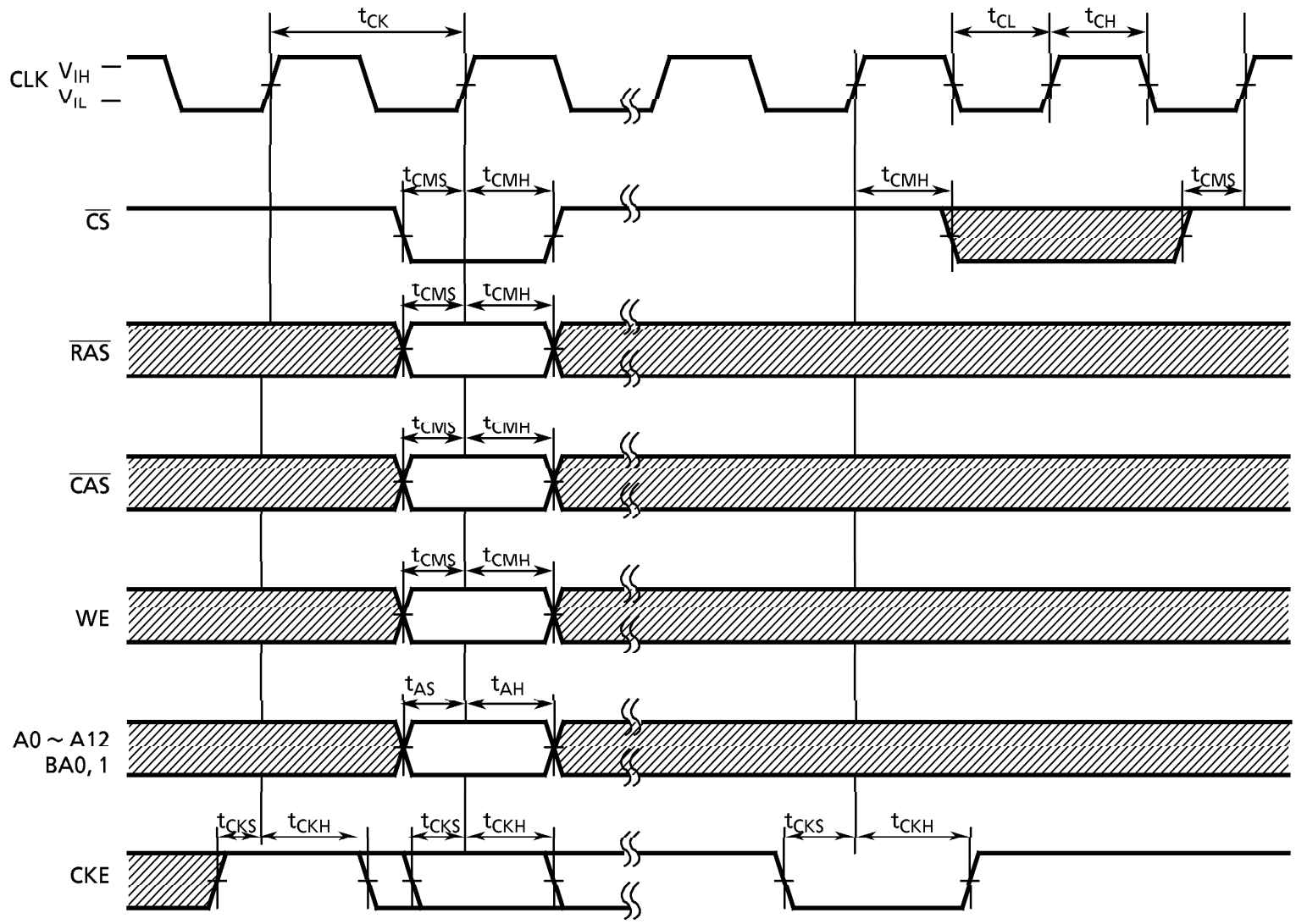
    The order in which 4) and 5) are performed is interchangeable.

TIMING DIAGRAMS

READ TIMING

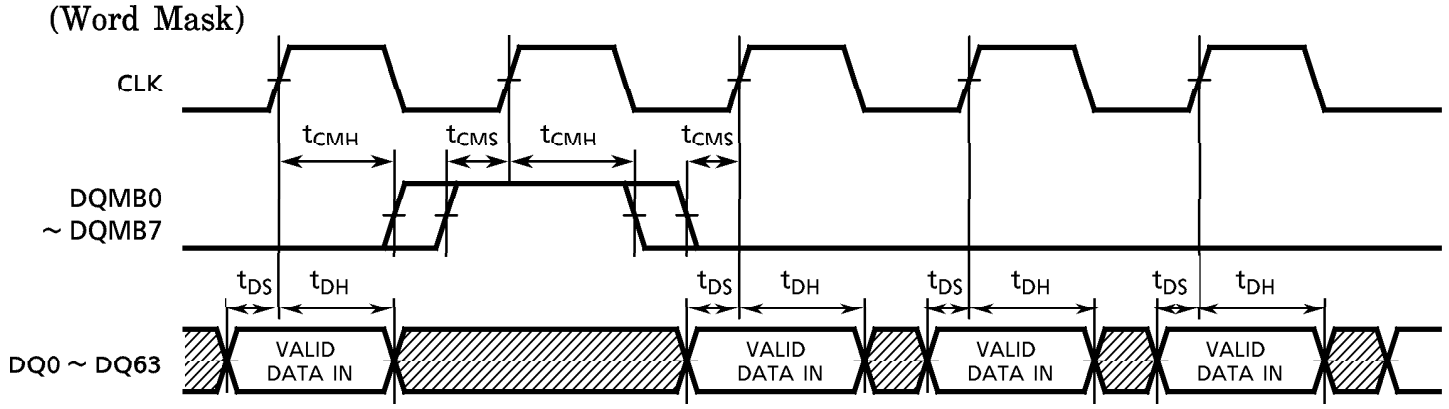


COMMAND INPUT TIMING

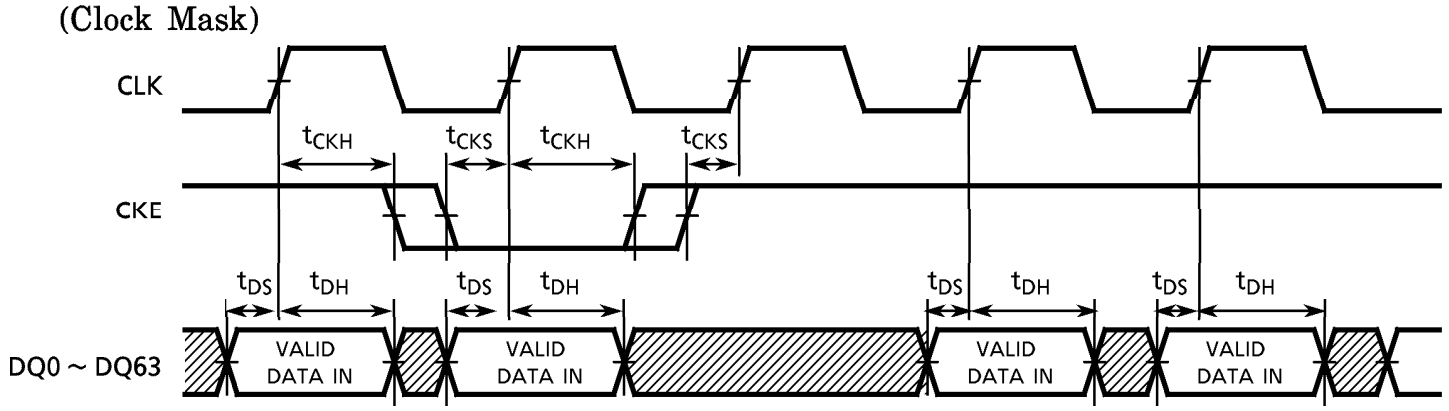


CONTROL TIMING FOR INPUT DATA

(Word Mask)

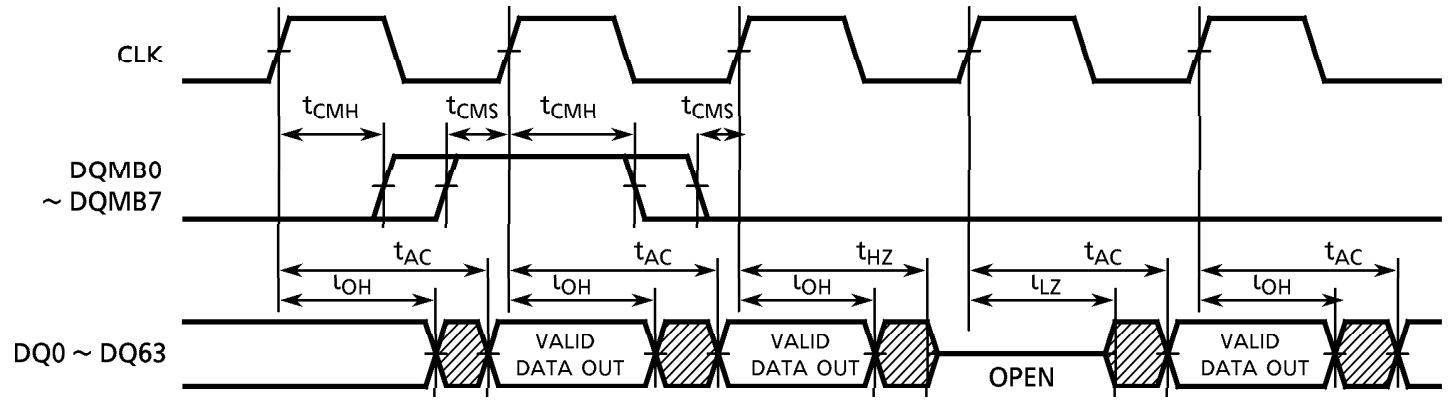


(Clock Mask)

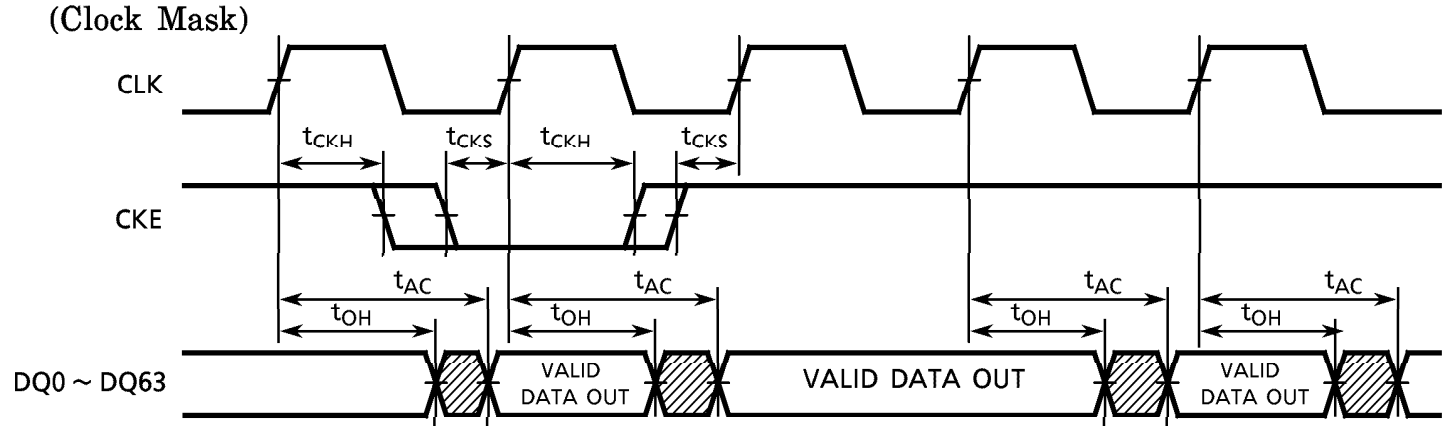


CONTROL TIMING FOR OUTPUT DATA

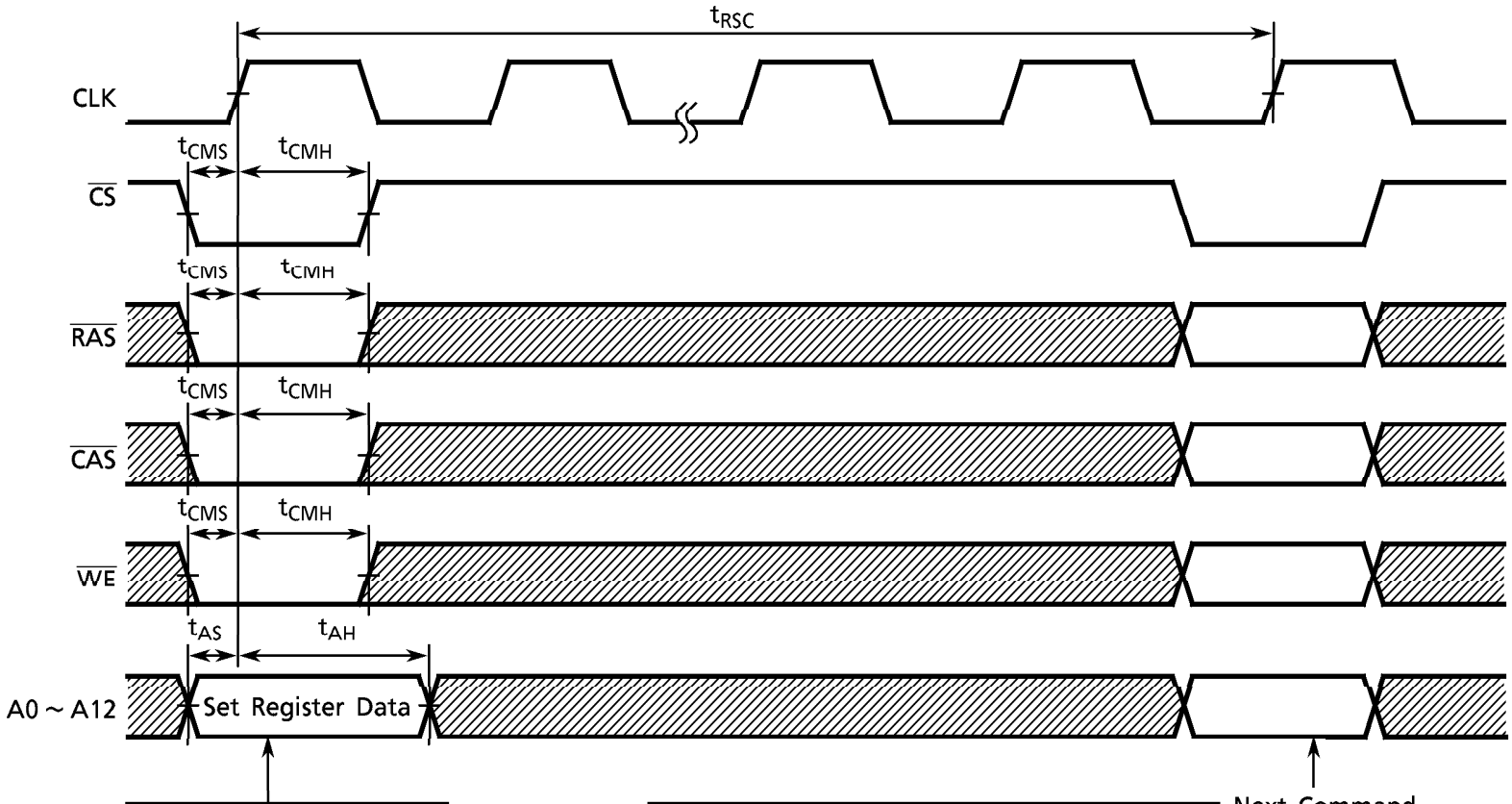
(Output Enable)



(Clock Mask)



MODE REGISTER SET CYCLE



A0	Burst Length	
A1		
A2		
A3	Addressing Mode	
A4	CAS Latency	
A5		
A6		
A7	0	(Test Mode)
A8	0	Reserved
A9	Write Mode	
A10	0	Reserved
A11	0	
A12	0	
BA0	0	
BA1	0	

			Burst Length	
A2	A1	A0	Sequential	Interleaved
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1	Full Page	

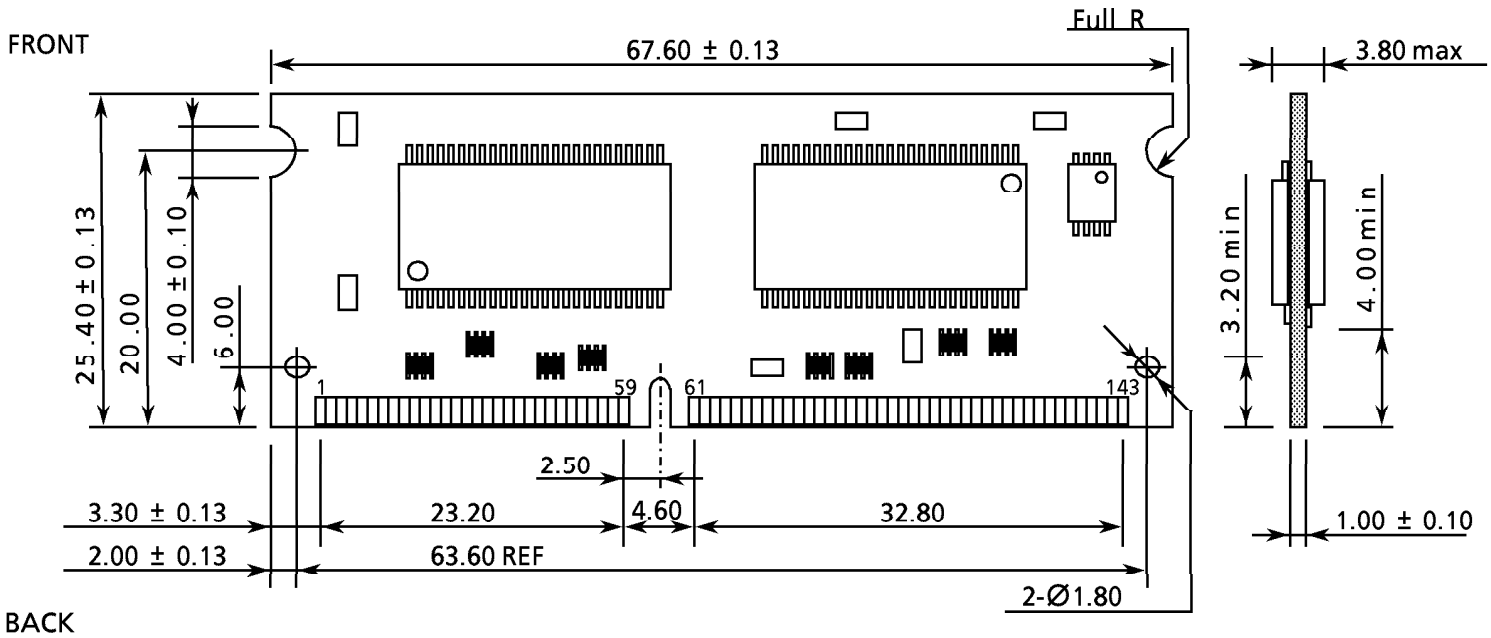
A3	Addressing Mode
0	Sequential
1	Interleaved

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	4

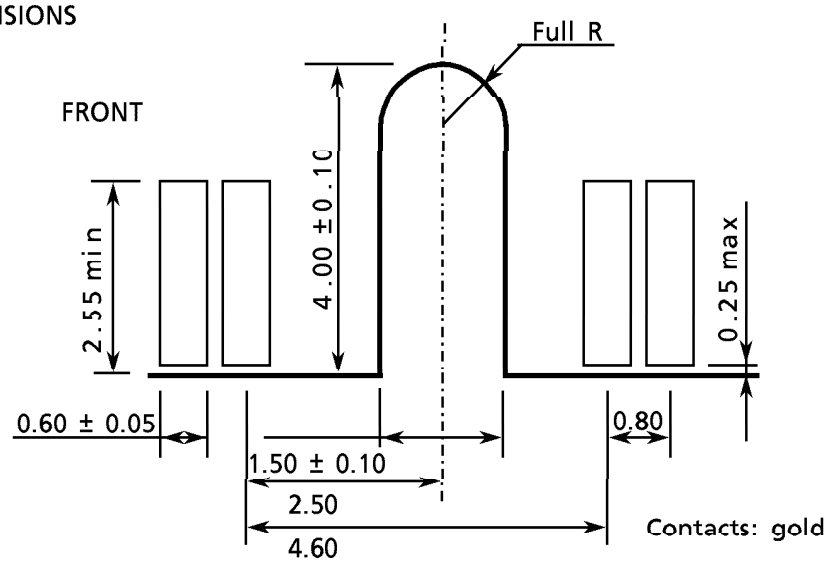
A9	Single Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

PACKAGE DIMENSIONS (THLY12N11C)

Unit: mm



CONTACT DIMENSIONS



Weight: 6.2g (typ.)