

Description

The NL84620R is a 256K bit Synchronous Content Addressable Memory (SyncCAM[®]-1R). The device performs high-speed parallel search operations on memory tables while simultaneously capturing and manipulating data from a data stream. Its primary application is as an address filter or an address translator for Fast Ethernet, Gigabit Ethernet, and ATM switches. The NL84620R has a streamlined instruction set and is a cost reduced version of the full-featured NL84620 device.

Features

- Match Flag times: 18/22 ns
- CAM Index output (pipeline mode): 10/12 ns
- Sustained searches of up to 40 Million/Second
- Separate 64-bit Comparand I/O bus, 32-bit Results bus and 14-bit Instruction bus
- Four 64-bit wide Mask Registers for easy masking of compare or write operations
- 14-bit instruction bus enables single cycle execution of all instructions
- Depth-expansion with no glue logic required
- 3.3V TTL compatible CMOS, 292-pin PBGA Package

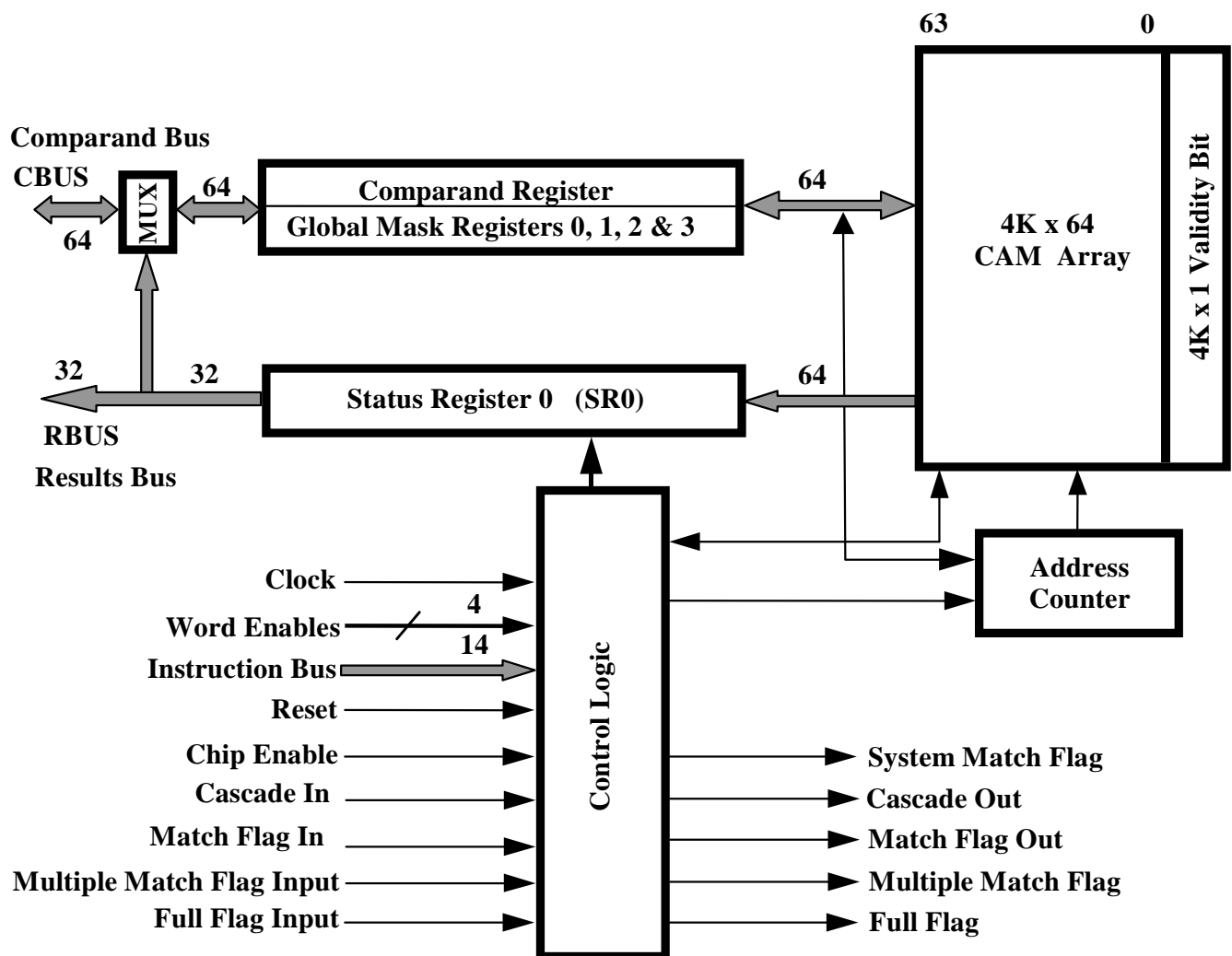


Figure 1 NL84620R Block Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	CBUS02	CBUS04	CBUS06	CBUS10	CBUS12	CBUS15	CBUS18	CBUS21	CBUS24	CBUS25	CBUS27	CBUS30	CBUS32	CBUS35	CBUS37	CBUS42	CBUS43	CBUS47	CBUS49	CBUS50	A
B	CBUS01	CBUS05	CBUS07	CBUS08	CBUS11	CBUS14	CBUS17	CBUS20	CBUS22	CBUS26	CBUS28	CBUS31	CBUS34	CBUS36	CBUS38	CBUS41	CBUS44	CBUS46	CBUS48	CBUS51	B
C	CBUS00	CBUS03	GND	CBUS09	CBUS13	VDD	CBUS16	CBUS19	CBUS23	VDD	CBUS29	CBUS33	CBUS39	VDD	CBUS40	CBUS45	GND	CBUS52	CBUS53	CBUS54	C
D	IBUS02	IBUS00	/RST	GND	GND	VDD	VDD	GND	GND	VDD	VDD	GND	GND	VDD	VDD	GND	GND	GND	CBUS55	CBUS56	D
E	IBUS04	IBUS03	IBUS01	GND													GND	CBUS58	CBUS57	CBUS59	E
F	IBUS07	IBUS06	IBUS05	VDD													VDD	VDD	CBUS60	CBUS61	F
G	IBUS09	IBUS08	VDD	VDD													VDD	(NC)	CBUS63	CBUS62	G
H	IBUS12	IBUS11	IBUS10	GND													GND	(NC)	(NC)	(NC)	H
J	/CE	CLK	IBUS13	GND													GND	(NC)	(NC)	(NC)	J
K	GND	/WEN2	/WEN3	VDD													VDD	VDD	(NC)	(NC)	K
L	/WEN1	/WEN0	VDD	VDD													VDD	(NC)	(NC)	(NC)	L
M	/FFI	/MMFI	VDD	GND													GND	(NC)	(NC)	(NC)	M
N	CSCUI	/MFDI	CSCDI	GND													GND	(NC)	(NC)	(NC)	N
P	(NC)	CSCUO	(NC)	VDD													VDD	VDD	(NC)	RBUS30	P
R	CSCDO	/MFD0	VDD	VDD													VDD	RBUS31	RBUS28	RBUS29	R
T	(NC)	/SMF	GND	GND													GND	RBUS26	RBUS25	RBUS27	T
U	/MMF	/FF	GND	GND	GND	VDD	VDD	GND	GND	VDD	VDD	GND	GND	VDD	VDD	GND	GND	GND	RBUS23	RBUS24	U
V	(NC)	(NC)	GND	(NC)	(NC)	VDD	(NC)	(NC)	(NC)	VDD	(NC)	RBUS01	RBUS07	VDD	RBUS08	RBUS13	GND	RBUS20	RBUS21	RBUS22	V
W	(NC)	(NC)	(NC)	(NC)	(NC)	(NC)	(NC)	(NC)	(NC)	(NC)	(NC)	(NC)	RBUS02	RBUS04	RBUS06	RBUS09	RBUS12	RBUS14	RBUS16	RBUS19	W
Y	(NC)	(NC)	(NC)	(NC)	(NC)	(NC)	(NC)	(NC)	(NC)	(NC)	(NC)	(NC)	RBUS00	RBUS03	RBUS05	RBUS10	RBUS11	RBUS15	RBUS17	RBUS18	Y

Figure 2 NL82721 Ball Assignment (292 PBGA, Top View)

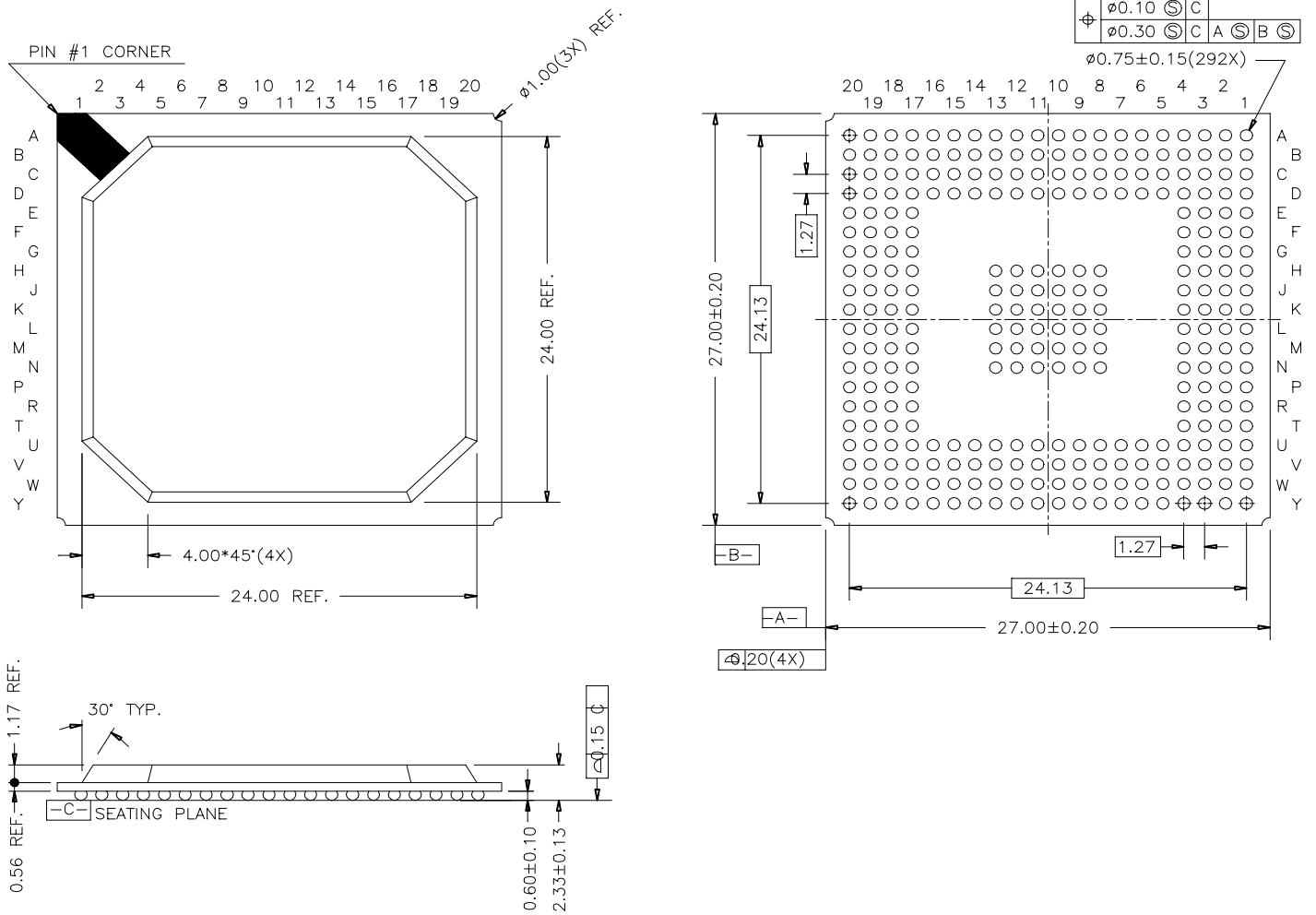


Figure 3: 292 PBGA Package Dimensions

1.0 Functional Description

The NL84620R is a Synchronous Content Addressable Memory (SyncCAM-1R) designed for use as an address filter or an address translator in 100/1000 Mb/s Ethernet and ATM switches and routers. This device can also be used to implement fast routing tables in Internet Protocol (IP) switches. The NL84620R has a total associative memory capacity of 256K bits organized as 4K x 64 bits.

A bi-directional 64-bit Comparand Bus (CBUS) enables all internal registers and memory to be accessed. An output only, 32-bit Results Bus (RBUS) provides status information after a compare operation. A 14-bit Instruction Bus (IBUS) allows instructions to be presented to the device once every cycle. All operations on the device are timed synchronously with the rising edge of a free running clock. This architecture permits back to back compare cycles to be executed without any bus latencies.

The Comparand Register (CR) is a 64-bit register that enables one to write the comparand data (key) and compare it with the contents of memory. This is the only register that enables a user to store and compare data with memory.

The NL84620R has four Global Mask Registers (GMR3-GMR0) that can each be selected on an operation by operation basis for write or compare operations. For a write operation, when the bits in these registers are programmed with '1's, the corresponding bits in memory will be masked, i.e. will not be written into. For compare operations, the corresponding bits in the associative data word will be forced to a match.

The 16-bit Device Configuration Register (DCR) enables the user to configure the device operation. The RBUS of the SyncCAM-1R can operate in Pipeline Mode only. The Address Counter may be set to be incremented automatically during write and so on. See Table 3f for a complete list.

The Status Register SR holds status information after compare, read, write or copy operations.

A 12-bit Address Counter (ACR) supplies the address to the memory array. This counter may be loaded with any valid start address and can be configured to increment once every cycle for read or write operations. This allows data to be loaded into or read out of the memory continuously.

Four Word Enable (/WEN3-/WEN0) inputs allow access to the internal registers and memory on 16-bit boundaries. These inputs also allow for bus matching on the CBUS bus with no glue logic.

The NL84620R can be clocked up to frequencies of 40MHz with a free running clock. A Chip Enable (/CE) input allows the device to be selected or deselected similar to any memory device. The device has flag inputs and outputs that enable depth cascading with no glue logic.

2.0 Pin Description

2.1 Clock (CLK):

This is a free running clock that is used to time all transactions on the CAM. The rising edge of the clock is the timing reference.

2.2 Chip Enable (/CE):

This is a synchronous input that selects the device for all operations, when asserted Low. When asserted High, the device is deselected and is in idle mode. In idle mode, the CBUS and the RBUS are high-Z. For single device operation, when the device is deselected (/CE asserted High) the Match, Multiple Match and System Match Flags are High and Full Flag is Low. For depth cascaded devices, the deselected devices will pass the flag input states through to the flag outputs. See Table 1.

2.3 Reset (/RST):

This is an asynchronous input and provides the hardware reset for the device. During initialization, this pin must be asserted low for a minimum of *three (3) cycles*. This will set all CAM words to empty, initialize the control logic, and clear all registers. The reset operation must be followed by at least one NOP instruction. Table 2 and Tables 3a-3d illustrate the state of the part after reset.

2.4 Full Flag Input (/FFI):

This input is provided for depth cascading multiple CAMs. When asserted low, this pin will allow data to be written into the CAM at the next free address (NFA) using the "Write to memory at NFA" instruction provided the device is not full. However, write to memory at address specified by the address counter is not affected by full flag input or output. For single device operation, the /FFI pin is tied to ground. For depth cascaded devices, the highest priority device has its /FFI input tied to ground, all other devices in the cascade having the /FFI tied to the Full Flag output (/FF) of the next higher priority device. Refer to the depth cascading section for more details.

2.5 Match Flag Down Input (/MFDI):

This input is provided for depth cascading multiple CAMs. For single device operation, this pin is tied to VDD. For depth cascaded devices, the highest Priority device has its /MFDI pin connected to VDD. All other devices in the cascade have their /MFDI pin tied to the Match Flag Down Output (/MFDO) of the next higher priority device. Refer to the depth cascading section for more details.

2.6 Multiple Match Flag Input (/MMFI):

This input is provided for depth cascading multiple CAMs. For single device operation, this pin is tied to VDD. For depth cascaded devices the highest priority device has its /MMFI tied to VDD. All other devices in the cascade have their /MMFI pin tied to the Multiple Match Flag (/MMF) of the next higher Priority device. Refer to the depth cascading section for more details.

2.7 Cascade Down Input (CSCDI):

This input is provided for depth cascading multiple CAMs. For single device operation, this pin is tied to ground. For depth cascaded devices the highest priority device has its CSCDI connected to ground. All other devices in the cascade have their CSCDI pin tied to the CSCDO of the next higher priority device. Refer to the depth cascading section for more details.

2.8 Cascade Up Input (CSCUI):

This input is provided for depth cascading multiple CAMs. For single device operation, this pin is tied to ground. For depth cascaded devices the lowest Priority device has its CSCUI connected to ground. All other devices in the cascade have their CSCUI pin tied to the CSCUO of the next lower priority device. Refer to the depth cascading section for more details.

2.9 Word Enable (/WEN_0,1,2,3):

This is a synchronous input and enables access to the CAM array and all the registers with 16-bit granularity. For 64-bit entities in the CAM, /WEN_3 enables access to bits 63-48, /WEN_2 to bits 47-32, /WEN_1 to bits 31-16 and /WEN_0 to bits 15-0. These control pins are effective only for read and write to memory and the registers; for all other operations they are a “don’t care”.

2.10 Instruction Bus (IBUS[13:0]):

This is a synchronous 14-bit bus that provides the operation code (Opcode) to the CAM. All instructions are executed in a single cycle.

2.11 Comparand Bus (CBUS[63:0]):

This is a 64-bit synchronous I/O bus that conveys data to and from the memory and the registers.

2.12 Cascade Down Output (CSCDO):

This output is provided for depth cascading multiple CAMs. For single device operation this pin must be left unconnected. For depth cascaded devices, the highest priority device has its CSCDO connected to the CSCDI of the next lower priority device. Refer to the depth expansion section for more details.

2.13 Full Flag (/FF):

This is a synchronous output and is updated after Write to Memory, Copy to Memory, set VBIT or Set Full Flag operations. After reset, this pin is high. When the device is full, /FF is asserted low. For depth cascaded devices, /FF is connected to /FFI of the next lower priority device. For depth cascaded devices, when single device mode is selected, deselected devices pass /FFI through to /FF.

2.14 Match Flag Down Output (/MFDO):

This synchronous output is provided for depth cascading CAMs. This output is updated for all compare operations. After reset, /MFDO is high. For depth cascaded devices, the /MFDO of a device is connected to the /MFDI of the next lower priority device. For depth cascaded devices, when single device mode is selected, deselected devices pass /MFDI through to /MFDO.

2.15 System Match Flag (/SMF):

This synchronous output provides the System Match Flag (either for single device or cascaded devices). This output is updated for all compare operations. After reset /SMF is high. Functionally this output is identical to /MFDO. When cascading, the /SMF is provided by the lowest priority CAM. The /SMF from all other CAMs in the cascade may be left unconnected.

2.16 Multiple Match Flag (/MMF):

This synchronous output provides the Multiple Match Flag (either for single device or cascaded devices). This output is updated for all compare operations. After reset /MMF is high. In depth cascaded systems the lowest priority device provides the /MMF. For cascaded devices, when single device mode is selected, the deselected devices pass /MMFI through to /MMF.

2.17 Results Bus (RBUS[31:0]):

This is a 32-bit synchronous bus (RBUS) that outputs the results of a compare operation. During a compare operation, when there is no match, RBUS is High-Z. For a compare operation, when there is a match, this bus outputs the CAM index of the Highest Priority Match (HPM), the Device ID, and the status of the flags.

The CAM index of HPM will be output on RBUS[31] through RBUS[20]. The lower 12 bits of Device ID are output on RBUS[19] through RBUS[8]. Bits RBUS[7] through RBUS[5] are reserved and will read '0'. RBUS[4] is the match flag status and will reflect the state of the external /MF pin. RBUS[3] is the multiple match flag status and will reflect the external /MMF pin. RBUS[2] is the full flag status and will reflect the state of the external /FF pin. RBUS[1] is reserved and will read '0'. RBUS[0] will reflect the state of the validity bit, '0' for Valid or '1' for empty, when a compare operation is issued referencing the validity bit.

The SyncCAM-1R operates in **pipeline mode** only. In pipeline mode, the results of a compare instruction are output on RBUS in the following cycle.

The user must set bit b7 to '1' in the Device Configuration Registers of each CAM device in the module to setup the RBUS to be in pipeline mode. **The default setting of this internal register after a hardware or software reset is '0'.** Refer to Table 3c for more details.

3.0 SyncCAM-1R Internal Registers

3.1 Status Register (SR0)

The 4K x 64 SyncCAM-1R device has one Status Register labeled SR0. This register holds the results of Compare, Read, Write or Copy operations. The RBUS outputs results after a comparison in either SR0 format. The user can also access the Status Registers from the CBUS by executing a “read status register” instruction. Table 3b describes the contents of these registers after reset. Table 3g describes the contents of this register after all other operations.

3.2 Comparand Register (CR)

The Comparand Register (CR) is a 64-bit register for loading the comparand (key) data into the device for compare and other operations. For bus widths of 16 or 32 bits, the Word Enable (/WEN3-/WEN0) inputs enable the user to load data into the CR and then compare its contents with the contents of memory. This feature enables the SyncCAM-1R to interface to buses that are 16, 32 and 64-bit wide seamlessly. This is the only register that enables the user to store and compare data with memory.

3.3 Global Mask Registers (GMR)

There are four 64-bit Global Mask Registers (GMR) that may be used either to mask compares or to mask data during memory writes. Each GMR may be selected on a cycle by cycle basis by specifying the GMR address in the instruction.

For compare instructions calling for a masked compare, if a mask bit is ‘1’, the corresponding bits in the memory will not enter the compare operation and behave as if a match occurred for that particular bit. If a mask bit is ‘0’, the

corresponding bits in the memory will enter the compare operation.

For memory write instructions calling for a masked write, if a mask bit is ‘1’, the corresponding bits in the memory will not be altered. If a mask bit is ‘0’, the corresponding bits in the memory will be written to.

3.4 Highest Priority Match Index Register (HPMR)

This register holds the address of the highest priority match. This register is updated after all compare operations. See table 3a.

3.5 Next Free Address Register (NFAR)

This register holds the address of next free address in the array. This is updated for all write to memory, copy to memory, and set VBIT instructions. See table 3a and the Next Free Address Register Section.

3.6 Device Configuration Register (DCR)

This register holds the programmable bits for selecting modes of operation of the CAM device. This register includes a field (read only) indicating the type of device. If the user wants the address counter to be incremented during read and write operations, bit b4 must be set to “1”. Bit b7 must be set to a “1” for proper operation. See table 3c for more details.

3.7 Device ID Register (DIDR)

This register holds the Device ID value. This register is written into as part of initialization sequence. This register is reset only during hardware reset. Software reset instruction does not alter this register. See table 3e.

Table 1: Logical State of the Outputs with /CE high

Output	Pin/Bus Name	Logical State
Comparand Bus	CBUS	High-Z
Results bus	RBUS	High-Z
Match Flag Down Output	/MFDO	Same as Match Flag Down Input (/MFDI)
System Match Flag	/SMF	Same as Match Flag Down Input (/MFDI)
Multiple Match Flag	/MMF	Same as Multiple Match Flag Input (/MMFI)
Full Flag	/FF	Same as Full Flag Input (/FFI).

Table 2: Logical State of the Outputs after Hardware or Software Reset

Output	Pin/Bus Name	Logical State
Comparand Bus	CBUS	High-Z
Results Bus	RBUS	High-Z
Match Flag Down Output	/MFDO	High
System Match Flag	/SMF	High
Multiple Match Flag	/MMF	High
Full Flag	/FF	High

Table 3a: Address Counter, NFAR, and HPM Registers after Hardware or Software Reset

b11	b10	b9	b8	b7	b6	B5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	0	0	0	0	0

Table 3b: Status Register 0 (SR0) after Hardware or Software Reset

b63	b52	b51	b40	b39	b37	b36	b35	b34	b33	b32
CAM Address	Device ID ^a	RSV	/MF	/MMF	/FF	RSV	VBIT			
0 0 0 Hex	0 0 0 Hex	000	1	1	1	0	1			

a) Only the lower 12-bits of the Device ID Register will appear. The Device ID Field is unchanged after software reset.

Table 3c: Device Configuration Register (DCR) after Hardware or Software Reset

b15	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
CAM Type ^b	RSV	Mode ^c	RSV	RSV	ACNT	RSV	RSV	RSV	RSV	RSV
000 0000	0	0	0	0	0	0	0	0	0	0

b) 000 0000 indicates a 4K x 64 SyncCAM-1R. This entry is read only.

c) Bit b7 must be set to 1 after hardware or software reset for proper SyncCAM-1R operation. This enables pipeline mode.

Table 3d State of the SyncCAM-1R after Hardware or Software Reset

#	Memory, Registers and Outputs	Status after Hardware Reset	Status after Software Reset
1	Device ID Register	All bits reset to '0'	Remains unchanged
2	Address Counter	All bits reset to '0'	All bits reset to '0'
3	Next Free Address Register	All bits reset to '0'	All bits reset to '0'
4	Global Mask Registers	All bits reset to '0'	All bits reset to '0'
5	Status Register	See table 3b	See table 3b
6	Device Configuration Register	See table 3c	See table 3c
7	Memory ^d	Undefined	Undefined
8	VBIT in Memory	Empty=1	Empty=1
9	Full Flag (/FF)	Reset to '1'	Reset to '1'
10	Comparand Bus (CBUS)	High-Z	High-Z
11	Results Bus (RBUS)	High-Z	High-Z
12	Match Flag Down Output (/MFDO)	High	High
13	System Match Flag (/SMF)	High	High
14	Multiple Match Flag (/MMF)	High	High
15	Cascade Down Output (CSCDO)	High	High

d) Memory indicates CAM Words and Local Mask Words

Table 3e: CBUS State under Operating Mode and Control Inputs

Control Inputs State	Comparand Bus (CBUS) State
Reset (/RST) = Low	High-Z
Chip Enable (/CE) = High	High-Z
Chip Enable (/CE) = Low	/WEN_X that are '0' enable corresponding 16-bits; others are High-Z
Global Device Mode Operation, /RST='1', /CE='0'	
Highest Priority Device (/MFDI='1' & /MFDO='0')	/WEN_X that are '0' enable corresponding 16-bits; others are High-Z
Device with Next Free Address (/FFI='0' & /FF='1')	/WEN_X that are '0' enable corresponding 16-bits; others are High-Z
All Other Devices	High-Z
Single Device Mode Operation, /RST='1', /CE='0'	
Selected Device (Device with Matching Device ID)	/WEN_X that are '0' enable corresponding 16-bits; others are High-Z
All Other Devices	High-Z

Table 3f: Device Configuration Register Format

b15	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
CAM Type	RSV	Mode	RSV	RSV	ACNT	RSV	RSV	RSV	RSV	RSV

Notes:

- b15-b9** CAM Type field. Reads "000 0000" for 4K x 64 SyncCAM-1R. This CAM Type field is read only.
- b8** Reserved. Will read '0'.
- b7** This bit must be set to '1' for proper SyncCAM-1R operation; the RBUS operates in **pipeline mode**. This bit is set to '0' after reset. (Hardware or Software)
- b6-b5** Reserved. Will read '0'.
- b4** When set to '1' this bit enables the **Address counter** to be **incremented**. When set to '0' it disables the address counter incrementing. This bit is set to '0' after reset. (Hardware or Software)
- b3-b0** Reserved. Will read '0'.

Table 3g: Status Register (SR0) Format

b63	b52	b51	b40	b39	b37	b36	b35	b34	b33	b32
CAM Address	Device ID			RSV		/MF	/MMF	/FF	RSV	V-bit

Notes:

- b63-b52** CAM Index field. Updated after all compare instructions. Updated with Highest Priority Match (HPM) index when there is a match.
- b51-b40** Lower 12 bits of the 16-bit Device ID. Updated when Device ID is written.
- b39-b37** Reserved; will read '000'.
- b36** Match flag. Updated after all compare operations; reflects the internal match flag status.
- b35** Multiple match flag. Updated after all compare operations; reflects the internal multiple match flag status.
- b34** Full flag. Updated after write to memory, copy to memory, set VBIT instructions; reflects internal full flag status.
- b33** Reserved. Will read '0'.
- b32** VBIT(valid or empty). Updated after all compare operations with the type of words compared; updated with the settings of VBIT after write to memory or copy to memory; updated with VBIT after set VBIT operation.

4.0 CAM Address Counter (ACR)

The CAM Address Counter (ACR) in the SyncCAM-1R allows a user to perform read, write or copy operations continuously. The user may set the start address in the counter and program the Device Configuration Register to increment the counter after write, read or copy operations. The ACR is set to increment by setting bit b4 in the Device Configuration Register to a '1'. When the counter is set **not to increment**, (bit b4='0'), then the counter address will not increment even for instructions that specify that the Address Counter be incremented.

When the CAM Address Counter is **set to increment** in the Device Configuration Register, the counter will be incremented after any of the following instructions are executed:

1. Copy operations to and from memory that reference the address counter.
2. Set VBIT to Valid or Empty at the address indicated by the Address Counter.
3. Write to memory and set VBIT to Valid or Empty at the address indicated by the Address Counter.
4. Write to memory masked by Global Mask Register, set VBIT to Valid or Empty at the address indicated by the Address Counter.
5. Read memory at address indicated by the Address Counter and increment Address Counter.

The following memory operations that reference the Address Counter **do not increment** the Address Counter even if b4 in the Configuration Register is set to '1' (Increment):

1. Write to memory, no change to VBIT.
2. Read memory.
3. Read memory (CAM Word).

These restrictions should be kept in mind when interfacing SyncCAM-1R to buses smaller than 64-bits wide.

5.0 Next Free Address Register (NFAR)

The Next Free Address Register (NFAR) holds the address of the memory word that has its VBIT set to empty, and that is numerically closest to zero. This address is generated from the output of the priority encoder in the SyncCAM-1R. When the device has no empty locations the NFAR holds the address of the last empty location.

The following operations will update the NFAR:

1. Write to Memory at NFAR; set VBIT to Valid.
2. Set VBIT to empty at the Address indicated by the Address Counter.
3. Set VBIT to empty at HPM address.
4. Set VBIT to empty at all matching locations.
5. Copy operations that reference the NFAR.

The NFAR will **not be updated** for the following operation:

1. Write to memory at next free address; no change to VBIT.

These restrictions should be kept in mind when interfacing SyncCAM-1R to buses smaller than 64-bits wide or when updating memory in segments smaller than 64-bits wide.

6.0 Validity Bit

Every location in the memory array has a corresponding Validity bit associated with it. This bit is referred to as the VBIT.

When the Empty bit is set to reflect the Valid state for a particular word, then that particular word will take part in Compare operations only when the compare operation with VBIT set to valid instruction is executed.

8.0 Initializing the SyncCAM-1R

The SyncCAM-1R needs to be initialized after power up for proper operation. The following steps show how to initialize the SyncCAM-1R for single device and for depth cascaded devices. Please refer to section 8 for details on depth cascading.

8.1 Single Device Initialization

1. Assert /RST pin low for a minimum of three cycles.
2. Execute NOP instruction (at least once).
3. Write to Device ID Register (any 16-bit value).
4. Select Single device mode (Device ID input on CBUS[15:0]).
5. Write to Device Configuration register and set bit b7 = '1'.

The SyncCAM-1R device is now ready for memory write, compare and other operations.

8.2 Depth Cascaded Devices Initialization

1. Assert /RST pin low for a minimum of three cycles.
 2. Execute NOP instruction (at least once).
 3. Write to Device ID Register (any 16-bit value).
 4. Set Full Flag.
 5. Write to Device ID Register (any 16-bit value).
- (Repeat 4 & 5 until all devices have ID written).
6. Execute a software Reset.
 7. Execute NOP instruction (at least once).
 8. Write to Device Configuration Register and set bit b7 = '1'.

The device IDs must all be unique for proper operation. At step 3, the first device has the ID written; at step 5, the second device has the ID written and so on. The SyncCAM-1R device is now ready for memory write, compare and other operations.

9.0 Writing to the CAM Array

After initialization, the user can write into the SyncCAM-1R array in many ways. Two common methods of accomplishing this are described below:

9.1 Writing to Memory: Option 1

One method of writing into the CAM array is to execute "Write to memory at next free address and set VBIT to Valid" instruction repeatedly until the memory is full or all data is written into the CAMs. The write operation begins in the device with /FFI = 0 and /FF=1, and continues until all locations have been written to (no EMPTY locations remain). When the last empty location has been written to, the /FF of that device will assert a '0' preventing any further "Write to memory at NFA" operations from occurring in that device. This will then enable the next lower priority device in the cascade to accept "Write to memory at NFA" operation. This continues until the last device in the chain becomes full and asserts /FF pin low, indicating that all the CAM devices are now full, and no empty locations remain.

9.2 Writing to the Memory: Option 2

Another method of writing to the CAM is to use the address from the internal address counter as opposed to the NFAR. The steps involved in this method are as follows:

1. Select Single Device Mode, with Device ID on the least significant bits of the CBUS.
2. Write to CAM word at address for ACNTR and set VBIT to valid.
3. User must either monitor the full flag for each individual device or keep an external count of the number of entries filled in each device and then enable the next CAM in a cascaded array.
4. Repeat steps 2 and 3 until all devices are full (/FF = 0 for single device or cascaded chain).
5. Select Global Device Mode.

10.0 Electrical Characteristics

10.1 Absolute Maximum Ratings^a

Supply voltage to GND	-0.5 to +4.6V
DC output voltage (Vout)	-0.5 to VDD + 0.5V ^b
DC output current	50mA ^c
T _{BIAS} Temperature under bias	-40°C to +85°C
T _{STG} Storage temperature	-65°C to +150°C

- a) Stresses greater than ABSOLUTE MAXIMUM RATINGS will cause permanent damage to the device, resulting in functional or reliability type failures.
- b) -2.0V for 10 ns, measured at the 50% point.
- c) Per output, one at a time, one-second duration

10.2 Power Supply Characteristics

Symbol	Parameter	Test Conditions	40 MHz	33 MHz	Unit
			Max.	Max.	
I _{DDO}	Operating Current	t _{CYC} = t _{CYC} (min)	700	650	mA
I _{SB}	Standby Current	/CE = '1'	90	90	mA

10.3 Capacitance

Symbol	Parameter	Max.	Unit	Notes
C _{IN}	Input Capacitance	6	pF	f=1MHz, V _{IN} =0V
C _{OUT}	Output Capacitance	8	pF	f=1MHz, V _{OUT} = 0V

10.4 DC Electrical Characteristics over Operating Range (T_A = 0°C - 70°C, VDD = 3.3V ± 5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{IH}	Input HIGH Voltage	Logic high for all Inputs	2.2	VDD + 0.5	V
V _{IL}	Input LOW Voltage	Logic low for all Inputs	-0.5	0.8	V
V _{OH}	Output HIGH Voltage	I _{OH} = -4mA, VDD = Min.	2.4	-	V
V _{OL}	Output LOW Voltage	I _{OL} = 4mA, VDD = Min.	-	0.4	V
I _{LI}	Input Leakage	VDD = 3.47V; GND ≤ V _{IN} ≤ VDD	-5	5	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ VDD	-10	10	μA

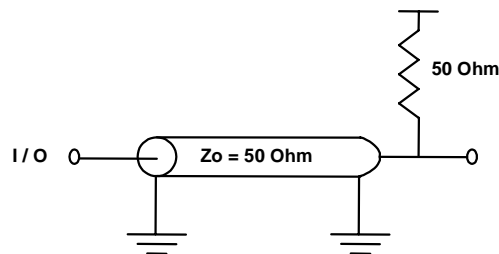


Figure 4 AC Test Conditions

11.0 AC Timing Parameters:

#	Parameter	Type	Description	40MHz		33 MHz	
				Min	Max	Min	Max
1	t _{CYC}	IN	Cycle	25		30	
2	t _{CYH}	IN	Cycle high	11.5		13.5	
3	t _{CYL}	IN	Cycle low	11.5		13.5	
4	t _{CSU}	IN	Chip Enable Set-up	4		5	
5	t _{CHD}	IN	Chip Enable Hold	0		0	
6	t _{WNSU}	IN	Word Enable Set-up	4		5	
7	t _{WNH}	IN	Word Enable Hold	0		0	
8	t _{DSU}	IN	Data Setup	4		5	
9	t _{DHD}	IN	Data Hold	0		0	
10	t _{INSU}	IN	Instruction Setup	4		5	
11	t _{INH}	IN	Instruction Hold	0		0	
12	t _{RB1}	OUT	RBUS Data Output (Pipeline Mode)		10		12
13	t _{RB2}	OUT	RBUS Data Output Hold (Pipeline Mode)	1		1	
14	t _{CDO}	I/O	CBUS Memory Data Output		22		25
15		I/O	CBUS Register Data Output		12		14
16	t _{CDH}	I/O	CBUS Data Output Hold	3.5		3.5	
17	t _{SMF}	OUT	System Match Flag Assertion and Deassertion	4	18	4	22
18	t _{MMF}	OUT	Multiple Match Flag Assertion and Deassertion	4	21	4	25
19	t _{FF1}	OUT	Full Flag Assertion and Deassertion (Write, Copy instructions)	2	23	2	26
20	t _{FF2}	OUT	Full Flag Assertion and Deassertion (VBC instructions)	2	30	2	34

1. **VDD = 3.3V +/- 5%, TA=0°C – 70°C, V_{IH}/V_{IL} = 3.0V/0V.**
2. **All timings are with reference to the rising edge of the clock. All timing numbers in nano seconds.**
3. **All timing numbers are for a single device (as opposed to devices in cascade).**
4. **Output hold times are guaranteed by design, but not tested in production.**

12.0 4K x 64 SyncCAM-1R Instruction Set

The SyncCAM-1R Instruction bus is 14-bits wide. It consists of a 11-bit “Opcode field” consisting of bits IBUS₁₃-IBUS₀₃ and a 1-bit global mask field “GMSK” consisting of IBUS₀₁.

Instruction Word (Opcode) Format:

IBUS ₁₃	IBUS ₁₂	IBUS ₁₁	IBUS ₁₀	IBUS ₀₉	IBUS ₀₈	IBUS ₀₇	IBUS ₀₆	IBUS ₀₅	IBUS ₀₄	IBUS ₀₃	IBUS ₀₂	IBUS ₀₁	IBUS ₀₀
Opcode Field											GMSK	0	

IBUS₁₃ – IBUS₀₃ Opcode field. This field determines all possible instructions.
 IBUS₀₂ – IBUS₀₁ Selects between the four Global Mask Registers.

#	IBUS ₀₂	IBUS ₀₁	Selects Global Mask Register
1	0	0	0
2	0	1	1
3	1	0	2
4	1	1	3

Instruction: [Opcode field] [y1y0] [z0]
 xxx xxxx xxxx GMSK 0
[Opcode field] Bits 13 - 3, coded as [w2 w1 w0]; w2 is bits 13-11; w1 is bits 10 – 7; w0 is bits 6 - 3
[GMSK] Bits 2 - 1, coded as y1y0
[0] Bit 0, coded as z0

13.0 SyncCAM-1R Instruction Opcodes and Description

13.1 Compare Instructions

#	Opcode in Hex	Instructions Explanation
	[Opcode] [GMSK] [CDS] [w2w1w0] [y1y0] [z0]	
1	[610] [0] [0] H	Compare Valid Entries
2	[614] [y1y0] [0] H	Compare Valid Entries using Global Mask Register
3	[620] [0] [0] H	Write to Comparand Register and Compare Valid Entries
4	[624] [y1y0] [0] H	Write to Comparand Register and Compare Valid Entries using Global Mask Register

13.2 Write Instructions

1	[000] [0] [0] H	NOP (No Operation)
2	[001] [0] [0] H	Write to Comparand
3	[002] [y1y0] [0] H	Write to Global Mask Register
4	[003] [0] [0] H	Write to Memory, No Change to VBIT
5	[004] [0] [0] H	Write to Memory, Set VBIT to Valid
6	[007] [y1y0] [0] H	Write to Memory masked by Global Mask Registers no Change to VBIT
7	[008] [y1y0] [0] H	Write to Memory masked by Global Mask Registers Set VBIT to Valid
8	[00C] [0] [0] H	Write to Memory at HPM address, Set VBIT to Valid
9	[013] [0] [0] H	Write to Memory at NFA, No change to VBIT
10	[014] [0] [0] H	Write to Memory at NFA, Set VBIT to Valid
11	[01B] [0] [0] H	Set VBIT to Valid at Address Counter
12	[01C] [0] [0] H	Set VBIT to Empty at Address Counter
13	[020] [0] [0] H	Set VBIT to Empty, at HPM address
14	[024] [0] [0] H	Set VBIT to Empty at all matching address

- All write operations are controlled by the four Word Enables.
- Instructions 11 to 14 are "VBC" instructions.

13.3 Copy Instructions

Opcode in Hex		Instructions Explanation
#	[Opcode][GMSK][CDS] [w2 w1 w0][y1 y0][z0]	
1	[02F] [0] [0] H	Copy Comparand Register to memory at NFA, Set VBIT to Valid

- Copy instruction is a 128-bit wide operation.

13.4 Special Instructions

1	[047] [0] [0] H	Write to Device Configuration Register
2	[048] [0] [0] H	Write to Device ID Register ^a
3	[04B] [0] [0] H	Set Full Flag ^a
4	[04C] [0] [0] H	Select Single Device Mode
5	[04D] [0] [0] H	Select Global Mode
6	[04E] [0] [0] H	Software Reset ^b
7	[04F] [0] [0] H	Write Address Counter

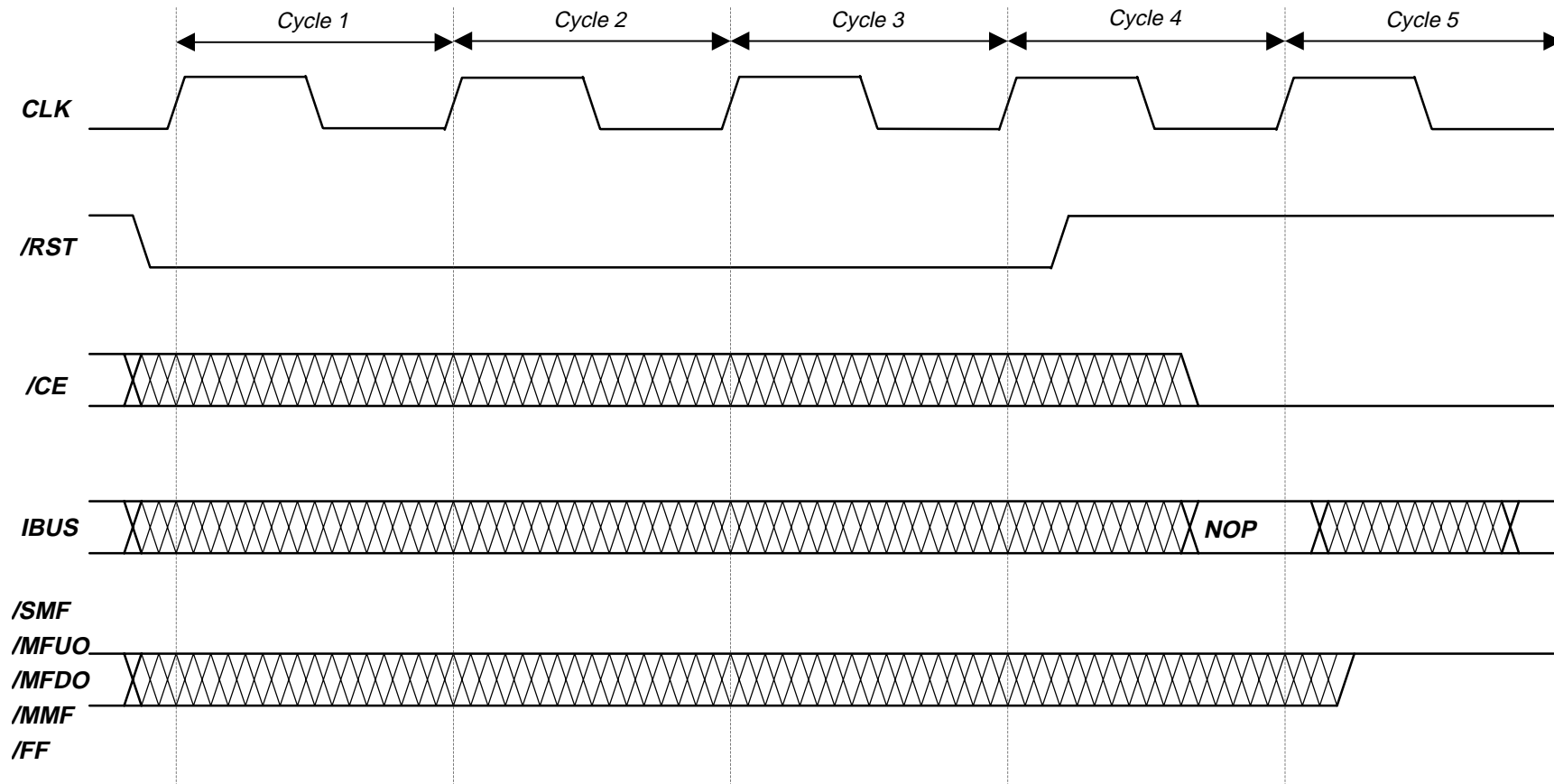
- a) This instruction will be executed in the device with /FI = 0 and /FF = 1. All other devices will treat this as NOP.
b) A Software instruction must be followed by a NOP instruction.

13.5 Read Operations

1	[200] [0] [0] H	Read Address Counter (Address output on CBUS [15:0])
2	[201] [0] [0] H	Read Memory at address
3	[202] [0] [0] H	Read Memory at address and Increment Counter
4	[203] [0] [0] H	Read Status Register (Data output on CBUS [63:32]), refer to Table 3g for details
5	[204] [y1y0] [0] H	Read Global Mask Register
6	[205] [0] [0] H	Read Comparand Register
7	[206] [0] [0] H	Read Next Free Address Register (Device ID output on CBUS [31:16] and NFA on CBUS [15:0])
8	[207] [0] [0] H	Read Memory at HPM Address
9	[209] [0] [0] H	Read Device Configuration Register (Data output on CBUS [15:0])
10	[20A] [0] [0] H	Read Device ID Register (Device ID output on CBUS [31:16])

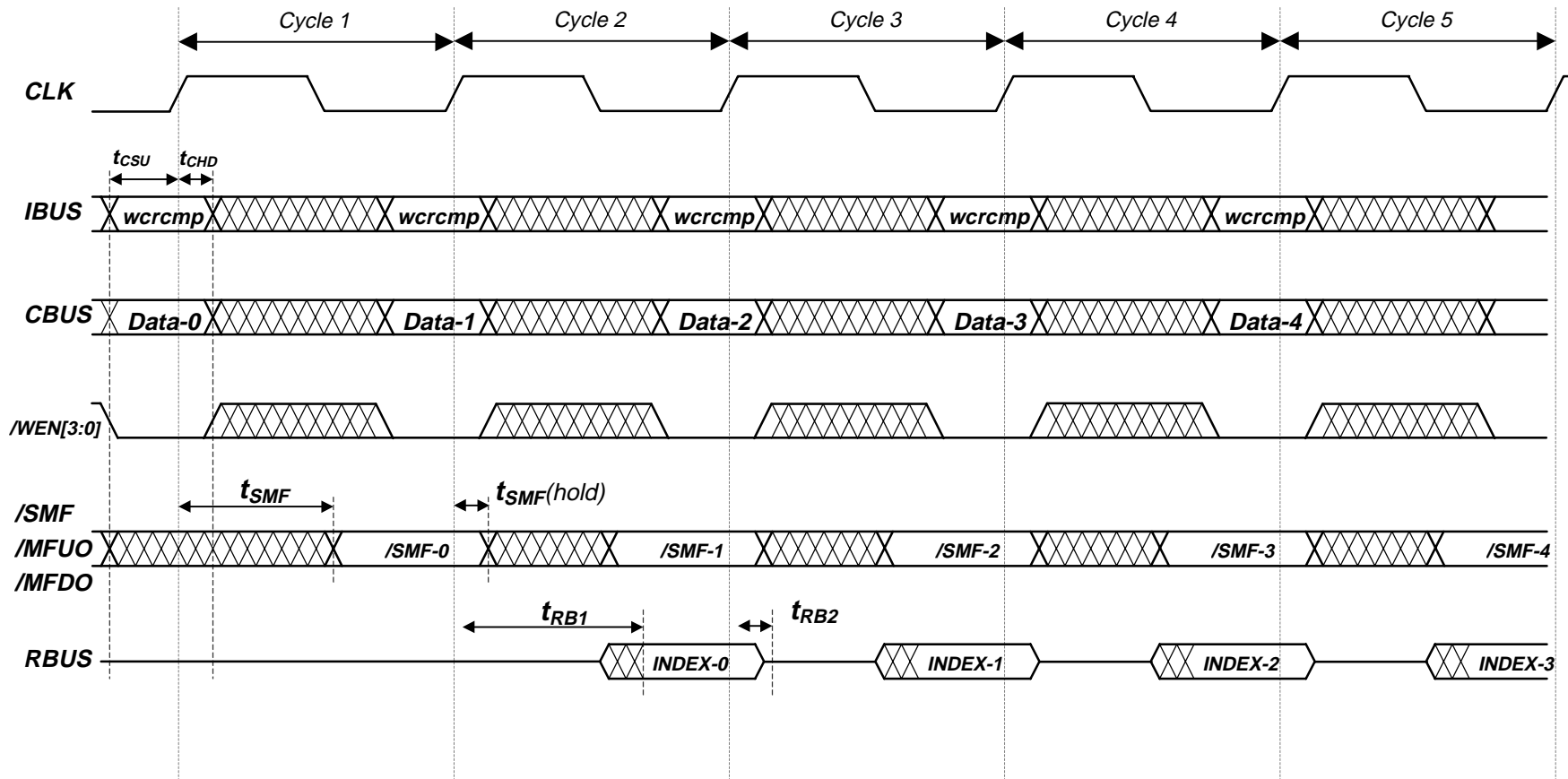
14.0 Timing Diagrams

RESET CYCLE



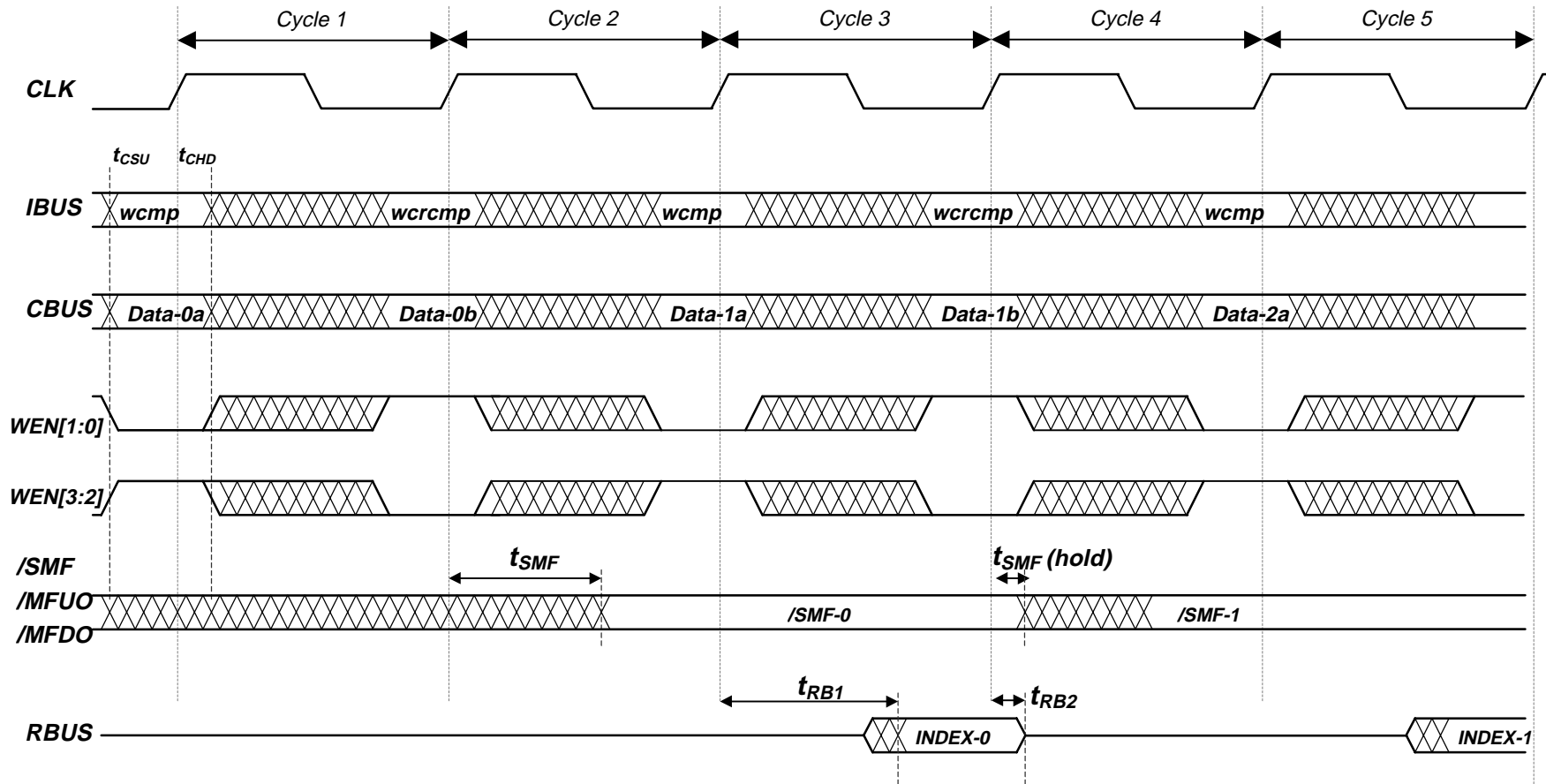
During Reset, CBUS[63:0], IBUS[13:0], and WEN[3:0] inputs are 'don't care'. RBUS is in High-Z. Reset must be followed by at least one "NOP" cycle.

64-bit Word Compare (64-bit interface)



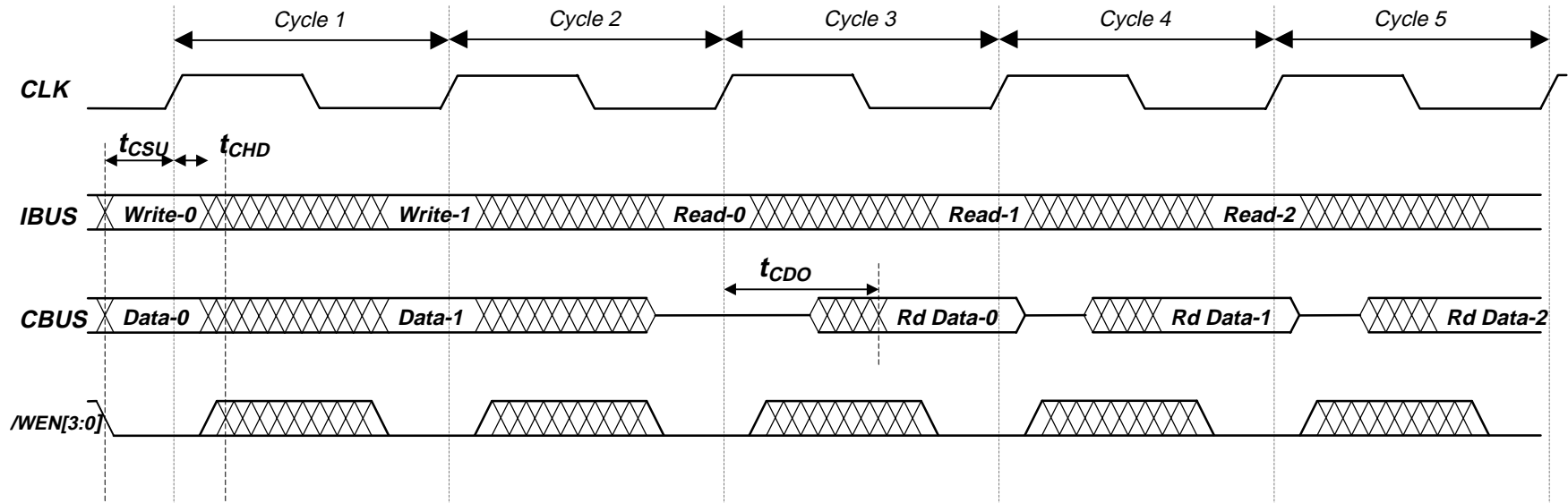
The Compare instruction is issued in the 1st cycle. The corresponding match flag is output in the 1st cycle and the RBUS output in the 2nd cycle. If a compare indicates no match (`/SMF=1'`), the corresponding RBUS output is High-Z. The instruction "Write to Comparand register and Compare" is denoted as "wrcmp". `/CE = '0'` during these cycles.

64-bit Word Compare (32-bit interface)



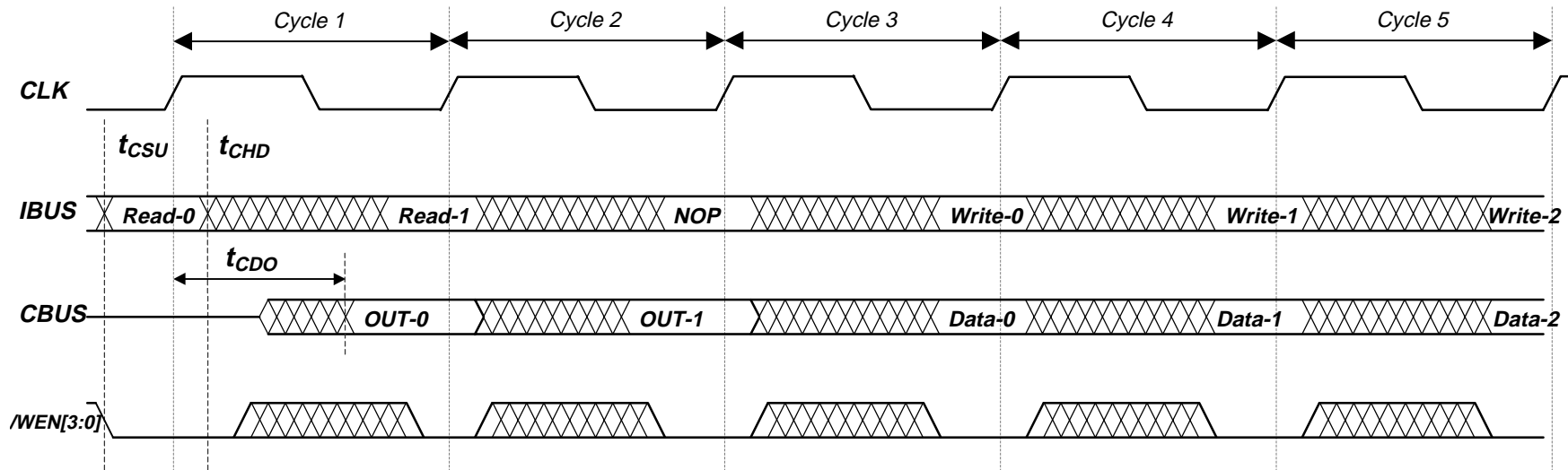
The Compare instruction is issued in the 2nd cycle. The corresponding match flag is output in the 2nd cycle and the RBUS in the 3rd cycle. If the compare instruction indicates no match (*/SMF*=‘1’) the corresponding RBUS output is High-Z. The instruction “Write to Comparand” is denoted as “*wcmp*” and “Write to Comparand and Compare” as “*wrcmp*”. */CE* = ‘0’ during these cycles.

Memory Write-Memory Read Cycles (64-bit interface)



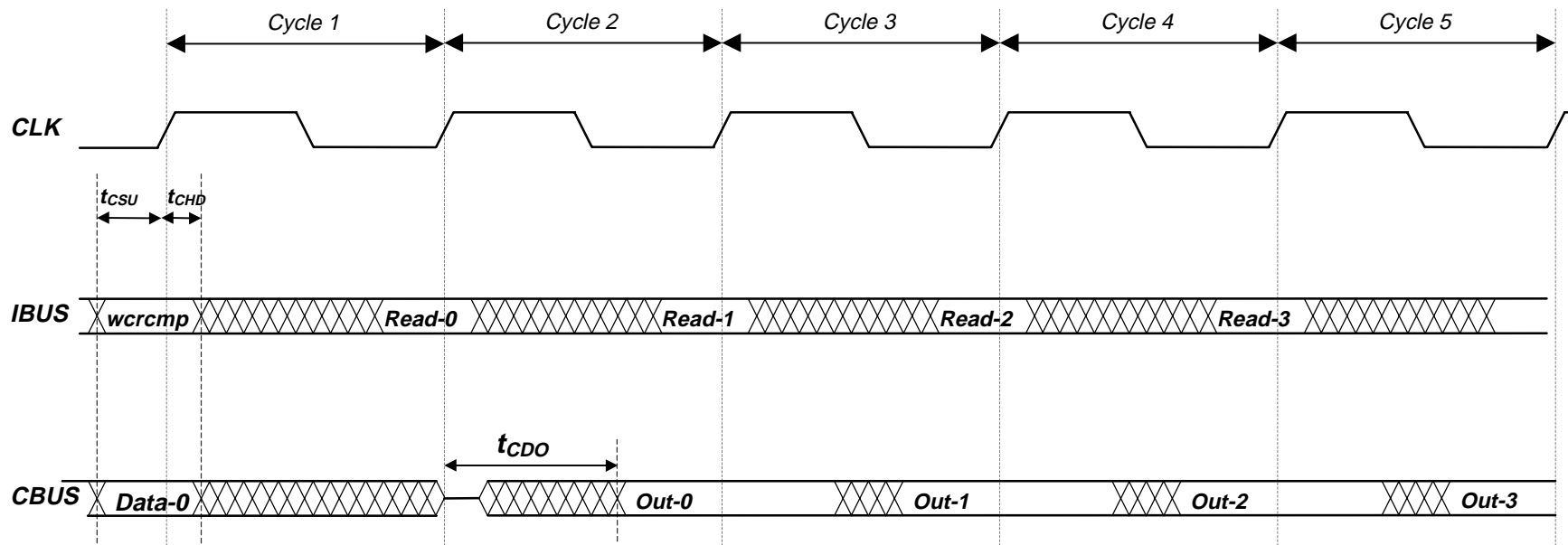
/CE = '0' during these cycles.

Memory Read-Memory Write Cycles (64-bit interface)



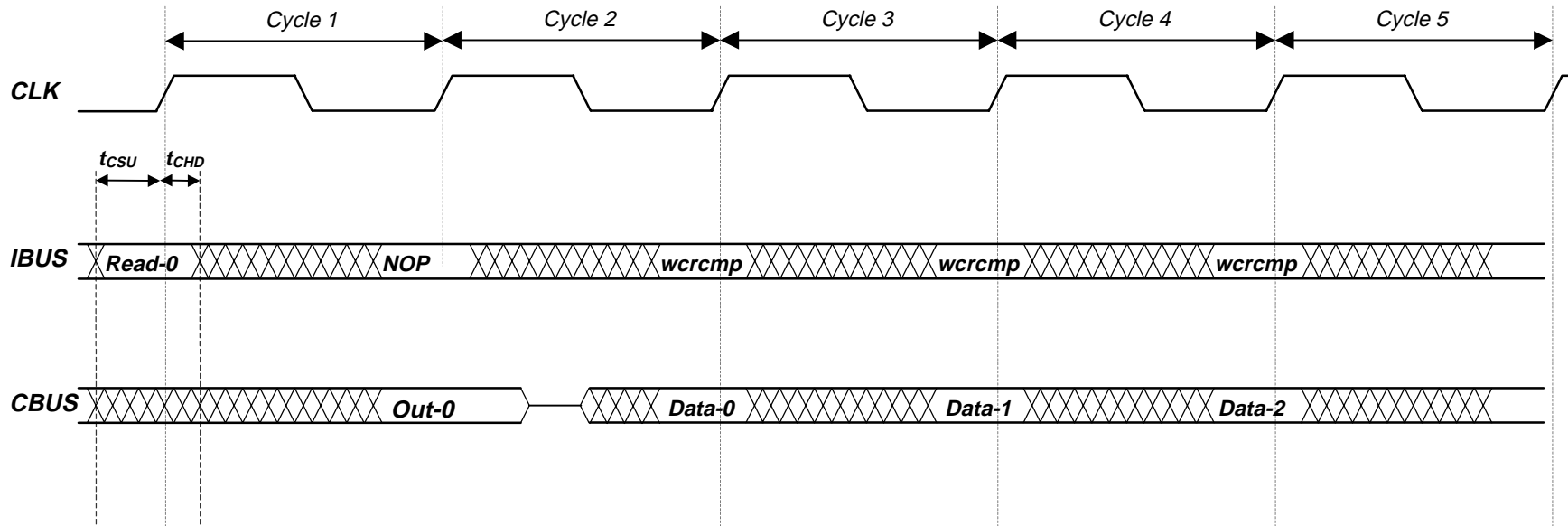
/CE = '0' during these cycles.

Compare/Memory Read Sequence



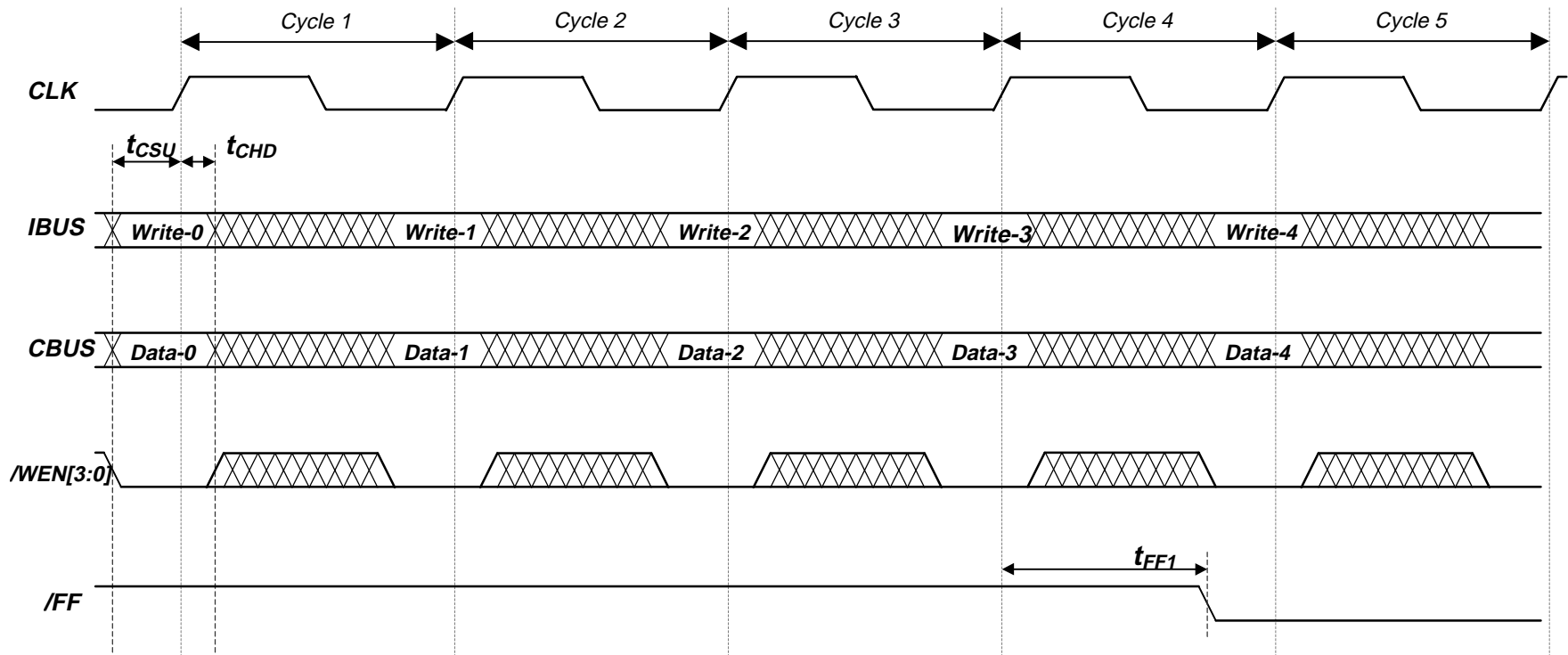
The compare instruction is issued in the 1st cycle. The instruction "Write to Comparand and Compare" is denoted as "wrcmp". /CE = '0' during these cycles.

Memory Read/Compare Sequence (64-bit)



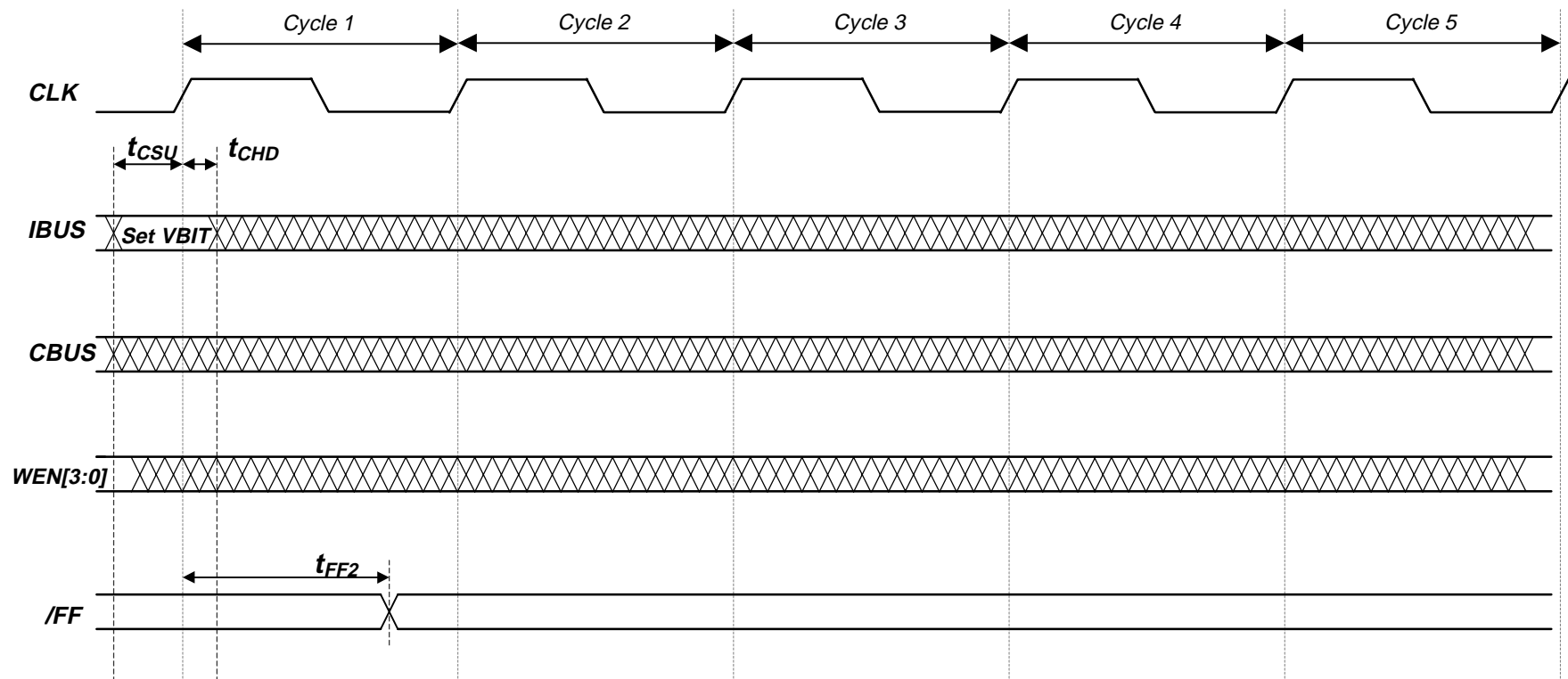
The instruction "Write to Comparand and Compare" as "wrcmp". The $/WEN[3:0]$ inputs are all '0'. $/CE = '0'$ during these cycles.

Memory Write Operation and the Full Flag



The device becomes full after write-3 operation is completed. The Full Flag is asserted in the same cycle as shown. /CE = '0' during these cycles.

Validity Bit Operation and the Full Flag



If the device becomes full after the instruction is executed, the Full Flag is asserted; if the device was originally full and the instruction sets a location to empty, the Full Flag is de-asserted. The Full Flag assertion/Deassertion happens in the same cycle as the instruction. /CE = '0' during these cycles.

14.0 Ordering Information

Part Number	Cycle Time	Package	Comments
NL84620R-33	33MHz	292 PBGA	
NL84620R-40	40MHz	292 PBGA	

15.0 Revision History

Date	Version	Comments
3/25/99	1.0	First Release
3/31/99	1.1	Changed wording in Sec 2.17, modified notes on Table 3g, clarified section 6.0, and added contact info.
4/7/99	1.2	Corrected “64-bit Word Compare (32-bit interface)” and “64-bit Word Compare (64-bit interface)” Timing Diagrams
4/14/99	1.3	Corrected wording in features section and deleted unnecessary table in Sec 13.

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