TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHC03F, TC74VHC03FN, TC74VHC03FT

QUAD 2-INPUT NAND GATE (OPEN DRAIN)

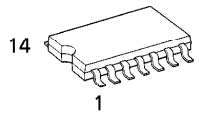
The TC74VHC03 is an advanced high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as the TC74VHC00. But the TC74VHC03 has, as its outputs, high performance MOS N-channel transistors. (OPEN-DRAIN outputs) This device can, therefore, with a suitable pull-up resistors, be used in wired-AND, LED driver and other application.

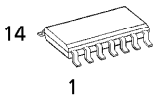
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES:

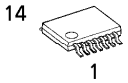
- High Speed ..... t_{pZ} = 3.7ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 2μA(Max.) at Ta = 25°C
- High Noise Immunity ..... $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection is provided on all inputs.
- Wide Operating Voltage Range ···· V_{CC} (opr) = 2V ~ 5.5V
- Low Noise ..... V_{OLP} = 0.8V (Max.)
- Pin and Function Compatible with 74ALS03



F (SOP14-P-300-1.27)
Weight : 0.18g (TYP.)

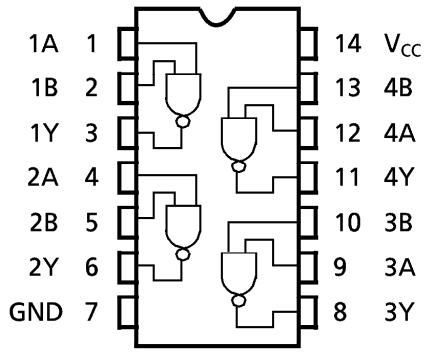


FN (SOL14-P-150-1.27)
Weight : 0.12g (TYP.)



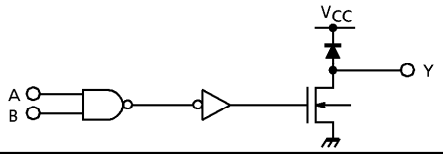
FT (TSSOP14-P-0044-0.65)
Weight : 0.06g (TYP.)

PIN ASSIGNMENT

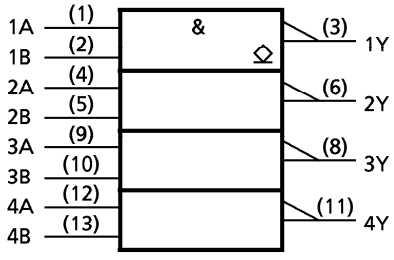


(TOP VIEW)

SYSTEM DIAGRAM (per gate)



IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

961001EBA2

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~100 (V_{CC} = 3.3 ± 0.3V) 0~20 (V_{CC} = 5 ± 0.5V)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0	1.50	−	−	1.50	−	V
				3.0~5.5	V_{CC} × 0.7	−	−	V_{CC} × 0.7	−	
Low - Level Input Voltage	V_{IL}			2.0	−	−	0.50	−	0.50	V
				3.0~5.5	−	−	V_{CC} × 0.3	−	V_{CC} × 0.3	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH}	I_{OL} = 50μA	2.0	−	0.0	0.1	−	0.1	V
				3.0	−	0.0	0.1	−	0.1	
				4.5	−	0.0	0.1	−	0.1	
			I_{OL} = 4mA	3.0	−	−	0.36	−	0.44	
			I_{OL} = 8mA	4.5	−	−	0.36	−	0.44	
Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	−	−	±0.25	−	±2.50	μA
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		0~5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	2.0	−	20.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pZL}	$R_L = 1k\Omega$	3.3 ± 0.3	15	—	5.5	7.9	1.0	9.5	ns
				50	—	8.0	11.4	1.0	13.0	
			5.0 ± 0.5	15	—	3.7	5.5	1.0	6.5	
				50	—	5.2	7.5	1.0	8.5	
Propagation Delay Time	t_{pLZ}	$R_L = 1k\Omega$	3.3 ± 0.3	50	—	8.0	11.4	1.0	13.0	ns
			5.0 ± 0.5	50	—	5.2	7.5	1.0	8.5	
Input Capacitance	C_{IN}				—	4	10	—	10	pF
Output Capacitance	C_{OUT}				—	5	—	—	—	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)			—	6	—	—	—	pF

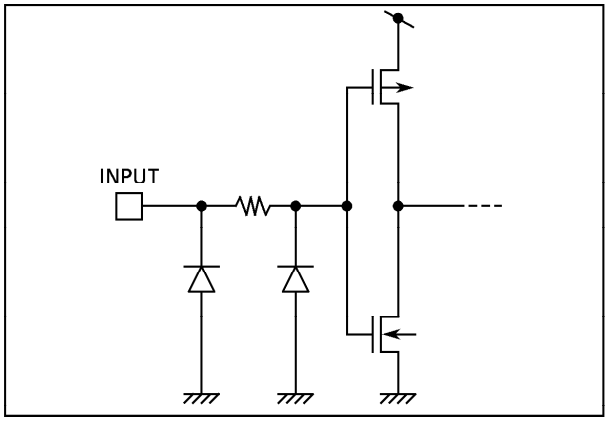
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4 \text{ (per Gate)}$$

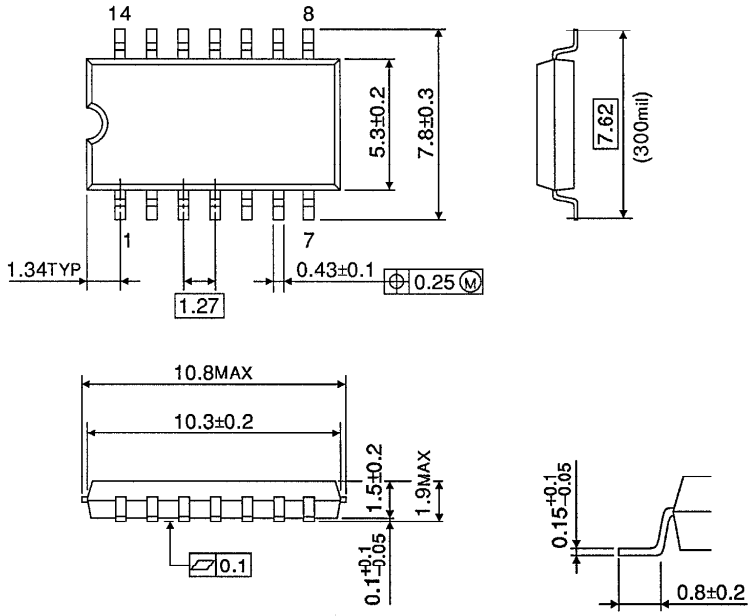
NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$C_L = 50pF$	5.0	0.3	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	$C_L = 50pF$	5.0	−0.3	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	$C_L = 50pF$	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	$C_L = 50pF$	5.0	—	1.5	V

INPUT EQUIVALENT CIRCUIT

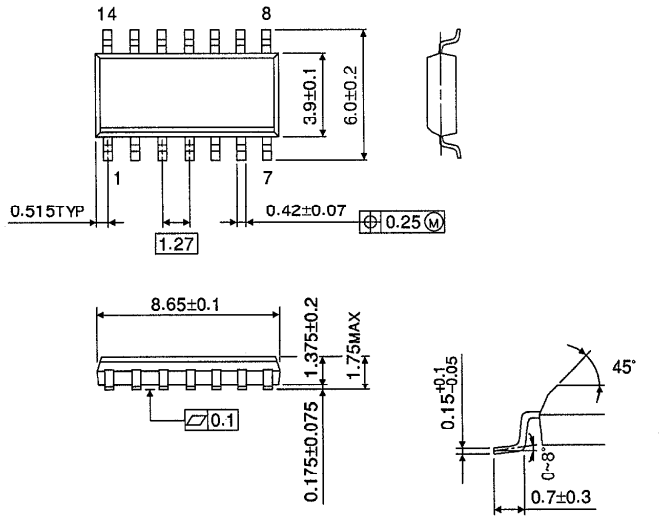


SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27) Unit in mm



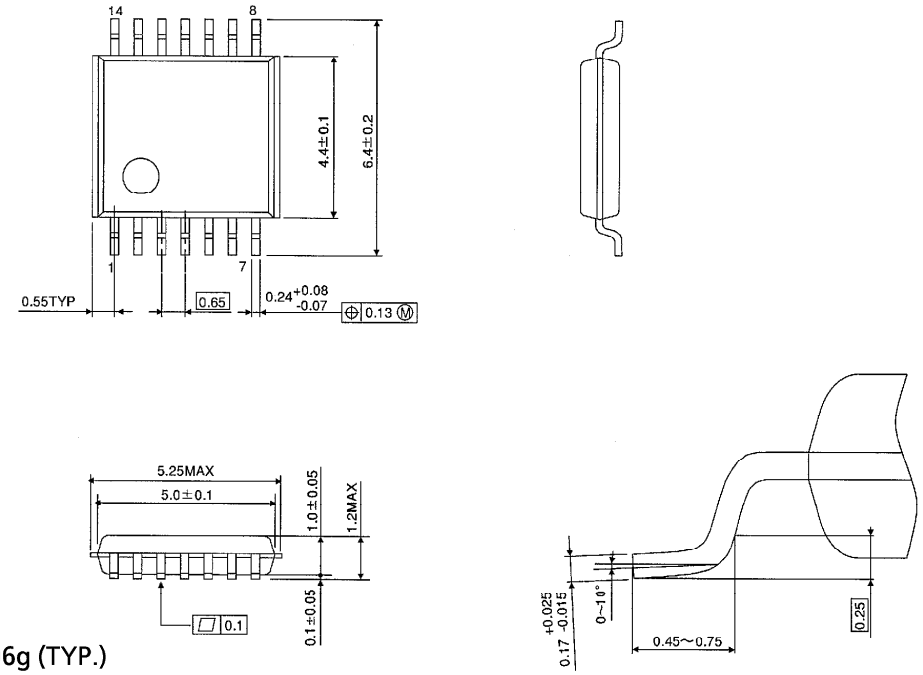
Weight : 0.18g (TYP.)

SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150-1.27) Unit in mm



Weight : 0.12g (TYP.)

TSSOP 14PIN OUTLINE DRAWING (TSSOP14-P-0044-0.65) Unit in mm



Weight : 0.06g (TYP.)