ispMACH™ 4000B/C Family

2.5V/1.8V In-System Programmable SuperFAST™ High Density PLDs

December 2001 **Data Sheet**

Features

■ High Performance

- f_{MAX} = 350MHz maximum operating frequency
- t_{PD} = 2.5ns propagation delay
- Up to four global clock pins with programmable clock polarity control
- Up to 80 PTs per output

■ Ease of Design

- Enhanced macrocells with individual clock, reset, preset and clock enable controls
- Up to four global OE controls
- Individual local OE control per I/O pin
- Excellent First-Time-Fit™ and refit
- Fast path, SpeedLocking™ Path, and wide-PT path
- Wide input gating (36 input logic blocks) for fast counters, state machines and address decoders

■ Low Power

- 1.8V core E²CMOS® technology
- CMOS design techniques provide low static and dynamic power

■ Broad Device Offering

- 32 to 512 macrocells
- 30 to 208 I/O pins
- 44 to 256 pins/balls in TQFP or fpBGA packages
- Commercial and industrial temperature ranges

■ Easy System Integration

- Operation with 3.3V, 2.5V or 1.8V LVCMOS I/O
- Operation with 2.5V (4000B) or 1.8V (4000C) supplies
- Hot-socketing
- Open-drain capability
- Input pull-up, pull-down or bus-keeper
- Programmable output slew rate
- 3.3V PCI compatible
- IEEE 1149.1 boundary scan testable
- 2.5V/1.8V In-System Programmable (ISP™) using IEEE 1532 compliant interface
- I/O pins with fast setup path

Table 1. ispMACH 4000B/C Family Selection Guide

	ispMACH 4032B/C*	**ispMACH 4064B/C***	**ispMACH 4128B/C***	**ispMACH 4256B/C***	**ispMACH 4384B/C***	**ispMACH 4512B/C***
Macrocells	32	64	128	256	384	512
User I/O Options	30/32	30/32/64	64/92	64/128/160	128/192	128/208
t_{PD} (ns)	2.5	2.5	3.0	3.0	3.5	3.5
t_S (ns)	1.75	1.75	2.2	2.2	2.4	2.4
t_{CO} (ns)	2.5	2.5	2.8	2.8	3.5	3.5
f_{MAX} (MHz)	350	350	300	300	256	256
Supply Voltages (V)	2.5/1.8V	2.5/1.8V	2.5/1.8V	2.5/1.8V	2.5/1.8V	2.5/1.8V
Pins/Package	44 TQFP 48 TQFP	44 TQFP 48 TQFP 100 TQFP	100 TQFP 128 TQFP	100 TQFP 176 TQFP 256 fpBGA**	176 TQFP 256 fpBGA	176 TQFP 256 fpBGA

*Preliminary

**128-I/O and 160-I/O configuration.

ispMACH 4000 Introduction

The high performance ispMACH 4000 family from Lattice offers a SuperFAST CPLD solution. The family is a blend of Lattice's two most popular architectures: the ispLSI® 2000 and ispMACH 4A. Retaining the best of both families, the ispMACH 4000 architecture focuses on significant innovations to combine the highest performance with low power in a flexible CPLD family.

The ispMACH 4000 combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

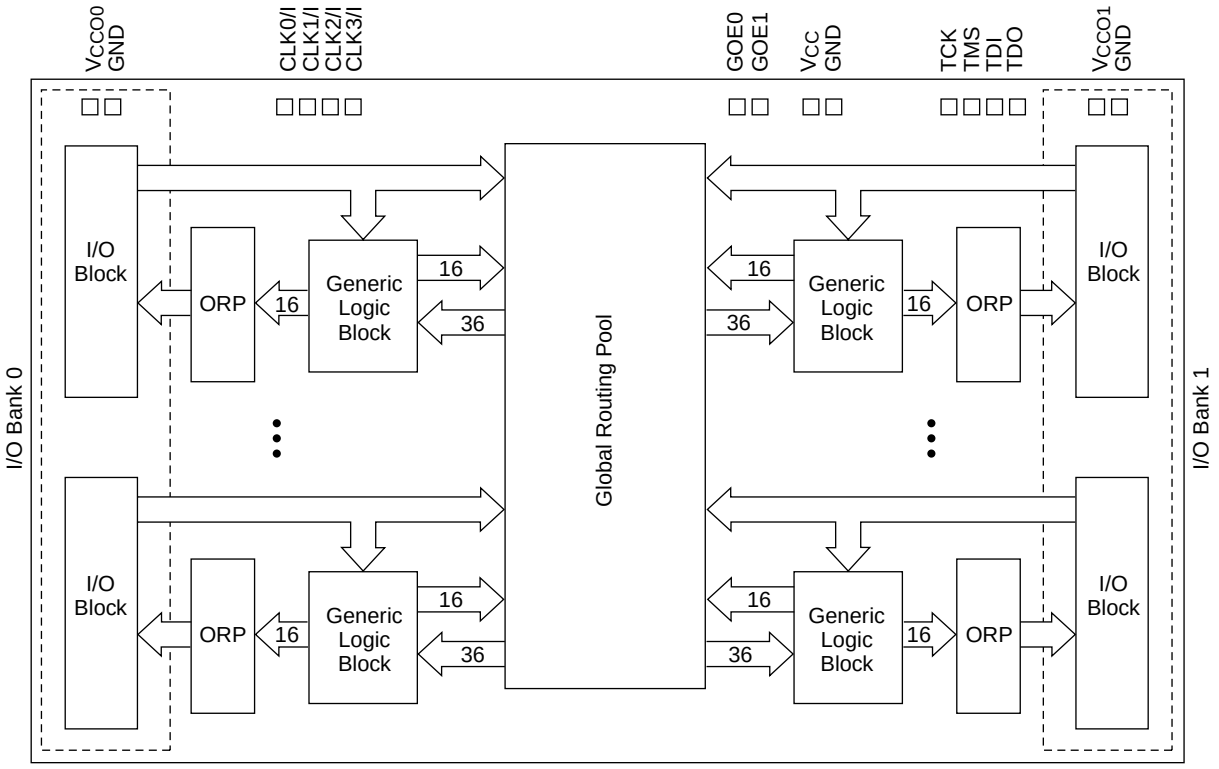
The ispMACH 4000 family offers densities ranging from 32 to 512 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP) and Fine Pitch BGA (fpBGA) packages ranging from 44 to 256 pins/balls. Table 1 shows the macrocell, package and I/O options, along with other key parameters.

The ispMACH 4000 family has enhanced system integration capabilities. It supports 2.5V (4000B) and 1.8V (4000C) supply voltages and 3.3V, 2.5V and 1.8V interface voltages. The ispMACH 4000 also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. The ispMACH 4000 family members are 2.5V/1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment.

Overview

The ispMACH 4000 devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

Figure 1. Functional Block Diagram



The I/Os in the ispMACH 4000 are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments.

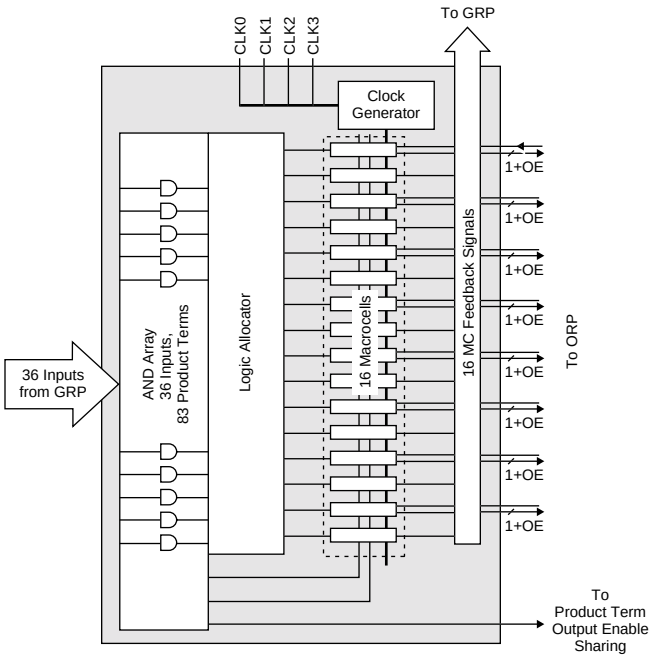
ispMACH 4000 Architecture

There are a total of two GLBs in the ispMACH 4032, increasing to 32 GLBs in the ispMACH 4512. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

Generic Logic Block

The ispMACH 4000 GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

Figure 2. Generic Logic Block

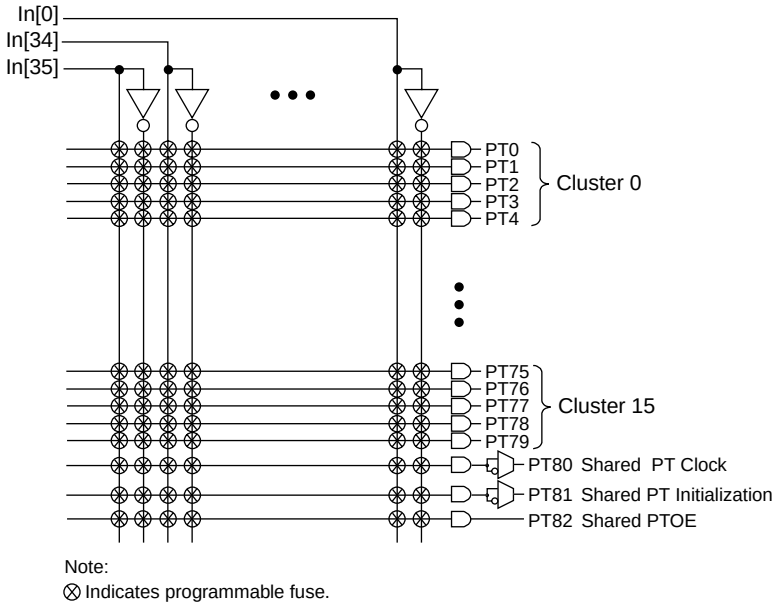


AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

Figure 3. AND Array



Enhanced Logic Allocator

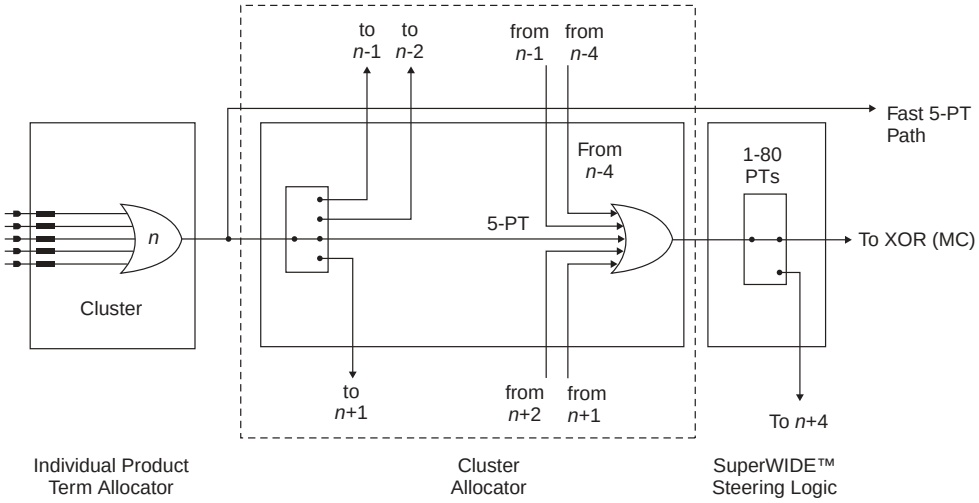
Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000 family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide three speed paths: 5-PT fast bypass path, 20-PT Speed Locking path and an up to 80-PT path. The availability of these three paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000 family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

Figure 4. Macrocell Slice



Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 2 shows the available functions for each of the five product terms in the cluster. The OR gate output connects to the associated I/O cell, providing a fast path for narrow combinatorial functions, and to the logic allocator.

Table 2. Individual PT Steering

Product Term	Logic	Control
PT*n*	Logic PT	Single PT for XOR/OR
PT*n*+1	Logic PT	Individual Clock (PT Clock)
PT*n*+2	Logic PT	Individual Initialization or Individual Clock Enable (PT Initialization/CE)
PT*n*+3	Logic PT	Individual Initialization (PT Initialization)
PT*n*+4	Logic PT	Individual OE (PTOE)

Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 3 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

Table 3. Available Clusters for Each Macrocell

Macrocell	Available Clusters			
M0	—	C0	C1	C2
M1	C0	C1	C2	C3
M2	C1	C2	C3	C4
M3	C2	C3	C4	C5
M4	C3	C4	C5	C6
M5	C4	C5	C6	C7
M6	C5	C6	C7	C8
M7	C6	C7	C8	C9
M8	C7	C8	C9	C10
M9	C8	C9	C10	C11
M10	C9	C10	C11	C12
M11	C10	C11	C12	C13
M12	C11	C12	C13	C14
M13	C12	C13	C14	C15
M14	C13	C14	C15	—
M15	C14	C15	—	—

Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cluster allocator *n*+4. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 4 shows the product term chains.

Table 4. Product Term Expansion Capability

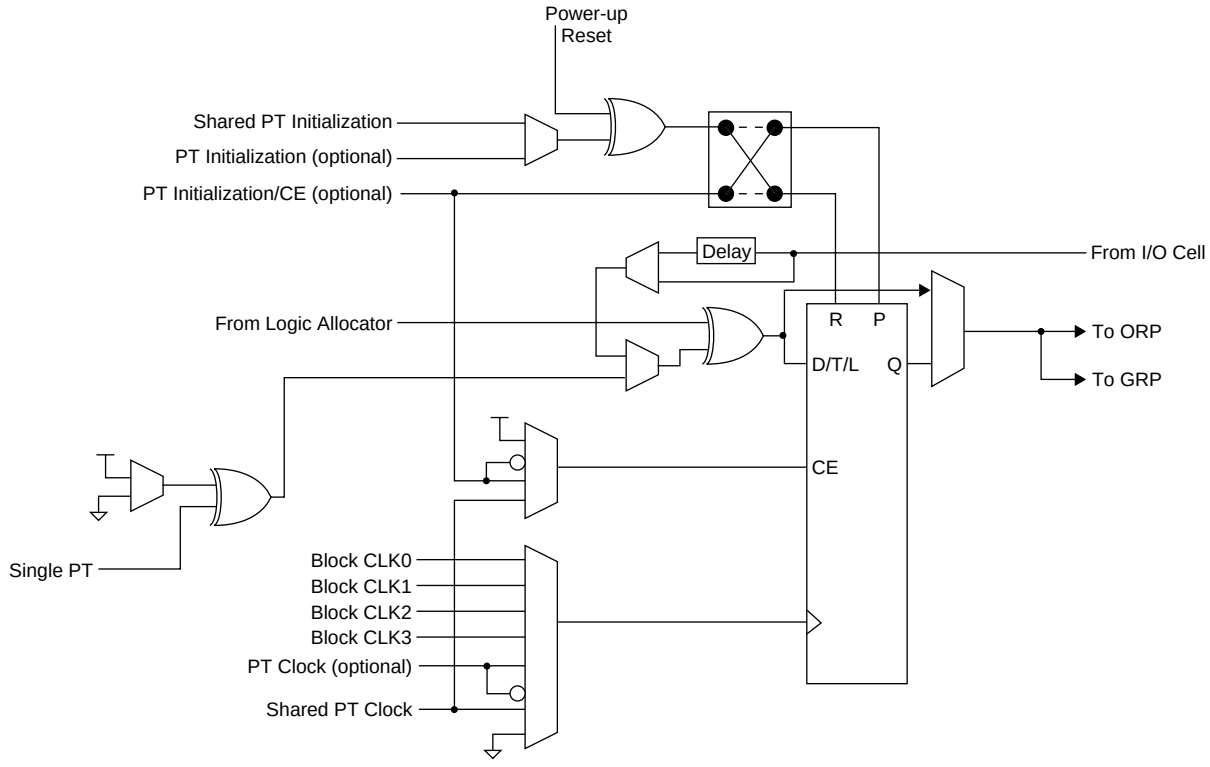
Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/ Macrocell
Chain-0	M0 → M4 → M8 → M12 → M0	75
Chain-1	M1 → M5 → M9 → M13 → M1	80
Chain-2	M2 → M6 → M10 → M14 → M2	75
Chain-3	M3 → M7 → M11 → M15 → M3	70

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP}. When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

Figure 5. Macrocell



Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

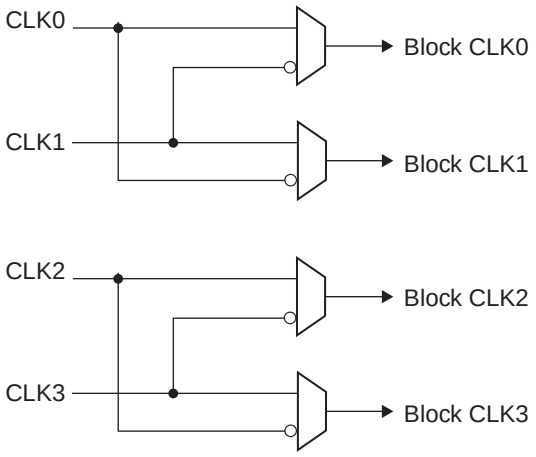
The ispMACH 4000 family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each ispMACH 4000 device has four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator



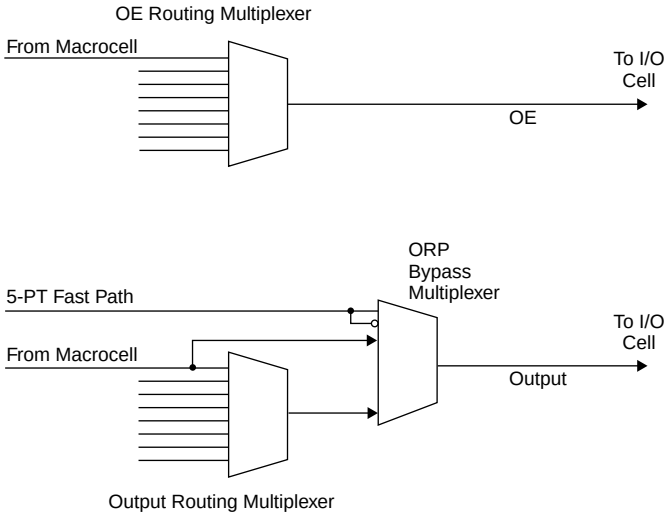
Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. Additionally, the output routing pool allows the macrocell output or true and complement forms of the 5-PT bypass signal to bypass the output routing multipliers and feed the I/O cell directly. The enhanced ORP of the ispMACH 4000 family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers
- Output Routing Pool Bypass Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

Figure 7. ORP Slice



Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 5, 6, 7 and 8 provide the connection details.

Table 5. ORP Combinations for I/O Blocks with 8 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5

Table 6. ORP Combinations for I/O Blocks with 16 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M1, M2, M3, M4, M5, M6, M7, M8
I/O 2	M2, M3, M4, M5, M6, M7, M8, M9
I/O 3	M3, M4, M5, M6, M7, M8, M9, M10
I/O 4	M4, M5, M6, M7, M8, M9, M10, M11
I/O 5	M5, M6, M7, M8, M9, M10, M11, M12
I/O 6	M6, M7, M8, M9, M10, M11, M12, M12
I/O 7	M7, M8, M9, M10, M11, M12, M13, M14
I/O 8	M8, M9, M10, M11, M12, M13, M14, M15
I/O 9	M9, M10, M11, M12, M13, M14, M15, M0
I/O 10	M10, M11, M12, M13, M14, M15, M0, M1
I/O 11	M11, M12, M13, M14, M15, M0, M1, M2
I/O 12	M12, M13, M14, M15, M0, M1, M2, M3
I/O 13	M13, M14, M15, M0, M1, M2, M3, M4
I/O 14	M14, M15, M0, M1, M2, M3, M4, M5
I/O 15	M15, M0, M1, M2, M3, M4, M5, M6

Table 7. ORP Combinations for I/O Blocks with 4 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M4, M5, M6, M7, M8, M9, M10, M11
I/O 2	M8, M9, M10, M11, M12, M13, M14, M15
I/O 3	M12, M13, M14, M15, M0, M1, M2, M3

Table 8. ORP Combinations for I/O Blocks with 10 I/Os

I/O Cell	Available Macrocells
I/O 0	M0, M1, M2, M3, M4, M5, M6, M7
I/O 1	M2, M3, M4, M5, M6, M7, M8, M9
I/O 2	M4, M5, M6, M7, M8, M9, M10, M11
I/O 3	M6, M7, M8, M9, M10, M11, M12, M13
I/O 4	M8, M9, M10, M11, M12, M13, M14, M15
I/O 5	M10, M11, M12, M13, M14, M15, M0, M1
I/O 6	M12, M13, M14, M15, M0, M1, M2, M3
I/O 7	M14, M15, M0, M1, M2, M3, M4, M5
I/O 8	M2, M3, M4, M5, M6, M7, M8
I/O 9	M10, M11, M12, M13, M14, M15, M0, M1

ORP Bypass and Fast Output Multiplexers

The ORP bypass and fast-path output multiplexer is a 4:1 multiplexer and allows the 5-PT fast path to bypass the ORP and be connected directly to the pin with either the regular output or the inverted output. This multiplexer also allows the register output to bypass the ORP to achieve faster t_{CO}.

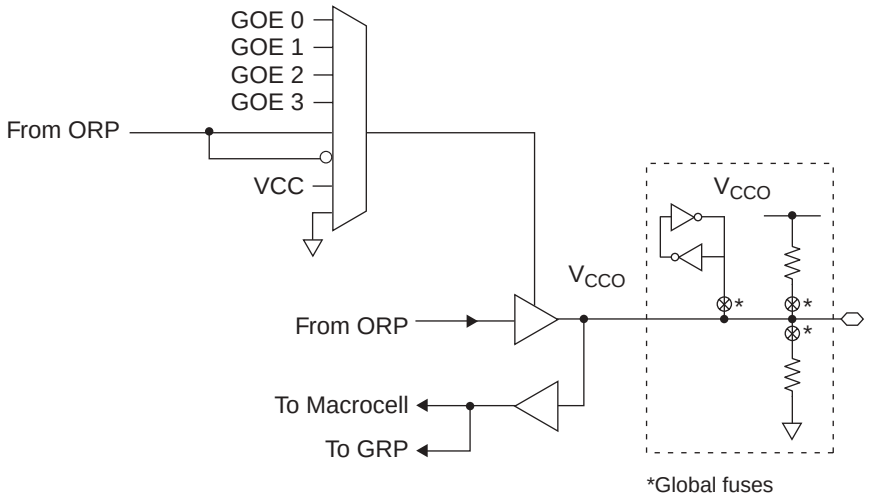
Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer and bus maintenance circuitry. Figure 8 details the I/O cell.

Figure 8. I/O Cell



Each output supports a variety of output standards dependent on the V_{CCO} supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the V_{CCO} supplied to its I/O bank. The I/O standards supported are:

- LVTTL
- LVCMOS 3.3
- LVCMOS 2.5
- LVCMOS 1.8
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, Pull-up Resistor or Pull-down Resistor. A fourth option is to provide none of these. The selection is done on a global basis. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-up Resistor.

Each ispMACH 4000 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (~3V/ns) or for the lower noise transition (~1V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

Global OE Generation

Most ispMACH 4000 family devices have a 4-bit wide Global OE Bus, except the ispMACH 4032 device that has a 2-bit wide Global OE Bus. This bus is derived from a 4-bit internal global OE PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

Figure 9. Global OE Generation for All Devices Except ispMACH 4032

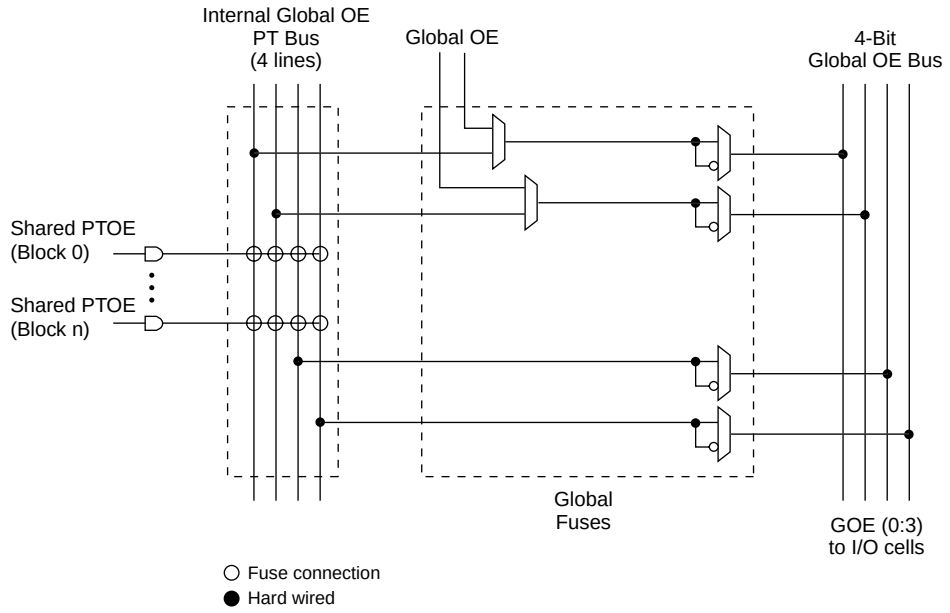
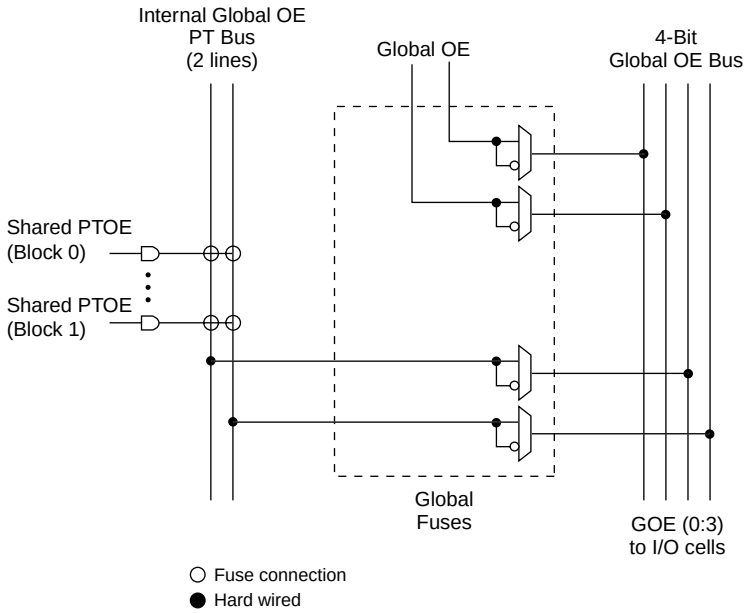


Figure 10. Global OE Generation for ispMACH 4032



Low Power and Power Management

The ispMACH 4000 family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced E^2 low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000 family offers SuperFAST pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 4000 devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os’ physical nature should be minimal so that board test time is minimized. The ispMACH 4000 family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispMACH 4000 devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All ispMACH 4000 devices are also compliant with the IEEE 1532 standard.

The ispMACH 4000 devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispMACH 4000 devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispMACH 4000 devices during the testing of a circuit board.

Security Bit

A programmable security bit is provided on the ispMACH 4000 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

Hot Socketing

The ispMACH 4000 devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals.

Density Migration

The ispMACH 4000 family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Absolute Maximum Ratings[1, 2, 3]

	ispMACH 4000C (1.8V)	ispMACH 4000B (2.5V)
Supply Voltage V_{CC}	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage V_{CCO}	-0.5 to 4.5V	-0.5 to 4.5V
Input or I/O Tristate Voltage Applied[4]	-0.5 to 4.5V	-0.5 to 4.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_j) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IH} (MAX) +2) volts is permitted for a duration of < 20ns.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage for 1.8V Devices	1.65	1.95	V
V_{CC}	Supply Voltage for 2.5V Devices	2.3	2.7	V
T_{JCOM}	Junction Commercial Temperature	0	90	C
T_{JIND}	Junction Industrial Temperature	-40	105	C

Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	±150	µA

1. Insensitive to sequence of V_{CC} and V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).
3. I_{DK} is additive to I_{PU} ,I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

I/O Recommended Operating Conditions

Standard	V_{CCO} (V)[1]	
	Min	Max
LVTTL	3.0	3.6
LVCMOS 3.3	3.0	3.6
LVCMOS 2.5	2.3	2.7
LVCMOS 1.8	1.65	1.95
PCI 3.3	3.0	3.6

1. Typical values for V_{CCO} are the average of the Min and Max values.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IL}, I_{IH}[1]	Input Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	10	µA
I_{PU}	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7V_{CCO}$	30	—	150	µA
I_{PD}	I/O Weak Pull-down Resistor Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
V_{BHT}	Bus Hold Trip Points	—	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C_1	I/O Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

Supply Current

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
ispMACH 4256B/C						
I_{CC}[1, 2, 3]	Operating Power Supply Current	V_{CC} = 2.5V	—	12.5	—	mA
		V_{CC} = 1.8V	—	2.5	—	
I_{CC}[4]	Standby Power Supply Current	V_{CC} = 2.5V	—	12	—	mA
		V_{CC} = 1.8V	—	2	—	mA
ispMACH 4512B/C						
I_{CC}[1, 2, 3]	Operating Power Supply Current	V_{CC} = 2.5V	—	12.5	—	mA
		V_{CC} = 1.8V	—	2.5	—	
I_{CC}[4]	Standby Power Supply Current	V_{CC} = 2.5V	—	12	—	mA
		V_{CC} = 1.8V	—	2	—	mA

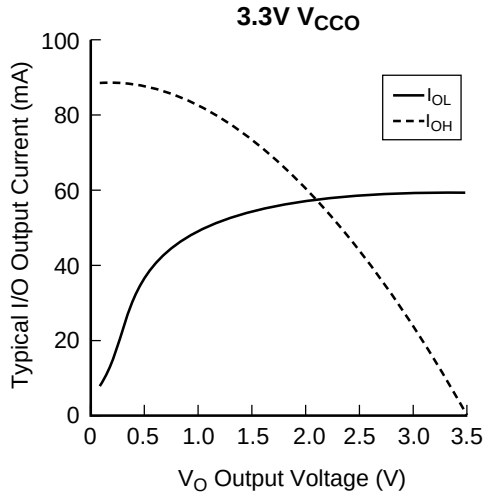
1. T_A = 25°C, frequency = 1.0MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. T_A = 25°C

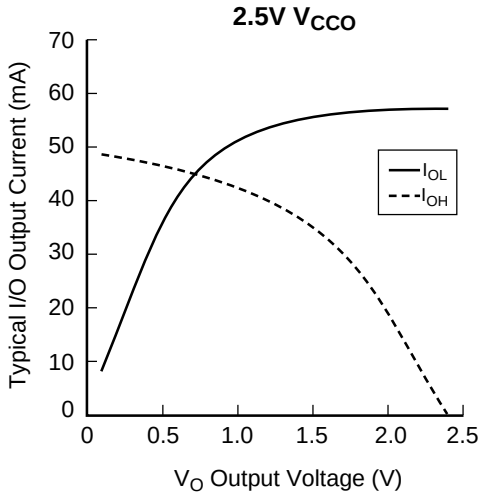
I/O DC Electrical Characteristics

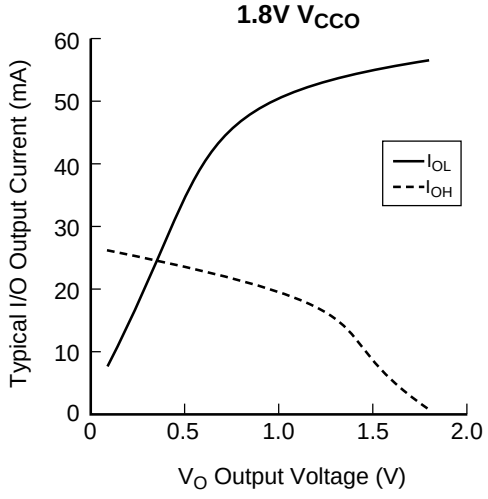
Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTL	-0.3	0.80	2.0	3.6	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 3.3	-0.3	0.80	2.0	3.6	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCO}$	$0.65V_{CCO}$	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
PCI 3.3	-0.3	$0.3\ V_{CC}$	$0.5\ V_{CC}$	3.6	$0.1\ V_{CCO}$	$0.9\ V_{CCO}$	1.5	-0.5

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed *n**8mA. Where *n* is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.







ispMACH 4256B/C External Switching Characteristics (Preliminary)

Over Recommended Operating Conditions

Parameter	Description[1,2,3]	-3		-5		-75		-10[5]		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	5-PT bypass combinatorial propagation delay	—	3.0	—	5.0	—	7.5	—	10.0	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	4.0	—	6.7	—	10.0	—	13.4	ns
t_S	GLB register setup time before clock	2.2	—	3.7	—	5.5	—	7.4	—	ns
t_{ST}	GLB register setup time before clock with T-type register	2.2	—	3.7	—	5.5	—	7.4	—	ns
t_{SIR}	GLB register setup time before clock, input register path	0.8	—	1.4	—	2.0	—	2.7	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.2	—	3.7	—	5.5	—	7.4	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.4	—	2.4	—	3.5	—	4.7	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	2.8	—	4.7	—	7.0	—	9.4	ns
t_R	External reset pin to output delay	—	4.4	—	7.4	—	11.0	—	14.7	ns
t_{RW}	External reset pulse duration	2.5	—	4.2	—	7.0	—	11.6	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	5.0	—	8.4	—	12.5	—	16.7	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	8.0	—	13.4	—	20.0	—	26.7	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	4.0	—	6.7	—	10.0	—	13.4	ns
t_{CW}	Global clock width, high or low	1.3	—	2.2	—	3.3	—	5.5	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.3	—	2.2	—	3.3	—	5.5	—	ns
t_{WIR}	Input register clock width, high or low	1.3	—	2.2	—	3.3	—	5.5	—	ns
f_{MAX}[4]	Clock frequency with internal feedback	300	—	180	—	120	—	90	—	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $[1/ (t_S + t_{CO})]$	200	—	120	—	80	—	60	—	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards. Timing v.2.6
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.
5. Only available for industrial grade.

ispMACH 4512B/C External Switching Characteristics (Preliminary)

Over Recommended Operating Conditions

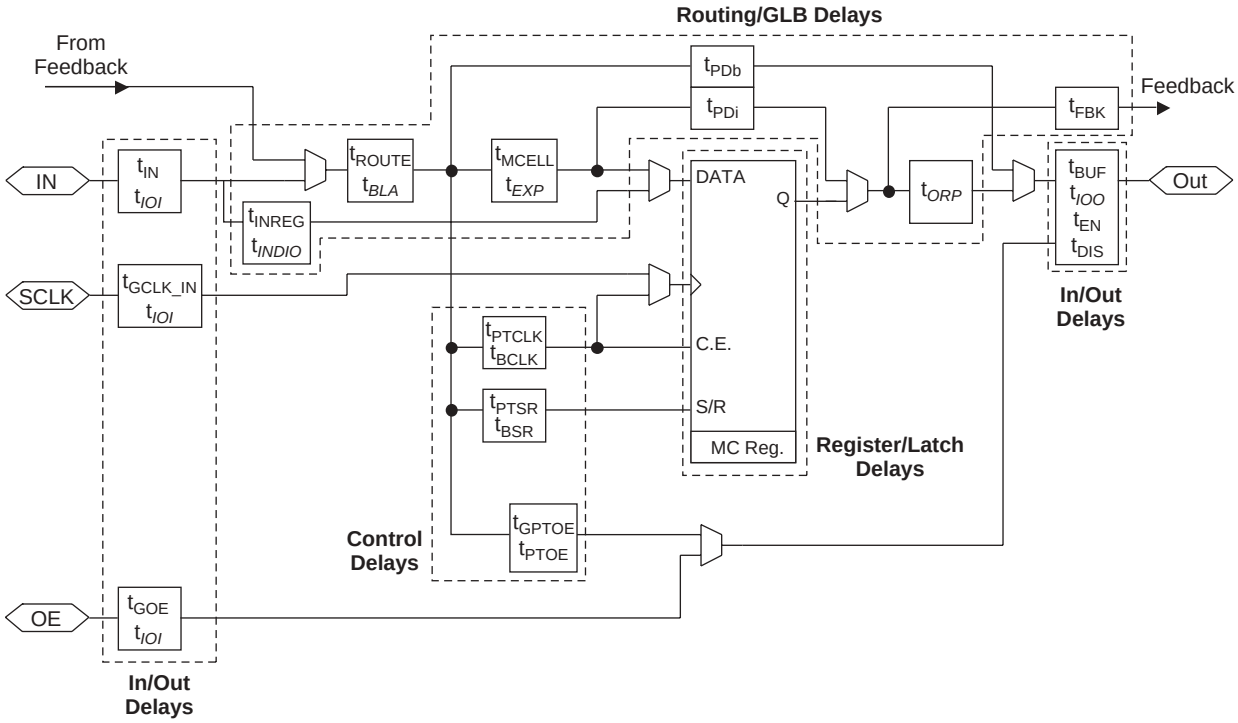
Parameter	Description[1,2,3]	-35		-5		-75		-10[5]		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	5-PT bypass combinatorial propagation delay	—	3.5	—	5.0	—	7.5	—	10.0	ns
t_{PD_MC}	20-PT combinatorial propagation delay through macrocell	—	4.7	—	6.7	—	10.0	—	13.4	ns
t_S	GLB register setup time before clock	2.4	—	3.4	—	5.0	—	6.7	—	ns
t_{ST}	GLB register setup time before clock with T-type register	2.4	—	3.4	—	5.0	—	6.7	—	ns
t_{SIR}	GLB register setup time before clock, input register path	0.6	—	0.9	—	1.3	—	1.7	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.4	—	3.4	—	5.0	—	6.7	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.8	—	2.5	—	3.8	—	5.0	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	3.5	—	5.0	—	7.5	—	10.0	ns
t_R	External reset pin to output delay	—	5.2	—	7.4	—	11.0	—	14.7	ns
t_{RW}	External reset pulse duration	3.0	—	4.2	—	7.0	—	11.6	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	5.9	—	8.4	—	12.5	—	16.7	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	9.4	—	13.4	—	20.0	—	26.7	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	4.7	—	6.7	—	10.0	—	13.4	ns
t_{CW}	Global clock width, high or low	1.6	—	2.2	—	3.3	—	5.5	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.6	—	2.2	—	3.3	—	5.5	—	ns
t_{WIR}	Input register clock width, high or low	1.6	—	2.2	—	3.3	—	5.5	—	ns
f_{MAX}[4]	Clock frequency with internal feedback	256	—	180	—	120	—	90	—	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $[1/ (t_S + t_{CO})]$	170	—	120	—	80	—	60	—	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards. Timing v.0.1
2. Measured using standard switching circuit, assuming GRP loading of 1 and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.
5. Only available for industrial grade.

Timing Model

The task of determining the timing through the ispMACH 4000 family, like any CPLD, is relatively simple. The timing model provided in Figure 10 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, please refer to Technical Note TN1004: *ispMACH 4000 Timing Model Design and Usage Guidelines.*

Figure 10. ispMACH 4000 Timing Model



Note: Italicized items are optional delay adders.

ispMACH 4256B/C Internal Timing Parameters (Preliminary)

Over Recommended Operating Conditions

Parameter	Description	-3		-5		-75		-10[1]		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
In/Out Delays										
t_{IN}	Input Buffer Delay	—	0.65	—	1.08	—	1.63	—	2.17	ns
t_{GOE}	Global OE Pin Delay	—	2.45	—	4.08	—	6.13	—	8.17	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.40	—	2.33	—	3.50	—	4.67	ns
t_{BUF}	Delay through Output Buffer	—	0.90	—	1.50	—	2.25	—	3.00	ns
t_{EN}	Output Enable Time	—	1.55	—	2.58	—	3.88	—	5.17	ns
t_{DIS}	Output Disable Time	—	1.55	—	2.58	—	3.88	—	5.17	ns
Routing/GLB Delays										
t_{ROUTE}	Delay through GRP	—	1.40	—	2.33	—	3.50	—	4.67	ns
t_{MCELL}	Macrocell Delay	—	0.90	—	1.50	—	2.25	—	3.00	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.90	—	1.50	—	2.25	—	3.00	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	0.05	—	0.08	—	0.13	—	0.17	ns
t_{PDi}	Macrocell Propagation Delay	—	0.05	—	0.08	—	0.13	—	0.17	ns
Register/Latch Delays										
t_{S}	Register Setup Time, D Flip-Flop	0.65	—	1.08	—	1.63	—	2.17	—	ns
t_{S_PT}	D-Register Setup (PT Clock)	1.45	—	2.42	—	3.63	—	4.83	—	ns
t_{ST}	Register Setup Time, T Flip-Flop	0.65	—	1.08	—	1.63	—	2.17	—	ns
t_{ST_PT}	Register Setup Time, T Flip-Flop (PT Clock)	1.45	—	2.42	—	3.63	—	4.83	—	ns
t_{H}	Register Hold Time, D Flip-Flop	1.55	—	2.58	—	3.88	—	5.17	—	ns
t_{HT}	Register Hold Time, T Flip-Flop	1.55	—	2.58	—	3.88	—	5.17	—	ns
t_{COi}	Register Clock to ORP Time	—	0.40	—	0.67	—	1.00	—	1.33	ns
t_{CES}	Clock Enable Setup Time	1.20	—	2.00	—	3.00	—	4.00	—	ns
t_{CEH}	Clock Enable Hold Time	2.25	—	3.75	—	5.63	—	7.50	—	ns
t_{SL}	Latch Setup Time	0.65	—	1.08	—	1.63	—	2.17	—	ns
t_{SL_PT}	Latch Setup Time (PT Clock)	1.45	—	2.42	—	3.63	—	4.83	—	ns
t_{HL}	Latch Hold Time	1.55	—	2.58	—	3.88	—	5.17	—	ns
t_{GOi}	Latch Gate to ORP Time	—	0.40	—	0.67	—	1.00	—	1.33	ns
t_{PDLi}	Propagation Delay through Transparent Latch to ORP	—	0.30	—	0.50	—	0.75	—	1.00	ns
t_{SRi}	Asynchronous Reset or Set to ORP Delay	—	0.50	—	0.83	—	1.25	—	1.67	ns
t_{SRR}	Asynchronous Reset or Set Recovery	—	2.00	—	3.33	—	5.00	—	6.67	ns
Control Delays										
t_{BCLK}	Block PT Clock Delay	—	1.40	—	2.33	—	3.50	—	4.67	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	1.15	—	1.92	—	2.88	—	3.83	ns
t_{BSR}	Block PT Set/Reset Delay	—	1.10	—	1.83	—	2.75	—	3.67	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	0.85	—	1.42	—	2.13	—	2.83	ns
t_{GPTOE}	Global PT OE Delay	—	4.40	—	7.33	—	11.00	—	14.67	ns
t_{PTOE}	Macrocell PT OE Delay	—	1.40	—	2.33	—	3.50	—	4.67	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to Timing Model in this data sheet for further details. Timing v.2.6

1. Only available for industrial grade.

ispMACH 4512B/C Internal Timing Parameters (Preliminary)

Over Recommended Operating Conditions

Parameter	Description	-35		-5		-75		-10[1]		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
In/Out Delays										
t_{IN}	Input Buffer Delay	—	0.76	—	1.08	—	1.63	—	2.17	ns
t_{GOE}	Global OE Pin Delay	—	2.86	—	4.08	—	6.13	—	8.17	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.87	—	2.67	—	4.00	—	5.33	ns
t_{BUF}	Delay through Output Buffer	—	1.05	—	1.50	—	2.25	—	3.00	ns
t_{EN}	Output Enable Time	—	1.81	—	2.58	—	3.88	—	5.17	ns
t_{DIS}	Output Disable Time	—	1.81	—	2.58	—	3.88	—	5.17	ns
Routing/GLB Delays										
t_{ROUTE}	Delay through GRP	—	1.63	—	2.33	—	3.50	—	4.67	ns
t_{MCELL}	Macrocell Delay	—	1.05	—	1.50	—	2.25	—	3.00	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.93	—	1.33	—	2.00	—	2.67	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{PDb}	5-PT Bypass Propagation Delay	—	0.06	—	0.08	—	0.13	—	0.17	ns
t_{PDi}	Macrocell Propagation Delay	—	0.06	—	0.08	—	0.13	—	0.17	ns
Register/Latch Delays										
t_{S}	Register Setup Time, D Flip-Flop	0.76	—	1.08	—	1.63	—	2.17	—	ns
t_{S_PT}	D-Register Setup (PT Clock)	1.69	—	2.42	—	3.63	—	4.83	—	ns
t_{ST}	Register Setup Time, T Flip-Flop	0.76	—	1.08	—	1.63	—	2.17	—	ns
t_{ST_PT}	Register Setup Time, T Flip-Flop (PT Clock)	1.69	—	2.42	—	3.63	—	4.83	—	ns
t_{H}	Register Hold Time, D Flip-Flop	1.58	—	2.25	—	3.38	—	4.50	—	ns
t_{HT}	Register Hold Time, T Flip-Flop	1.58	—	2.25	—	3.38	—	4.50	—	ns
t_{COi}	Register Clock to ORP Time	—	0.47	—	0.67	—	1.00	—	1.33	ns
t_{CES}	Clock Enable Setup Time	1.63	—	2.33	—	3.50	—	4.67	—	ns
t_{CEH}	Clock Enable Hold Time	2.63	—	3.75	—	5.63	—	7.50	—	ns
t_{SL}	Latch Setup Time	0.76	—	1.08	—	1.63	—	2.17	—	ns
t_{SL_PT}	Latch Setup Time (PT Clock)	1.69	—	2.42	—	3.63	—	4.83	—	ns
t_{HL}	Latch Hold Time	1.63	—	2.33	—	3.50	—	4.67	—	ns
t_{GOi}	Latch Gate to ORP Time	—	0.47	—	0.67	—	1.00	—	1.33	ns
t_{PDLi}	Propagation Delay through Transparent Latch to ORP	—	0.35	—	0.50	—	0.75	—	1.00	ns
t_{SRi}	Asynchronous Reset or Set to ORP Delay	—	0.58	—	0.83	—	1.25	—	1.67	ns
t_{SRR}	Asynchronous Reset or Set Recovery	—	2.33	—	3.33	—	5.00	—	6.67	ns
Control Delays										
t_{BCLK}	Block PT Clock Delay	—	1.63	—	2.33	—	3.50	—	4.67	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	1.34	—	1.92	—	2.88	—	3.83	ns
t_{BSR}	Block PT Set/Reset Delay	—	1.28	—	1.83	—	2.75	—	3.67	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	0.99	—	1.42	—	2.13	—	2.83	ns
t_{GPTOE}	Global PT OE Delay	—	5.13	—	7.33	—	11.00	—	14.67	ns
t_{PTOE}	Macrocell PT OE Delay	—	1.63	—	2.33	—	3.50	—	4.67	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to Timing Model in this data sheet for further details. Timing v.0.1

1. Only available for industrial grade.

ispMACH 4256B/C Timing Adders (Preliminary)[1]

Adder Type	Base Parameter	Description	-3		-5		-75		-10[2]		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Optional Delay Adders											
t_{INDIO}	t_{INREG}	Input register delay	—	1.40	—	2.33	—	3.50	—	4.67	ns
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.33	—	0.56	—	0.83	—	1.11	ns
t_{ORP}	—	Output routing pool delay	—	0.10	—	0.17	—	0.25	—	0.33	ns
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.04	—	0.07	—	0.10	—	0.13	ns
t_{IOI} Input Adjusters											
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	—	0.00	—	0.00	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	—	0.60	ns
t_{IOO} Output Adjusters											
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	—	0.10	ns
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	—	0.00	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.2.6

1. Refer to Technical Note TN1004: *ispMACH 4000 Timing Model Design and Usage Guidelines* for information regarding usage of these adders.
2. Only available for industrial grade.

ispMACH 4512B/C Timing Adders (Preliminary)[1]

Adder Type	Base Parameter	Description	-35		-5		-75		-10[2]		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Optional Delay Adders											
t_{INDIO}	t_{INREG}	Input register delay	—	1.75	—	2.50	—	3.75	—	5.00	ns
t_{EXP}	t_{MCELL}	Product term expander delay	—	0.39	—	0.56	—	0.83	—	1.11	ns
t_{ORP}	—	Output routing pool delay	—	0.12	—	0.17	—	0.25	—	0.33	ns
t_{BLA}	t_{ROUTE}	Additional block loading adder	—	0.05	—	0.07	—	0.10	—	0.13	ns
t_{IOI} Input Adjusters											
LVTTL_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVTTL standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 3.3 standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 2.5 standard	—	0.60	—	0.60	—	0.60	—	0.60	ns
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using LVCMOS 1.8 standard	—	0.00	—	0.00	—	0.00	—	0.00	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{GOE}	Using PCI compatible input	—	0.60	—	0.60	—	0.60	—	0.60	ns
t_{IOO} Output Adjusters											
LVTTL_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as TTL buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
LVCMOS33_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
LVCMOS25_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V buffer	—	0.10	—	0.10	—	0.10	—	0.10	ns
LVCMOS18_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V buffer	—	0.00	—	0.00	—	0.00	—	0.00	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as PCI compatible buffer	—	0.20	—	0.20	—	0.20	—	0.20	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.00	—	1.00	—	1.00	—	1.00	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.0.1

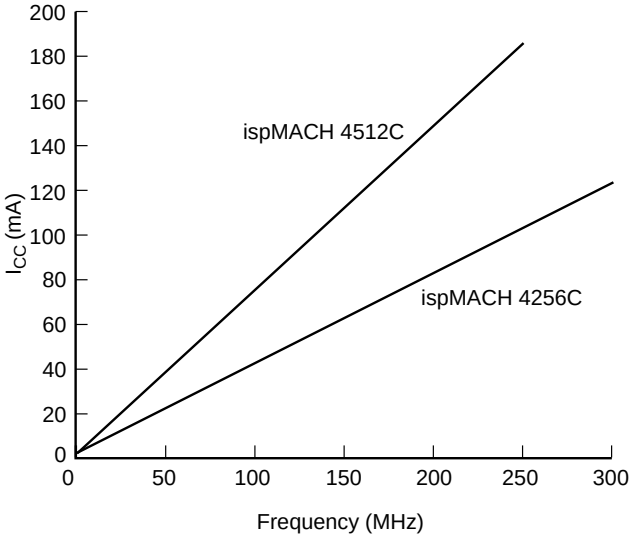
1. Refer to Technical Note TN1004: *ispMACH 4000 Timing Model Design and Usage Guidelines* for information regarding usage of these adders.
2. Only available for industrial grade.

Boundary Scan Waveforms and Timing Specifications

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN test] clock cycle	40	—	ns
t_{BTCH}	TCK [BSCAN test] pulse width high	20	—	ns
t_{BTCL}	TCK [BSCAN test] pulse width low	20	—	ns
t_{BTSU}	TCK [BSCAN test] setup time	8	—	ns
t_{BTH}	TCK [BSCAN test] hold time	10	—	ns
t_{BRF}	TCK [BSCAN test] rise and fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t_{BTOZ}	TAP controller falling edge of clock to data output disable	—	10	ns
t_{BTVO}	TAP controller falling edge of clock to data output enable	—	10	ns
t_{BTCPSU}	BSCAN test Capture register setup time	8	—	ns
t_{BTCPH}	BSCAN test Capture register hold time	10	—	ns
t_{BTUCO}	BSCAN test Update reg, falling edge of clock to valid output	—	25	ns
t_{BTUOZ}	BSCAN test Update reg, falling edge of clock to output disable	—	25	ns
t_{BTUOV}	BSCAN test Update reg, falling edge of clock to output enable	—	25	ns

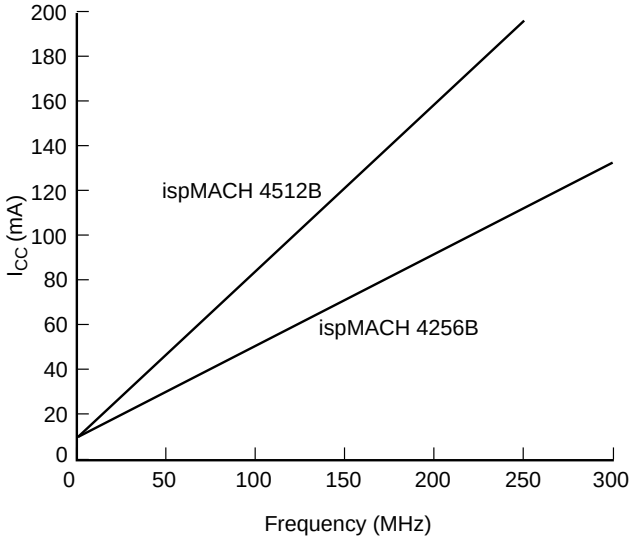
Power Consumption

ispMACH 4000C
Typical I_{CC} vs. Frequency



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25° C.

ispMACH 4000B
Typical I_{CC} vs. Frequency



Note: The devices are configured with maximum number of 16-bit counters, typical current at 2.5V, 25° C.

Power Estimation Coefficients

Device	A	B
ispMACH 4032B	—	—
ispMACH 4032C	—	—
ispMACH 4064B	—	—
ispMACH 4064C	—	—
ispMACH 4128B	—	—
ispMACH 4128C	—	—
ispMACH 4256B	12	0.0115
ispMACH 4256C	2	0.0115
ispMACH 4384B	—	—
ispMACH 4384C	—	—
ispMACH 4512B	12	0.0115
ispMACH 4512C	2	0.0115

Note: For further information about the use of these coefficients, refer to Technical Note TN1005, *Power Estimation in ispMACH 4000B/C Devices*.

Switching Test Conditions

Figure 11 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 9.

Figure 11. Output Test Load, LVTTL and LVCMOS Standards

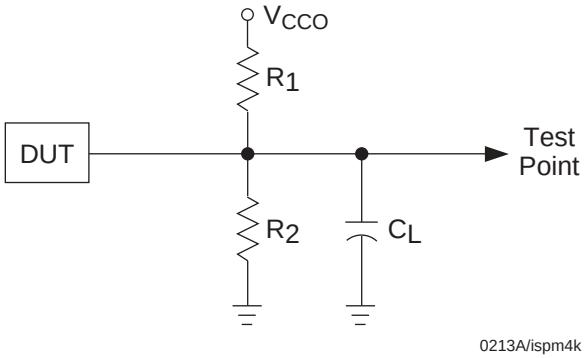


Table 9. Test Fixture Required Components

Test Condition	R_1	R_2	C_L[1]	Timing Ref.	V_{CCO}
LVCMOS I/O, (L -> H, H -> L)	106Ω	106Ω	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = V_{CCO}/2	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = V_{CCO}/2	LVCMOS 1.8 = 1.65V
LVCMOS I/O (Z -> H)	∞	106Ω	35pF	1.5V	3.0V
LVCMOS I/O (Z -> L)	106Ω	∞	35pF	1.5V	3.0V
LVCMOS I/O (H -> Z)	∞	106Ω	5pF	V_{OH} - 0.3	3.0V
LVCMOS I/O (L -> Z)	106Ω	∞	5pF	V_{OL} + 0.3	3.0V

1. C_L includes test fixtures and probe capacitance.

Signal Descriptions

Signal Names	Description	
TMS	Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine	
TCK	Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine	
TDI	Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data	
TDO	Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out	
GOE0, GOE1	Input – These pins are the Global Output Enable Input pins	
GND	Ground	
NC	Not Connected	
V_{CC}	The power supply pins for logic core	
CLK0/I, CLK1/I, CLK2/I, CLK3/I	These pins are configured to be either CLK input or as an input	
V_{CCO0}, V_{CCO1}	The power supply pins for each I/O bank	
yzz	Input/Output[1] – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15	
	ispMACH 4032	y: A-B
	ispMACH 4064	y: A-D
	ispMACH 4128	y: A-G
	ispMACH 4256	y: A-P
	ispMACH 4384	y: A-X
	ispMACH 4512	y: A-AH

1. In some packages, certain I/O are only available for use as inputs. See the signal connections table for details.

ispMACH 4256B/C and 4512B/C Power Supply and NC Connections[1]

Signal	100 TQFP	176 TQFP	256 fpBGA[2, 3, 4]
V_{CC}	25, 40, 75, 90	42, 69, 88, 130, 157, 176	B2, B15, G8, G9, K8, K9, R2, R15
V_{CCO0}	13, 33, 95	4, 22, 40, 56, 166	D6, F4, H7, J7, L4, N6
V_{CCO1}	45, 63, 83	78, 92, 110, 128, 144	D11, F13, H10, J10, L13, N11
GND	1, 26, 51, 76	2, 46, 65, 90, 134, 153	A1, A16, C6, C11, F3, F14, G7, G10, H8, H9, J8, J9, K7, K10, L3, L14, P6, P11, T1, T16
GND (Bank0)	7, 18, 32, 96	13, 31, 55, 155, 167	
GND (Bank1)	46, 57, 68, 82	67, 79, 101, 119, 143	
NC	—	1, 43, 44, 45, 89, 131, 132, 133	A4, A5, A6, A11, A12, A13, A15, B5, B6, B11, B12, B14, C7, D1, D4, D5, D10, D12, D16, E1, E2, E4, E5, E7, E10, E13, E14, E15, E16, F1, F2, F15, F16, G1, G4, G5, G6, G12, G13, G14, J11, K3, K4, K15, L1, L2, L12, L15, L16, M1, M2, M3, M4, M5, M12, M13, M15, M16, N1, N2, N7, N10, N12, N14, P5, P12, R4, R5, R6, R11, R12, R16, T2, T4, T5, T6, T11, T12, T13, T15

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Internal GNDs and I/O GNDs (Bank 0/1) are connected inside package.
3. V_{CCO} balls connect to two power planes within the package, one for V_{CCO0} and one for V_{CCO1}.
4. No connect (NC) balls listed are for the ispMACH 4256B/C devices only. There are no NC signals on the ispMACH 4512B/C devices.

ispMACH 4256B/C Logic Signal Connections: 100 TQFP

Bank No	GLB	ORP	ispMACH 4256B/C
-	GND	-	1
-	TDI	-	2
0	C14	C^7	-
0	C12	C^6	3
0	C10	C^5	4
0	C8	C^4	-
0	C6	C^3	5
0	C4	C^2	-
0	C2	C^1	6
0	C0	C^0	-
0	GND (Bank 0)	-	7
0	D14	D^7	-
0	D12	D^6	8
0	D10	D^5	9
0	D8	D^4	-
0	D6	D^3	10
0	D4	D^2	11
0	D2	D^1	-
0	D0	D^0	12*
0	VCC (Bank 0)	-	13
0	E0	E^0	-
0	E2	E^1	-
0	E4	E^2	14
0	E6	E^3	15
0	E8	E^4	-
0	E10	E^5	16
0	E12	E^6	17
0	E14	E^7	-
0	GND (Bank 0)	-	18
0	F0	F^0	-
0	F2	F^1	19
0	F4	F^2	-
0	F6	F^3	20
0	F8	F^4	-
0	F10	F^5	21
0	F12	F^6	22
0	F14	F^7	23*
-	TCK	-	24
-	VCC	-	25
-	GND	-	26
0	G14	G^7	27*
0	G12	G^6	28
0	G10	G^5	29
0	G8	G^4	-

ispMACH 4256B/C Logic Signal Connections: 100 TQFP (Cont.)

Bank No	GLB	ORP	ispMACH 4256B/C
0	G6	G^3	30
0	G4	G^2	-
0	G2	G^1	31
0	G0	G^0	-
0	GND (Bank 0)	-	32
0	VCC (Bank 0)	-	33
0	H14	H^7	-
0	H12	H^6	34
0	H10	H^5	35
0	H8	H^4	-
0	H6	H^3	36
0	H4	H^2	-
0	H2	H^1	37
0	H0	H^0	-
-	CLK1/I	-	38
-	CLK2/I	-	39
-	VCC	-	40
1	I0	I^0	-
1	I2	I^1	41
1	I4	I^2	-
1	I6	I^3	42
1	I8	I^4	-
1	I10	I^5	43
1	I12	I^6	44
1	I14	I^7	-
1	VCC (Bank 1)	-	45
1	GND (Bank 1)	-	46
1	J0	J^0	-
1	J2	J^1	47
1	J4	J^2	-
1	J6	J^3	48
1	J8	J^4	-
1	J10	J^5	49
1	J12	J^6	50
1	J14	J^7	-
-	GND	-	51
-	TMS	-	52
1	K14	K^7	-
1	K12	K^6	53
1	K10	K^5	54
1	K8	K^4	-
1	K6	K^3	55
1	K4	K^2	-
1	K2	K^1	56

ispMACH 4256B/C Logic Signal Connections: 100 TQFP (Cont.)

Bank No	GLB	ORP	ispMACH 4256B/C
1	K0	K^0	-
1	GND (Bank 1)	-	57
1	L14	L^7	-
1	L12	L^6	58
1	L10	L^5	59
1	L8	L^4	-
1	L6	L^3	60
1	L4	L^2	61
1	L2	L^1	-
1	L0	L^0	62*
1	VCC (Bank 1)	-	63
1	M0	M^0	-
1	M2	M^1	-
1	M4	M^2	64
1	M6	M^3	65
1	M8	M^4	-
1	M10	M^5	66
1	M12	M^6	67
1	M14	M^7	-
1	GND (Bank 1)	-	68
1	N0	N^0	-
1	N2	N^1	69
1	N4	N^2	-
1	N6	N^3	70
1	N8	N^4	-
1	N10	N^5	71
1	N12	N^6	72
1	N14	N^7	73*
1	VCC (Bank 1)	-	-
-	TDO	-	74
-	VCC	-	75
-	GND	-	76
1	O14	O^7	77*
1	O12	O^6	78
1	O10	O^5	79
1	O8	O^4	-
1	O6	O^3	80
1	O4	O^2	-
1	O2	O^1	81
1	O0	O^0	-
1	GND (Bank 1)	-	82
1	VCC (Bank 1)	-	83
1	P14	P^7	-
1	P12	P^6	84

ispMACH 4256B/C Logic Signal Connections: 100 TQFP (Cont.)

Bank No	GLB	ORP	ispMACH 4256B/C
1	P10	P^5	85
1	P8	P^4	-
1	P6	P^3	86
1	P4	P^2	-
1	P2/GOE1	P^1	87
1	P0	P^0	-
-	CLK3/I	-	88
-	CLK0/I	-	89
-	VCC	-	90
0	A0	A^0	-
0	A2/GOE0	A^1	91
0	A4	A^2	-
0	A6	A^3	92
0	A8	A^4	-
0	A10	A^5	93
0	A12	A^6	94
0	A14	A^7	-
0	VCC (Bank 0)	-	95
0	GND (Bank 0)	-	96
0	B0	B^0	-
0	B2	B^1	97
0	B4	B^2	-
0	B6	B^3	98
0	B8	B^4	-
0	B10	B^5	99
0	B12	B^6	100

*This pin is input only in this package.

ispMACH 4256B/C, 4512B/C Logic Signal Connections: 176 TQFP

Pin Number	Bank Number	ispMACH 4256B/C		ispMACH 4512B/C	
		GLB	ORP	GLB	ORP
1	-	NC	-	NC	-
2	-	GND	-	GND	-
3	-	TDI	-	TDI	-
4	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
5	0	C14	C^7	C14	C^7
6	0	C12	C^6	C12	C^6
7	0	C10	C^5	C10	C^5
8	0	C8	C^4	C8	C^4
9	0	C6	C^3	C6	C^3
10	0	C4	C^2	C4	C^2
11	0	C2	C^1	C2	C^1

ispMACH 4256B/C, 4512B/C Logic Signal Connections: 176 TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4256B/C		ispMACH 4512B/C	
		GLB	ORP	GLB	ORP
12	0	C0	C^0	C0	C^0
13	0	GND (Bank 0)	-	GND (Bank 0)	-
14	0	D14	D^7	G14	G^7
15	0	D12	D^6	G12	G^6
16	0	D10	D^5	G10	G^5
17	0	D8	D^4	G8	G^4
18	0	D6	D^3	G6	G^3
19	0	D4	D^2	G4	G^2
20	0	D2	D^1	G2	G^1
21	0	D0	D^0	G0	G^0
22	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
23	0	E0	E^0	J0	J^0
24	0	E2	E^1	J2	J^1
25	0	E4	E^2	J4	J^2
26	0	E6	E^3	J6	J^3
27	0	E8	E^4	J8	J^4
28	0	E10	E^5	J10	J^5
29	0	E12	E^6	J12	J^6
30	0	E14	E^7	J14	J^7
31	0	GND (Bank 0)	-	GND (Bank 0)	-
32	0	F0	F^0	N0	N^0
33	0	F2	F^1	N2	N^1
34	0	F4	F^2	N4	N^2
35	0	F6	F^3	N6	N^3
36	0	F8	F^4	N8	N^4
37	0	F10	F^5	N10	N^5
38	0	F12	F^6	N12	N^6
39	0	F14	F^7	N14	N^7
40	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
41	-	TCK	-	TCK	-
42	-	VCC	-	VCC	-
43	-	NC	-	NC	-
44	-	NC	-	NC	-
45	-	NC	-	NC	-
46	-	GND (Bank 0)	-	GND (Bank 0)	-
47	0	G14	G^7	O14	O^7
48	0	G12	G^6	O12	O^6
49	0	G10	G^5	O10	O^5
50	0	G8	G^4	O8	O^4
51	0	G6	G^3	O6	O^3
52	0	G4	G^2	O4	O^2
53	0	G2	G^1	O2	O^1
54	0	G0	G^0	O0	O^0

ispMACH 4256B/C, 4512B/C Logic Signal Connections: 176 TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4256B/C		ispMACH 4512B/C	
		GLB	ORP	GLB	ORP
55	0	GND (Bank 0)	-	GND (Bank 0)	-
56	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
57	0	H14	H^7	P14	P^7
58	0	H12	H^6	P12	P^6
59	0	H10	H^5	P10	P^5
60	0	H8	H^4	P8	P^4
61	0	H6	H^3	P6	P^3
62	0	H4	H^2	P4	P^2
63	0	H2	H^1	P2	P^1
64	0	H0	H^0	P0	P^0
65	-	GND	-	GND	-
66	-	CLK1/I	-	CLK1/I	-
67	1	GND (Bank 1)	-	GND (Bank 1)	-
68	-	CLK2/I	-	CLK2/I	-
69	-	VCC	-	VCC	-
70	1	I0	I^0	AX0	AX^0
71	1	I2	I^1	AX2	AX^1
72	1	I4	I^2	AX4	AX^2
73	1	I6	I^3	AX6	AX^3
74	1	I8	I^4	AX8	AX^4
75	1	I10	I^5	AX10	AX^5
76	1	I12	I^6	AX12	AX^6
77	1	I14	I^7	AX14	AX^7
78	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
79	1	GND (Bank 1)	-	GND (Bank 1)	-
80	1	J0	J^0	BX0	BX^0
81	1	J2	J^1	BX2	BX^1
82	1	J4	J^2	BX4	BX^2
83	1	J6	J^3	BX6	BX^3
84	1	J8	J^4	BX8	BX^4
85	1	J10	J^5	BX10	BX^5
86	1	J12	J^6	BX12	BX^6
87	1	J14	J^7	BX14	BX^7
88	-	VCC	-	VCC	-
89	-	NC	-	NC	-
90	-	GND (Bank 1)	-	GND (Bank 1)	-
91	-	TMS	-	TMS	-
92	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
93	1	K14	K^7	CX14	CX^7
94	1	K12	K^6	CX12	CX^6
95	1	K10	K^5	CX10	CX^5
96	1	K8	K^4	CX8	CX^4
97	1	K6	K^3	CX6	CX^3

ispMACH 4256B/C, 4512B/C Logic Signal Connections: 176 TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4256B/C		ispMACH 4512B/C	
		GLB	ORP	GLB	ORP
98	1	K4	K^2	CX4	CX^2
99	1	K2	K^1	CX2	CX^1
100	1	K0	K^0	CX0	CX^0
101	1	GND (Bank 1)	-	GND (Bank 1)	-
102	1	L14	L^7	GX14	GX^7
103	1	L12	L^6	GX12	GX^6
104	1	L10	L^5	GX10	GX^5
105	1	L8	L^4	GX8	GX^4
106	1	L6	L^3	GX6	GX^3
107	1	L4	L^2	GX4	GX^2
108	1	L2	L^1	GX2	GX^1
109	1	L0	L^0	GX0	GX^0
110	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
111	1	M0	M^0	JX0	JX^0
112	1	M2	M^1	JX2	JX^1
113	1	M4	M^2	JX4	JX^2
114	1	M6	M^3	JX6	JX^3
115	1	M8	M^4	JX8	JX^4
116	1	M10	M^5	JX10	JX^5
117	1	M12	M^6	JX12	JX^6
118	1	M14	M^7	JX14	JX^7
119	1	GND (Bank 1)	-	GND (Bank 1)	-
120	1	N0	N^0	NX0	NX^0
121	1	N2	N^1	NX2	NX^1
122	1	N4	N^2	NX4	NX^2
123	1	N6	N^3	NX6	NX^3
124	1	N8	N^4	NX8	NX^4
125	1	N10	N^5	NX10	NX^5
126	1	N12	N^6	NX12	NX^6
127	1	N14	N^7	NX14	NX^7
128	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
129	-	TDO	-	TDO	-
130	-	VCC	-	VCC	-
131	-	NC	-	NC	-
132	-	NC	-	NC	-
133	-	NC	-	NC	-
134	-	GND (Bank 1)	-	GND (Bank 1)	-
135	1	O14	O^7	OX14	OX^7
136	1	O12	O^6	OX12	OX^6
137	1	O10	O^5	OX10	OX^5
138	1	O8	O^4	OX8	OX^4
139	1	O6	O^3	OX6	OX^3
140	1	O4	O^2	OX4	OX^2

ispMACH 4256B/C, 4512B/C Logic Signal Connections: 176 TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4256B/C		ispMACH 4512B/C	
		GLB	ORP	GLB	ORP
141	1	O2	O^1	OX2	OX^1
142	1	O0	O^0	OX0	OX^0
143	1	GND (Bank 1)	-	GND (Bank 1)	-
144	1	VCCO (Bank 1)	-	VCCO (Bank 1)	-
145	1	P14	P^7	PX14	PX^7
146	1	P12	P^6	PX12	PX^6
147	1	P10	P^5	PX10	PX^5
148	1	P8	P^4	PX8	PX^4
149	1	P6	P^3	PX6	PX^3
150	1	P4	P^2	PX4	PX^2
151	1	P2/GOE1	P^1	PX2/GOE1	PX^1
152	1	P0	P^0	PX0	PX^0
153	-	GND	-	GND	-
154	-	CLK3/I	-	CLK3/I	-
155	0	GND (Bank 0)	-	GND (Bank 0)	-
156	-	CLK0/I	-	CLK0/I	-
157	-	VCC	-	VCC	-
158	0	A0	A^0	A0	A^0
159	0	A2/GOE0	A^1	A2//GOE0	A^1
160	0	A4	A^2	A4	A^2
161	0	A6	A^3	A6	A^3
162	0	A8	A^4	A8	A^4
163	0	A10	A^5	A10	A^5
164	0	A12	A^6	A12	A^6
165	0	A14	A^7	A14	A^7
166	0	VCCO (Bank 0)	-	VCCO (Bank 0)	-
167	0	GND (Bank 0)	-	GND (Bank 0)	-
168	0	B0	B^0	B0	B^0
169	0	B2	B^1	B2	B^1
170	0	B4	B^2	B4	B^2
171	0	B6	B^3	B6	B^3
172	0	B8	B^4	B8	B^4
173	0	B10	B^5	B10	B^5
174	0	B12	B^6	B12	B^6
175	0	B14	B^7	B14	B^7
176	-	VCC	-	-	-

ispMACH 4256B/C, 4512B/C Logic Signal Connections: 256 fpBGA

BGA Ball Number	Bank Number	ispMACH 4256B/C		ispMACH 4512B/C	
		GLB	ORP	GLB	ORP
VCC	-	-	-	-	-
GND	-	-	-	-	-
C3	0	TDI	-	TDI	-
VCCO (Bank 0)	0	-	-	-	-
B1	0	C14	C^7	C14	C^7
F5	0	C12	C^6	C12	C^6
D3	0	C10	C^5	C10	C^5
C1	0	C8	C^4	C8	C^4
C2	0	C6	C^3	C6	C^3
E3	0	C4	C^2	C4	C^2
D2	0	C2	C^1	C1	C^1
F6	0	C0	C^0	C0	C^0
D1	0	NC	-	H0	H^0
E2	0	NC	-	H4	H^2
E4	0	NC	-	F4	F^2
G5	0	NC	-	F6	F^3
E1	0	NC	-	F8	F^4
VCCO (Bank 0)	0	-	-	-	-
GND	0	-	-	-	-
F2	0	NC	-	F10	F^5
F1	0	NC	-	F12	F^6
G1	0	NC	-	F14	F^7
G6	0	NC	-	H8	H^4
G4	0	NC	-	H12	H^6
H6	0	D14	D^7	G14	G^7
G3	0	D12	D^6	G12	G^6
H5	0	D10	D^5	G10	G^5
G2	0	D8	D^4	G8	G^4
H1	0	D6	D^3	G6	G^3
H2	0	D4	D^2	G4	G^2
H3	0	D2	D^1	G2	G^1
H4	0	D0	D^0	G0	G^0
VCCO (Bank 0)	0	-	-	-	-
GND	0	-	-	-	-
J4	0	E0	E^0	J0	J^0
J3	0	E2	E^1	J2	J^1
J2	0	E4	E^2	J4	J^2
J1	0	E6	E^3	J6	J^3
K1	0	E8	E^4	J8	J^4
J5	0	E10	E^5	J10	J^5
K2	0	E12	E^6	J12	J^6
J6	0	E14	E^7	J14	J^7
K3	0	NC	-	I0	I^0

ispMACH 4256B/C, 4512B/C Logic Signal Connections: 256 fpBGA (Cont.)

BGA Ball Number	Bank Number	ispMACH 4256B/C		ispMACH 4512B/C	
		GLB	ORP	GLB	ORP
K4	0	NC	-	I4	I^2
L1	0	NC	-	K0	K^0
L2	0	NC	-	K2	K^1
M1	0	NC	-	K4	K^2
GND	-	-	-	-	-
VCCO (Bank 0)	0	-	-	-	-
M2	0	NC	-	K6	K^3
N1	0	NC	-	K8	K^4
M3	0	NC	-	K10	K^5
M4	0	NC	-	I8	I^4
N2	0	NC	-	I12	I^6
K5	0	F0	F^0	N0	N^0
P1	0	F2	F^1	N2	N^1
K6	0	F4	F^2	N4	N^2
N3	0	F6	F^3	N6	N^3
L5	0	F8	F^4	N8	N^4
P2	0	F10	F^5	N10	N^5
L6	0	F12	F^6	N12	N^6
R1	0	F14	F^7	N14	N^7
VCCO (Bank 0)	0	-	-	-	-
P3	0	TCK	-	TCK	-
VCC	-	-	-	-	-
GND	-	-	-	-	-
T2	0	NC	-	K12	K^6
M5	0	NC	-	K14	K^7
N4	0	G14	G^7	O14	O^7
T3	0	G12	G^6	O12	O^6
R3	0	G10	G^5	O10	O^5
M6	0	G8	G^4	O8	O^4
P4	0	G6	G^3	O6	O^3
L7	0	G4	G^2	O4	O^2
N5	0	G2	G^1	O2	O^1
M7	0	G0	G^0	O0	O^0
P5	0	NC	-	M0	M^0
R4	0	NC	-	M4	M^2
T4	0	NC	-	L0	L^0
GND	-	-	-	-	-
VCCO (Bank 0)	0	-	-	-	-
R5	0	NC	-	L4	L^2
T5	0	NC	-	L8	L^4
R6	0	NC	-	L12	L^6
T6	0	NC	-	M8	M^4
N7	0	NC	-	M12	M^6

ispMACH 4256B/C, 4512B/C Logic Signal Connections: 256 fpBGA (Cont.)

BGA Ball Number	Bank Number	ispMACH 4256B/C		ispMACH 4512B/C	
		GLB	ORP	GLB	ORP
P7	0	H14	H^7	P14	P^7
R7	0	H12	H^6	P12	P^6
L8	0	H10	H^5	P10	P^5
T7	0	H8	H^4	P8	P^4
M8	0	H6	H^3	P6	P^3
N8	0	H4	H^2	P4	P^2
R8	0	H2	H^1	P2	P^1
P8	0	H0	H^0	P0	P^0
GND	-	-	-	-	-
T8	0	CLK1/I	-	CLK1/I	-
GND	-	-	-	-	-
N9	1	CLK2/I	-	CLK2/I	-
VCC	-	-	-	-	-
P9	1	I0	I^0	AX0	AX^0
R9	1	I2	I^1	AX2	AX^1
T9	1	I4	I^2	AX4	AX^2
T10	1	I6	I^3	AX6	AX^3
R10	1	I8	I^4	AX8	AX^4
M9	1	I10	I^5	AX10	AX^5
P10	1	I12	I^6	AX12	AX^6
L9	1	I14	I^7	AX14	AX^7
N10	1	NC	-	DX0	DX^0
T11	1	NC	-	DX4	DX^2
R11	1	NC	-	EX0	EX^0
T12	1	NC	-	EX4	EX^2
N12	1	NC	-	EX8	EX^4
VCCO (Bank 1)	1	-	-	-	-
GND	-	-	-	-	-
R12	1	NC	-	EX12	EX^6
T13	1	NC	-	DX8	DX^4
P12	1	NC	-	DX12	DX^6
M10	1	J0	J^0	BX0	BX^0
R13	1	J2	J^1	BX2	BX^1
L10	1	J4	J^2	BX4	BX^2
T14	1	J6	J^3	BX6	BX^3
M11	1	J8	J^4	BX8	BX^4
R14	1	J10	J^5	BX10	BX^5
P13	1	J12	J^6	BX12	BX^6
N13	1	J14	J^7	BX14	BX^7
M12	1	NC	-	FX0	FX^0
T15	1	NC	-	FX2	FX^1
VCC	-	-	-	-	-
GND	-	-	-	-	-

ispMACH 4256B/C, 4512B/C Logic Signal Connections: 256 fpBGA (Cont.)

BGA Ball Number	Bank Number	ispMACH 4256B/C		ispMACH 4512B/C	
		GLB	ORP	GLB	ORP
GND	-	-	-	-	-
P14	1	TMS	-	TMS	-
VCCO (Bank 1)	1	-	-	-	-
L12	1	NC	-	FX4	FX^2
R16	1	NC	-	FX6	FX^3
N14	1	NC	-	FX8	FX^4
P15	1	K14	K^7	CX14	CX^7
L11	1	K12	K^6	CX12	CX^6
P16	1	K10	K^5	CX10	CX^5
K11	1	K8	K^4	CX8	CX^4
M14	1	K6	K^3	CX6	CX^3
K12	1	K4	K^2	CX4	CX^2
N15	1	K2	K^1	CX2	CX^1
N16	1	K0	K^0	CX0	CX^0
M15	1	NC	-	HX0	HX^0
M13	1	NC	-	HX4	HX^2
VCCO (Bank 1)	1	-	-	-	-
GND	-	-	-	-	-
M16	1	NC	-	FX10	FX^5
L15	1	NC	-	FX12	FX^6
L16	1	NC	-	FX14	FX^7
J11	1	NC	-	HX8	HX^4
K15	1	NC	-	HX12	HX^6
J12	1	L14	L^7	GX14	GX^7
K13	1	L12	L^6	GX12	GX^6
K14	1	L10	L^5	GX10	GX^5
K16	1	L8	L^4	GX8	GX^4
J16	1	L6	L^3	GX6	GX^3
J15	1	L4	L^2	GX4	GX^2
H16	1	L2	L^1	GX2	GX^1
J13	1	L0	L^0	GX0	GX^0
VCCO (Bank 1)	1	-	-	-	-
GND	1	-	-	-	-
J14	1	M0	M^0	JX0	JX^0
H15	1	M2	M^1	JX2	JX^1
H14	1	M4	M^2	JX4	JX^2
H13	1	M6	M^3	JX6	JX^3
G16	1	M8	M^4	JX8	JX^4
H12	1	M10	M^5	JX10	JX^5
G15	1	M12	M^6	JX12	JX^6
H11	1	M14	M^7	JX14	JX^7
F16	1	NC	-	IX0	IX^0
G13	1	NC	-	IX4	IX^2

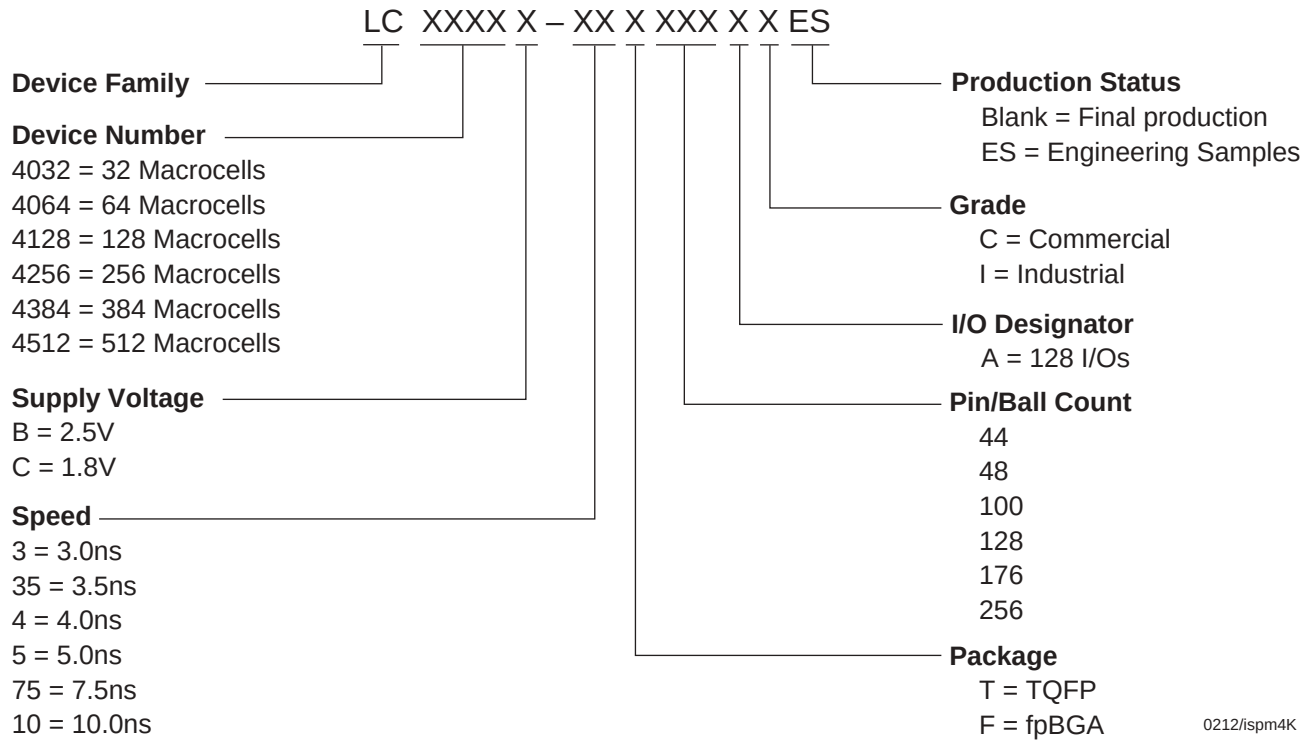
ispMACH 4256B/C, 4512B/C Logic Signal Connections: 256 fpBGA (Cont.)

BGA Ball Number	Bank Number	ispMACH 4256B/C		ispMACH 4512B/C	
		GLB	ORP	GLB	ORP
G14	1	NC	-	KX0	KX^0
F15	1	NC	-	KX2	KX^1
E16	1	NC	-	KX4	KX^2
GND	-	-	-	-	-
VCCO (Bank 1)	1	-	-	-	-
E15	1	NC	-	KX6	KX^3
G12	1	NC	-	KX8	KX^4
E13	1	NC	-	KX10	KX^5
D16	1	NC	-	IX8	IX^4
E14	1	NC	-	IX12	IX^6
G11	1	N0	N^0	NX0	NX^0
D15	1	N2	N^1	NX2	NX^1
F11	1	N4	N^2	NX4	NX^2
C16	1	N6	N^3	NX6	NX^3
F12	1	N8	N^4	NX8	NX^4
D14	1	N10	N^5	NX10	NX^5
C15	1	N12	N^6	NX12	NX^6
B16	1	N14	N^7	NX14	NX^7
VCCO (Bank 1)	1	-	-	-	-
C14	1	TDO	-	TDO	-
VCC	-	-	-	-	-
VCC	-	-	-	-	-
GND	-	-	-	-	-
A15	1	NC	-	KX12	KX^6
B14	1	NC	-	KX14	KX^7
E12	1	O14	O^7	OX14	OX^7
A14	1	O12	O^6	OX12	OX^6
C13	1	O10	O^5	OX10	OX^5
D13	1	O8	O^4	OX8	OX^4
E11	1	O6	O^3	OX6	OX^3
B13	1	O4	O^2	OX4	OX^2
F10	1	O2	O^1	OX2	OX^1
C12	1	O0	O^0	OX0	OX^0
E10	1	NC	-	MX0	MX^0
A13	1	NC	-	MX4	MX^2
D12	1	NC	-	LX0	LX^0
GND	-	-	-	-	-
VCCO (Bank 1)	1	-	-	-	-
B12	1	NC	-	LX4	LX^2
A12	1	NC	-	LX8	LX^4
B11	1	NC	-	LX12	LX^6
A11	1	NC	-	MX8	MX^4
D10	1	NC	-	MX12	MX^6

ispMACH 4256B/C, 4512B/C Logic Signal Connections: 256 fpBGA (Cont.)

BGA Ball Number	Bank Number	ispMACH 4256B/C		ispMACH 4512B/C	
		GLB	ORP	GLB	ORP
C10	1	P14	P^7	PX14	PX^7
B10	1	P12	P^6	PX12	PX^6
A10	1	P10	P^5	PX10	PX^5
A9	1	P8	P^4	PX8	PX^4
F9	1	P6	P^3	PX6	PX^3
B9	1	P4	P^2	PX4	PX^2
E9	1	P2/GOE1	P^1	PX2/GOE1	PX^1
C9	1	P0	P^0	PX0	PX^0
GND	-	-	-	-	-
D9	0	CLK3/I	-	CLK3/I	-
GND	-	-	-	-	-
B8	0	CLK0/I	-	CLK0/I	-
VCC	-	-	-	-	-
D8	0	A0	A^0	A0	A^0
C8	0	A2/GOE0	A^1	A2/GOE0	A^1
A8	0	A4	A^2	A4	A^2
A7	0	A6	A^3	A6	A^3
B7	0	A8	A^4	A8	A^4
E8	0	A10	A^5	A10	A^5
D7	0	A12	A^6	A12	A^6
F8	0	A14	A^7	A14	A^7
C7	0	NC	-	D0	D^0
A6	0	NC	-	D4	D^2
B6	0	NC	-	E0	E^0
A5	0	NC	-	E4	E^2
B5	0	NC	-	E8	E^4
VCCO (Bank 0)	0	-	-	-	-
GND	-	-	-	-	-
D5	0	NC	-	E12	E^6
A4	0	NC	-	D8	D^4
E7	0	NC	-	D12	D^6
A3	0	B0	B^0	B0	B^0
F7	0	B2	B^1	B2	B^1
B4	0	B4	B^2	B4	B^2
C5	0	B6	B^3	B6	B^3
A2	0	B8	B^4	B8	B^4
E6	0	B10	B^5	B10	B^5
B3	0	B12	B^6	B12	B^6
C4	0	B14	B^7	B14	B^7
D4	0	NC	-	F0	F^0
E5	0	NC	-	F2	F^1
VCC	-	-	-	-	-
GND	-	-	-	-	-

Part Number Description



Ordering Information

Commercial

Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256B-3T100C	256	2.5	3.0	TQFP	100	64	C
LC4256B-5T100C	256	2.5	5.0	TQFP	100	64	C
LC4256B-75T100C	256	2.5	7.5	TQFP	100	64	C
LC4256B-3T176C	256	2.5	3.0	TQFP	176	128	C
LC4256B-5T176C	256	2.5	5.0	TQFP	176	128	C
LC4256B-75T176C	256	2.5	7.5	TQFP	176	128	C
LC4256B-3F256AC	256	2.5	3.0	fpBGA	256	128	C
LC4256B-5F256AC	256	2.5	5.0	fpBGA	256	128	C
LC4256B-75F256AC	256	2.5	7.5	fpBGA	256	128	C
LC4256C-3T100C	256	1.8	3.0	TQFP	100	64	C
LC4256C-5T100C	256	1.8	5.0	TQFP	100	64	C
LC4256C-75T100C	256	1.8	7.5	TQFP	100	64	C
LC4256C-3T176C	256	1.8	3.0	TQFP	176	128	C
LC4256C-5T176C	256	1.8	5.0	TQFP	176	128	C
LC4256C-75T176C	256	1.8	7.5	TQFP	176	128	C
LC4256C-3F256AC	256	1.8	3.0	fpBGA	256	128	C
LC4256C-5F256AC	256	1.8	5.0	fpBGA	256	128	C
LC4256C-75F256AC	256	1.8	7.5	fpBGA	256	128	C

Commercial (Cont.)

Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4512B-35T176C	512	2.5	3.5	TQFP	176	128	C
LC4512B-5T176C	512	2.5	5.0	TQFP	176	128	C
LC4512B-75T176C	512	2.5	7.5	TQFP	176	128	C
LC4512B-35F256C	512	2.5	3.5	fpBGA	256	208	C
LC4512B-5F256C	512	2.5	5.0	fpBGA	256	208	C
LC4512B-75F256C	512	2.5	7.5	fpBGA	256	208	C
LC4512C-35T176C	512	1.8	3.5	TQFP	176	128	C
LC4512C-5T176C	512	1.8	5.0	TQFP	176	128	C
LC4512C-75T176C	512	1.8	7.5	TQFP	176	128	C
LC4512C-35F256C	512	1.8	3.5	fpBGA	256	208	C
LC4512C-5F256C	512	1.8	5.0	fpBGA	256	208	C
LC4512C-75F256C	512	1.8	7.5	fpBGA	256	208	C

Note: The speed grades for these devices are dual marked. For example, the commercial grade -3xxxxC is also marked with the industrial grade -5xxxxI. The commercial grade is always one speed grade faster than the associated dual mark industrial grade.

Industrial

Part Number	Macrocells	Voltage	T_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4256B-5T100I	256	2.5	5.0	TQFP	100	64	I
LC4256B-75T100I	256	2.5	7.5	TQFP	100	64	I
LC4256B-10T100I	256	2.5	10.0	TQFP	100	64	I
LC4256B-5T176I	256	2.5	5.0	TQFP	176	128	I
LC4256B-75T176I	256	2.5	7.5	TQFP	176	128	I
LC4256B-10T176I	256	2.5	10.0	TQFP	176	128	I
LC4256B-5F256AI	256	2.5	5.0	fpBGA	256	128	I
LC4256B-75F256AI	256	2.5	7.5	fpBGA	256	128	I
LC4256B-10F256AI	256	2.5	10.0	fpBGA	256	128	I
LC4256C-5T100I	256	1.8	5.0	TQFP	100	64	I
LC4256C-75T100I	256	1.8	7.5	TQFP	100	64	I
LC4256C-10T100I	256	1.8	10.0	TQFP	100	64	I
LC4256C-5T176I	256	1.8	5.0	TQFP	176	128	I
LC4256C-75T176I	256	1.8	7.5	TQFP	176	128	I
LC4256C-10T176I	256	1.8	10.0	TQFP	176	128	I
LC4256C-5F256AI	256	1.8	5.0	fpBGA	256	128	I
LC4256C-75F256AI	256	1.8	7.5	fpBGA	256	128	I
LC4256C-10F256AI	256	1.8	10.0	fpBGA	256	128	I

Industrial (Cont.)

Part Number	Macrocells	Voltage	T_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4512B-5T176I	512	2.5	5.0	TQFP	176	128	I
LC4512B-75T176I	512	2.5	7.5	TQFP	176	128	I
LC4512B-10T176I	512	2.5	10.0	TQFP	176	128	I
LC4512B-5F256I	512	2.5	5.0	fpBGA	256	208	I
LC4512B-75F256I	512	2.5	7.5	fpBGA	256	208	I
LC4512B-10F256I	512	2.5	10.0	fpBGA	256	208	I
LC4512C-5T176I	512	1.8	5.0	TQFP	176	128	I
LC4512C-75T176I	512	1.8	7.5	TQFP	176	128	I
LC4512C-10T176I	512	1.8	10.0	TQFP	176	128	I
LC4512C-5F256I	512	1.8	5.0	fpBGA	256	208	I
LC4512C-75F256I	512	1.8	7.5	fpBGA	256	208	I
LC4512C-10F256I	512	1.8	10.0	fpBGA	256	208	I

Note: The speed grades for these devices are dual marked. For example, the commercial grade -3xxxxC is also marked with the industrial grade -5xxxxI. The commercial grade is always one speed grade faster than the associated dual mark industrial grade.

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000B/C family:

- *ispMACH 4000 Timing Model Design and Usage Guidelines* (TN1004)
- *ispMACH 4000B/C Power Consumption* (TN1005)