



128Kx8 Monolithic SRAM, SMD 5962-89598

FEATURES

- Access Times of 15*, 17, 20, 25, 35, 45, 55ns
- Battery Back-up Operation
 - 2V Data Retention (EDI88130LPS)
- \overline{CS}_1 , CS_2 & \overline{OE} Functions for Bus Control
- Inputs and Outputs Directly TTL Compatible
- Organized as 128Kx8
- Commercial, Industrial and Military Temperature Ranges
- Thru-hole and Surface Mount Packages JEDEC Pinout
 - 32 pin Sidebraced Ceramic DIP, 400 mil (Package 102)
 - 32 pin Sidebraced Ceramic DIP, 600 mil (Package 9)
 - 32 lead Ceramic SOJ (Package 140)
 - 32 pad Ceramic Quad LCC (Package 12)
 - 32 pad Ceramic LCC (Package 141)
 - 32 lead Ceramic Flatpack (Package 142)
- Single +5V ($\pm 10\%$) Supply Operation

The EDI88130CS is a high speed, high performance, 128Kx8 bits monolithic Static RAM.

An additional chip enable line provides system memory security during power down in non-battery backed up systems and memory banking in high speed battery backed systems where large multiple pages of memory are required.

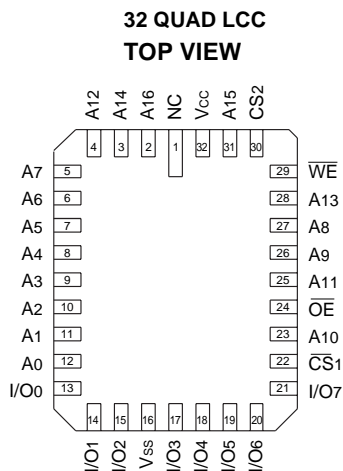
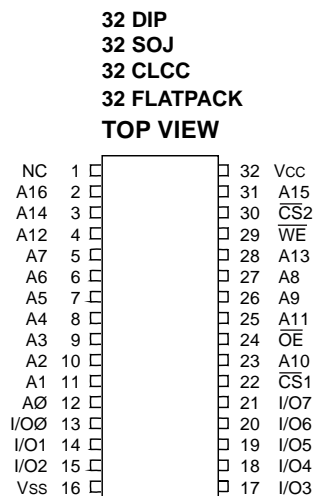
The EDI88130CS has eight bi-directional input-output lines to provide simultaneous access to all bits in a word.

A low power version, EDI88130LPS, offers a 2V data retention function for battery back-up applications.

Military product is available compliant to MIL-PRF-38535.

**15ns access time is advanced information, contact factory for availability.*

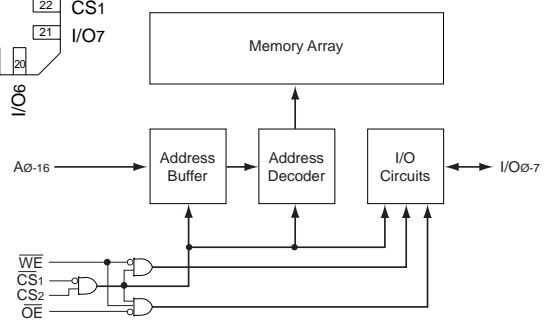
FIG. 1 PIN CONFIGURATION



PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-16	Address Inputs
\overline{WE}	Write Enable
\overline{CS}_1 , CS_2	Chip Selects
\overline{OE}	Output Enable
V _{CC}	Power (+5V $\pm 10\%$)
V _{SS}	Ground
NC	Not Connected

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to Vss	-0.2 to 7.0	V
Operating Temperature TA (Ambient)		
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Ceramic	-65 to +150	°C
Power Dissipation	1.7	W
Output Current	40	mA
Junction Temperature, TJ	175	°C

NOTE:

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	—	VCC +0.5	V
Input Low Voltage	VIL	-0.5	—	+0.8	V

DC CHARACTERISTICS

(VCC = 5V, TA = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Leakage Current	ILI	VIN = 0V to VCC	—	—	±5	µA
Output Leakage Current	ILO	VI/O = 0V to VCC	—	—	±10	µA
Operating Power Supply Current	ICC1	WE, CS1 = VIL, I/I/O = 0mA, CS2 = VIH (15-17ns)	—	—	300	mA
			—	—	225	mA
			—	—	200	mA
Standby (TTL) Power Supply Current	ICC2	CS1 ≥ VIH and/or CS2 ≤ VIL, VIN ≥ VIH or ≤ VIL (17-55ns)	—	—	25	mA
			—	—	60	mA
Full Standby Power Supply Current	ICC3	CS1 ≥ VCC -0.2V and/or CS2 ≤ 0.2V VIN ≥ VCC -0.2V or VIN ≤ 0.2V CS (17-55ns) CS (15ns) LPS	—	3	10	mA
			—	—	15	mA
			—	—	5	mA
Output Low Voltage	VOL	IOL = 8.0mA	—	—	0.4	V
Output High Voltage	VOH	IOH = -4.0mA	2.4	—	—	V

TRUTH TABLE

OE	CS1	CS2	WE	Mode	Output	Power
X	H	X	X	Standby	High Z	ICC2, ICC3
X	X	L	X	Standby	High Z	ICC2, ICC3
H	L	H	H	Output Deselect	High Z	ICC1
L	L	H	H	Read	Data Out	ICC1
X	L	H	L	Write	Data In	ICC1

CAPACITANCE

(TA = +25°C)

Parameter	Symbol	Condition	Max		Unit
			LCC	CSQJ,DIP, Flatpack	
Address Lines	CI	VIN = VCC or VSS, f = 1.0MHz	6	12	pF
Data Lines	CO	VOUT = VCC or VSS, f = 1.0MHz	8	14	pF

These parameters are sampled, not 100% tested.

AC TEST CONDITIONS

Figure 1

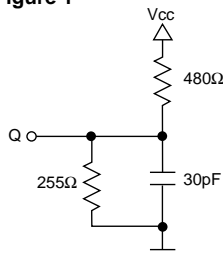
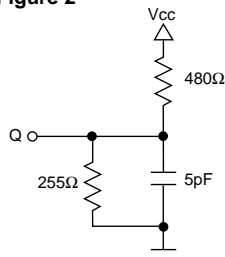


Figure 2



Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For tEH0Z, tGH0Z and tWL0Z, CL = 5pF Figure 2)



AC CHARACTERISTICS – READ CYCLE (15 to 20ns)

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		15ns*		17ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tAVAV	tRC	15		17		20		ns
Address Access Time	tAVQV	tAA		15		17		20	ns
Chip Enable Access Time	tE1LQV tE2HQV	tACS		15		17		20	ns
Chip Enable to Output in Low Z (1)	tE1LOX tE2HOX	tCLZ tCLZ	5 5		5 5		5 5		ns ns
Chip Disable to Output in Low Z (1)	tE1HQZ tE2LQZ	tCHZ tCHZ		6 6		7 7		8 8	ns ns
Output Hold from Address Change	tAVQX	tOH	3		3		3		ns
Output Enable to Output Valid	tGLQV	tOE		6		6		7	ns
Output Enable to Output in Low Z (1)	tGLQX	tOLZ	0		0		0		ns
Output Disable to Output in High Z(1)	tGHQZ	tOHZ		5		6		8	ns
Chip Enable to Power Up (1)	tE1LICCH tE2HICCH	tPU tPU	0 0		0 0		0 0		ns ns
Chip Enable to Power Down (1)	tE1HICCL tE2LICCL	tPD tPD		15		17		20	ns

1. This parameter is guaranteed by design but not tested.

* 15ns access time is advanced information, contact factory for availability.

AC CHARACTERISTICS – READ CYCLE (25 to 55ns)

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		25ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tAVAV	tRC	25		35		45		55		ns
Address Access Time	tAVQV	tAA		25		35		45		55	ns
Chip Enable Access Time	tE1LQV	tACS		25		35		45		55	ns
Chip Enable Access Time	tE2HQV	tACS		25		35		45		55	ns
Chip Enable to Output in Low Z (1)	tE1LOX tE2HOX	tCLZ tCLZ	5 5		5 5		5 5		5 5		ns ns
Chip Disable to Output in Low Z (1)	tE1HQZ tE2LQZ	tCHZ tCHZ		10 10		15 15		20 20		20 20	ns ns
Output Hold from Address Change	tAVQX	tOH	0		0		0		0		ns
Output Enable to Output Valid	tGLQV	tOE		10		15		20		25	ns
Output Enable to Output in Low Z (1)	tGLQX	tOLZ	0		0		0		0		ns
Output Disable to Output in High Z(1)	tGHQZ	tOHZ		10		15		20		20	ns
Chip Enable to Power Up (1)	tE1LICCH tE2HICCH	tPU tPU	0 0		0 0		0 0		0 0		ns ns
Chip Enable to Power Down (1)	tE1HICCL tE2LICCL	tPD tPD		25		35		45		55	ns

1. This parameter is guaranteed by design but not tested.



AC CHARACTERISTICS – WRITE CYCLE (15 to 20ns)

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol		15ns*		17ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	15		17		20		ns
Chip Enable to End of Write	tE1LWH	tCW	12		13		15		ns
	tE1LE1H	tCW	12		13		15		ns
	tE2HWH	tCW	12		13		15		ns
	tE2HE2L	tCW	12		13		15		ns
Address Setup Time	tAVWL	tAS	0		0		0		ns
	tAVE1L	tAS	0		0		0		ns
	tAVE2H	tAS	0		0		0		ns
Address Valid to End of Write	tAVWH	tAW	12		13		15		ns
Write Pulse Width	tWLWH	tWP	12		13		15		ns
	tWLE1H	tWP	12		13		15		ns
	tWLE2L	tWP	12		13		15		ns
Write Recovery Time	tWHAX	tWR	0		0		0		ns
	tE1HAX	tWR	0		0		0		ns
	tE2LAX	tWR	0		0		0		ns
Data Hold Time	tWHDX	tDH	0		0		0		ns
	tE1HDX	tDH	0		0		0		ns
	tE2LDX	tDH	0		0		0		ns
Write to Output in High Z (1)	tWLQZ	tWHZ	0	7	0	8	0	8	ns
Data to Write Time	tDVWH	tDW	7		8		10		ns
	tDVE1H	tDW	7		8		10		ns
	tDVE2L	tDW	7		8		10		ns
Output Active from End of Write (1)	tWHQX	tWLZ	3		3		3		ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE CYCLE (25 to 55ns)

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol		25ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	25		35		45		55		ns
Chip Enable to End of Write	tE1LWH	tCW	20		25		35		45		ns
	tE1LE1H	tCW		16		20		25		40	ns
	tE2HWH	tCW	16		20		25		40		ns
	tE2HE2L	tCW		16		20		25		40	ns
Address Setup Time	tAVWL	tAS	0		0		0		0		ns
	tAVE1L	tAS	0		0		0		0		ns
	tAVE2H	tAS	0		0		0		0		ns
Address Valid to End of Write	tAVWH	tAW	20		25		35		45		ns
	tAVEH	tAW	20		25		35		45		ns
Write Pulse Width	tWLWH	tWP	20		30		30		35		ns
	tWLE1H	tWP	20		30		30		35		ns
	tWLE2L	tWP	20		30		30		35		ns
Write Recovery Time	tWHAX	tWR	0		0		5		5		ns
	tE1HAX	tWR	0		0		5		5		ns
	tE2LAX	tWR	0		0		5		5		ns
Data Hold Time	tWHDX	tDH	0		0		0		0		ns
	tE1HDX	tDH	0		0		0		0		ns
	tE2LDX	tDH	0		0		0		0		ns
Write to Output in High Z (1)	tWLQZ	tWHZ	0	10	0	13	0	15	0	20	ns
Data to Write Time	tDVWH	tDW	15		20		20		25		ns
	tDVE1H	tDW	15		20		20		25		ns
	tDVE2L	tDW	15		20		20		25		ns
Output Active from End of Write (1)	tWHQX	tWLZ	3		3		3		3		ns

1. This parameter is guaranteed by design but not tested.



FIG. 2 TIMING WAVEFORM - READ CYCLES

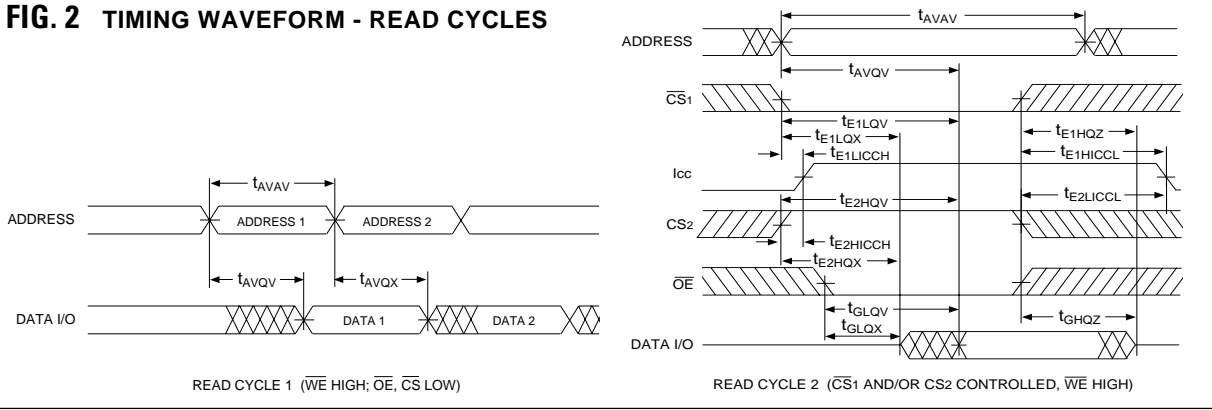


FIG. 3 WRITE CYCLE 1

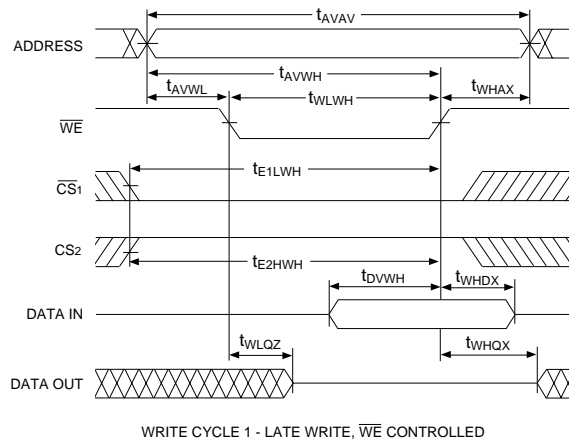
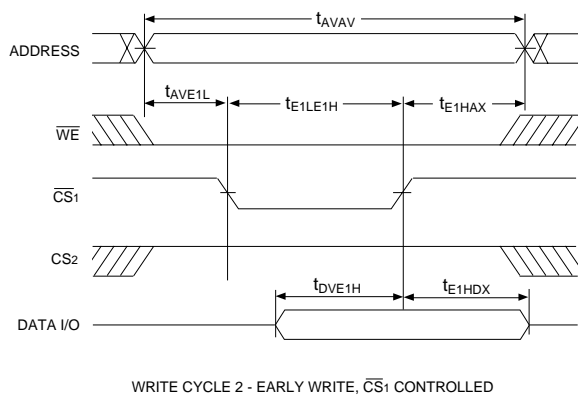
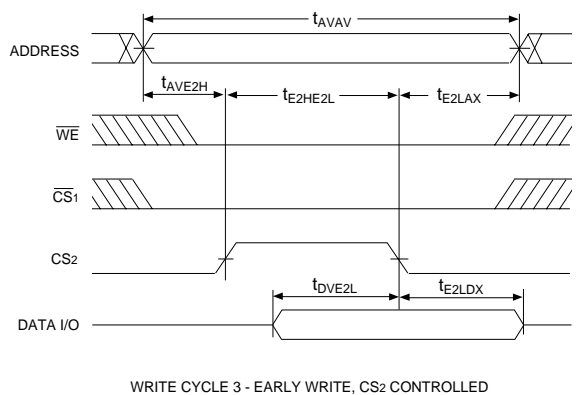


FIG. 4 WRITE CYCLES 2



WRITE CYCLES 3





DATA RETENTION CHARACTERISTICS (EDI88130LPS ONLY)

(TA = -55°C to +125°C)

Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V _{DD}	V _{DD} = 2.0V	2	-	-	V
Data Retention Quiescent Current	I _{CCDR}	$\overline{CS}_1 \geq V_{DD} - 0.2V$ and/or $CS_2 \geq V_{SS} + 0.2V$	-	0.5	2	mA
Chip Disable to Data Retention Time (1)	T _{CDR}	V _{IN} ≥ V _{DD} - 0.2V	0	-	-	ns
Operation Recovery Time (1)	T _R	or V _{IN} ≤ 0.2V	T _{AVAV} *	-	-	ns

NOTE:

1. Parameter guaranteed by design, but not tested.

* Read Cycle Time

FIG. 5 DATA RETENTION - \overline{CS}_1 CONTROLLED

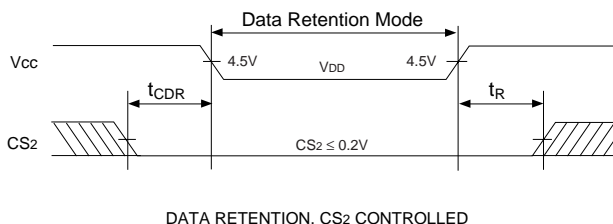
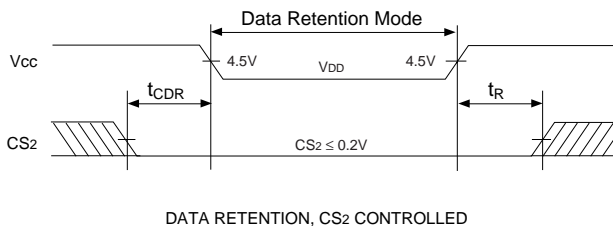
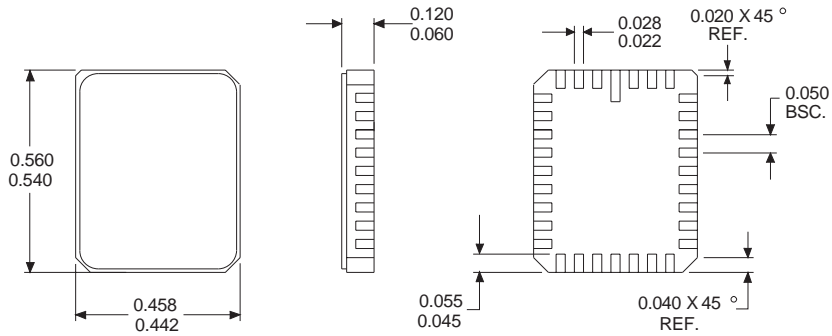


FIG. 6 DATA RETENTION - CS₂ CONTROLLED



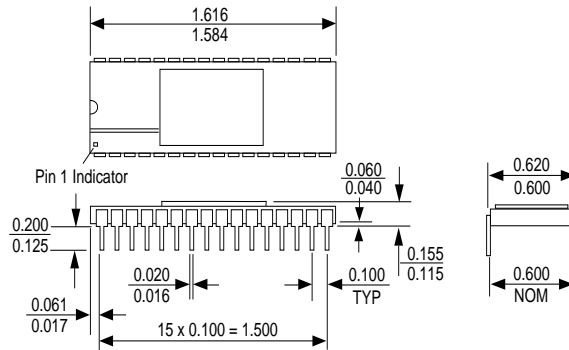


PACKAGE 12: 32 PIN CERAMIC QUAD LCC



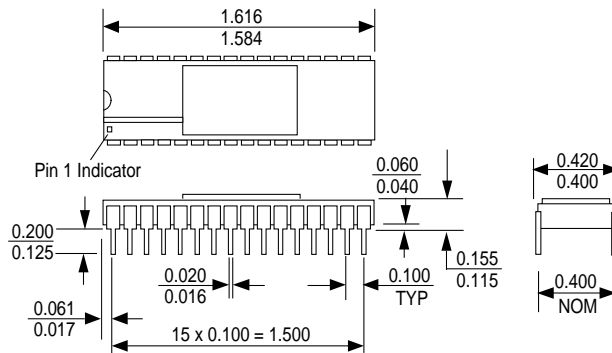
ALL DIMENSIONS ARE IN INCHES

PACKAGE 9: 32 PIN SIDEBRAZED CERAMIC DIP (600 mils wide)



ALL DIMENSIONS ARE IN INCHES

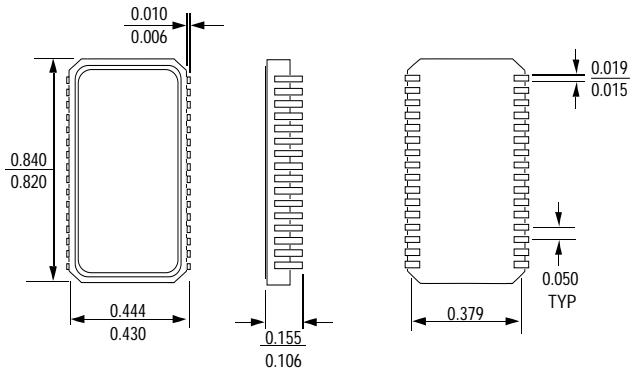
PACKAGE 102: 32 PIN SIDEBRAZED CERAMIC DIP (400 mils wide)



ALL DIMENSIONS ARE IN INCHES

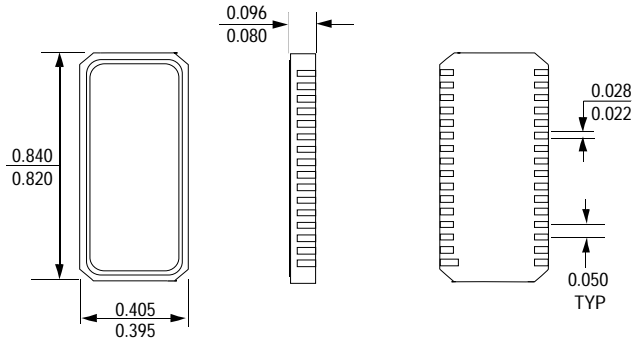


PACKAGE 140: 32 LEAD CERAMIC SOJ



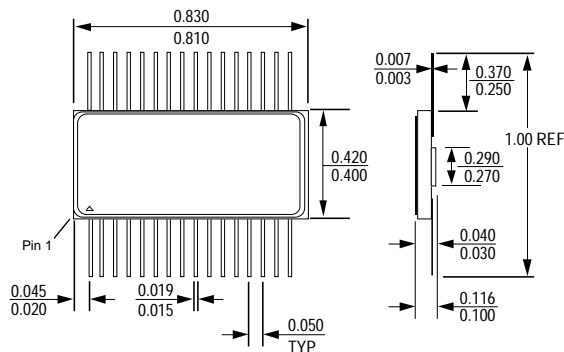
ALL DIMENSIONS ARE IN INCHES

PACKAGE 141: 32 PAD CERAMIC LCC



ALL DIMENSIONS ARE IN INCHES

PACKAGE 142: 32 PIN CERAMIC FLATPACK



ALL DIMENSIONS ARE IN INCHES



ORDERING INFORMATION

EDI 8 8 130 CS X X X

WHITE ELECTRONIC DESIGNS _____

SRAM _____

ORGANIZATION, 128Kx8 _____
(130 = Dual CS)

TECHNOLOGY: _____
CS = CMOS Standard Power (5V)
LPS = Low Power

ACCESS TIME (ns) _____

PACKAGE TYPE: _____
C = 32 lead Sidebrazed DIP, 600 mil (Package 9)
F = 32 lead Ceramic Flatpack (Package 142)
L = 32 pad Ceramic LCC (Package 141)
L32 = 32 pad Ceramic Quad LCC (Package 12)
N = 32 lead Ceramic SOJ (Package 140)
T = 32 lead Sidebrazed DIP, 400 mil (Package 102)

DEVICE GRADE: _____
B = MIL-STD-883 Compliant
M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C