WHITE ELECTRONIC DESIGNS

512Kx8 STATIC RAM CMOS, MODULE

FEATURES

- 512Kx8 bit CMOS Static
- Random Access Memory
  - Access Times 20 through 100ns
  - Data Retention Function (EDI8F8512LP)
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- High Density Packaging
  - 36 Pin SIP, No. 63
  - 32 Pin DIP, JEDEC Pinout, No. 91 (55-100ns)
  - 32 Pin DIP, JEDEC Pinout, No. 183 (20-35ns)
- Single +5V (±10%) Supply Operation

DESCRIPTION

The EDI8F8512C is a 4096K bit CMOS Static RAM based on four 128Kx8 or 256Kx4 (high speed) Static RAMs mounted on a multi-layered epoxy laminate (FR4) substrate.

Functional equivalence to the monolithic four megabit Static RAM is achieved by utilization of an on-board decoder that interprets the higher order address(es) to select one of the128Kx8 or 256Kx4 Static RAMs.

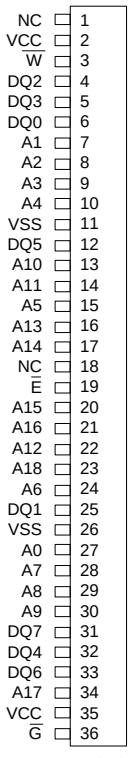
The 32 pin DIP pinout adheres to the JEDEC standard for the four megabit device, to ensure compatibility with future monolithics.

A low power version with data retention (EDI8F8512LP) is also available.

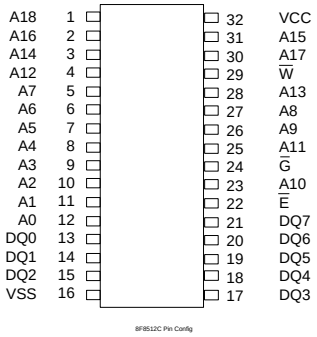
All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8F8512C requires no clocks or refreshing for operation.

FIG. 1

PIN CONFIGURATIONS AND BLOCK DIAGRAM

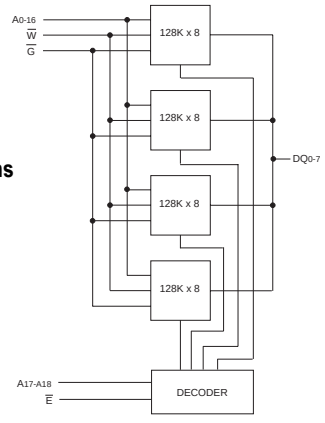


8F8512C Pin Config.



8F8512C Pin Config

55-100ns

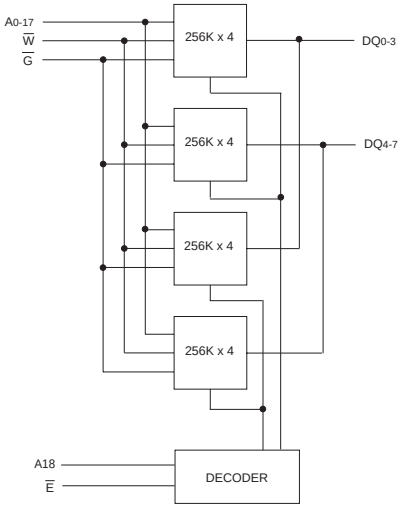


8F8512C Blk Dia

PIN NAMES

AØ-A18	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

20-35ns



8F8512C Blk Dia2

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	4 Watts
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC TEST CONDITIONS

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load 20-35ns	1TTL = 30pF
70-100ns	1TTL, CL =100pF

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions		Min	Typ*		Max			Units
					≤35	≥55	20-25	35	55-100	ns
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle		–	340	70	570	390	130	mA
Standby (TTL) Power	ICC2	$\overline{E}$ ≥ VIH, VIN - VIL	DIP	–	50	10	85	85	55	mA
Supply Current		VIN ≥ VIH	SIP	–	–	–	–	–	65	mA
Full Standby Power	ICC3	$\overline{E}$ ≥ VCC-0.2V	C	–	5	2	40	40	5	mA
Supply Current (CMOS)		VIN ≥ VCC-0.2V or VIN ≤ 0.2V	LP	–	–	40	–	–	400	µA
Input Leakage Current	ILI	VIN = 0V to VCC		–	–	–	±10	±10	±10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		–	–	–	±10	±10	±10	µA
Output High Voltage	VOH	IOH=-1.0mA (≥70),or -4.0(≤35)		2.4	–	–	–	–	–	V
Output Low Voltage	VOL	IOL = 2.1mA (≥70),or 8.0mA(≤35)		–	–	–	0.4	0.4	0.4	V

*Typical: TA=25°C, VCC=5.0V

TRUTH TABLE

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

CAPACITANCE

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	30	pF
Data Lines	CD/Q	43	pF
Chip Enable Line	CC	10	pF
Write and Output Enable Lines	CW	32	pF

These parameters are sampled, not 100% tested.

AC CHARACTERISTICS READ CYCLE

	Symbol		20ns		25ns		35ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	20		25		35		ns
Address Access Time	TAVQV	TAA		20		25		35	ns
Chip Enable Access Time	TELQV	TACS		20		25		35	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		10		12		15	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		13		15		20	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		8		10		12	ns

Note 1: Parameter guaranteed, but not tested.

FIG. 2

READ CYCLE 1 - $\overline{W}$ HIGH, $\overline{G}$, $\overline{E}$ LOW

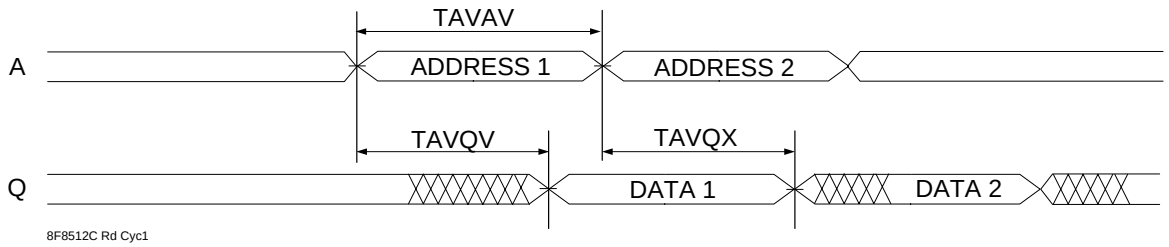
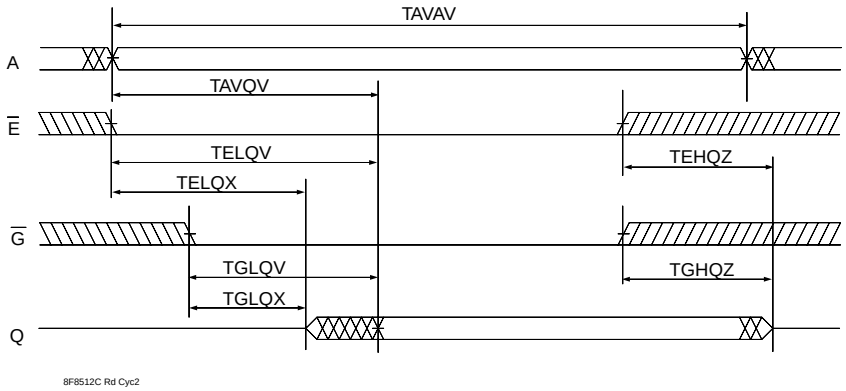


FIG. 3

READ CYCLE 2 - $\overline{W}$ HIGH



AC CHARACTERISTICS READ CYCLE

Parameter	Symbol JEDEC	Symbol Alt.	55ns Min	55ns Max	70ns Min	70ns Max	85ns Min	85ns Max	100ns Min	100ns Max	Units
Read Cycle Time	TAVAV	TRC	55		70		85		100		ns
Address Access Time	TAVQV	TAA		55		70		85		100	ns
Chip Enable Access Time	TELQV	TACS		55		70		85		100	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	5		5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		30		30		35		40	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		40		40		45		50	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		30		30		35		40	ns

Note 1: Parameter guaranteed, but not tested.

AC CHARACTERISTICS WRITE CYCLE

Write Cycle Parameter	Symbol JEDEC	Symbol Alt	20ns Min	20ns Max	25ns Min	25ns Max	35ns Min	35ns Max	Units
Write Cycle Time	TAVAV	TWC	20		25		35		ns
Chip Enable to End of Write	TELWH	TCW	15		20		30		ns
	TELEH	TCW	15		20		30		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	15		20		30		ns
	TAVEH	TAW	15		20		30		ns
Write Pulse Width	TWLWH	TWP	15		20		25		ns
	TWLEH	TWP	15		20		25		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time	TWHDX	TDH	3		3		3		ns
	TEHDX	TDH	3		3		3		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	10	0	12	0	15	ns
Data to Write Time	TDVWH	TDW	12		15		20		ns
	TDVEH	TDW	12		15		20		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

AC CHARACTERISTICS WRITE CYCLE

Parameter	Symbol JEDEC	Symbol Alt.	55NS Min	55NS Max	70ns Min	70ns Max	85n Min	85n Max	100ns Min	100ns Max	Units
Write Cycle Time	TAVAV	TWC	55		70		85		100		ns
Chip Enable to End of Write	TELWH	TCW	50		65		70		80		ns
	TELEH	TCW	50		65		70		80		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	50		65		70		80		ns
	TAVEH	TAW	50		65		70		80		ns
Write Pulse Width	TWLWH	TWP	50		65		70		80		ns
	TWLEH	TWP	50		65		70		80		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		0		ns
	TEHDX	TDH	0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	30	0	30	0	35	0	40	ns
Data to Write Time	TDVWH	TDW	30		30		35		40		ns
	TDVEH	TDW	30		30		35		40		ns
Output Active from End of Write (1)	TWHQX	TWLZ	5		5		5		5		ns

Note 1: Parameter guaranteed, but not tested.

FIG. 6

WRITE CYCLE 1 - $\overline{W}$ CONTROLLED

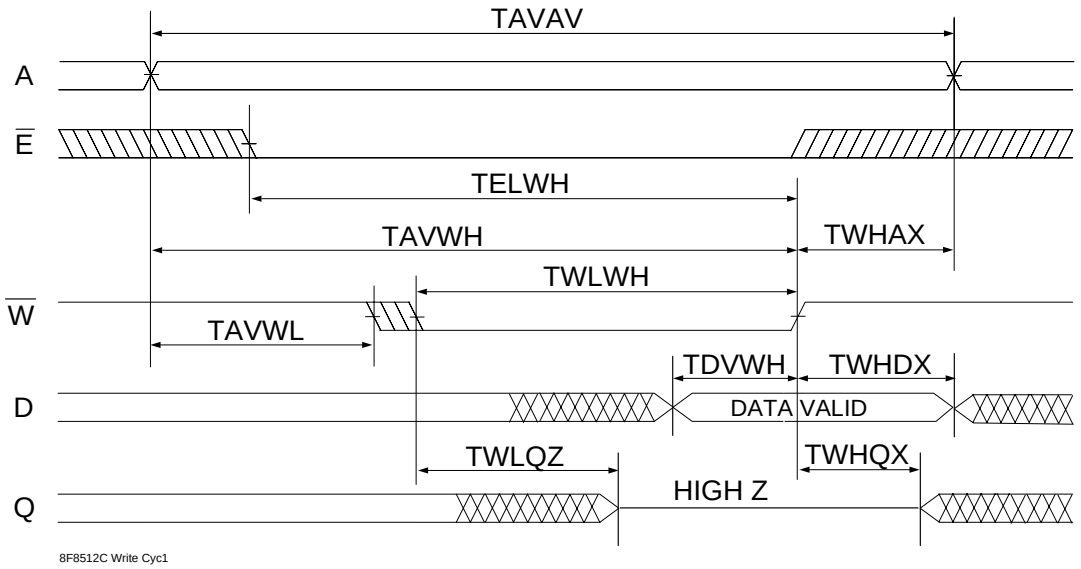
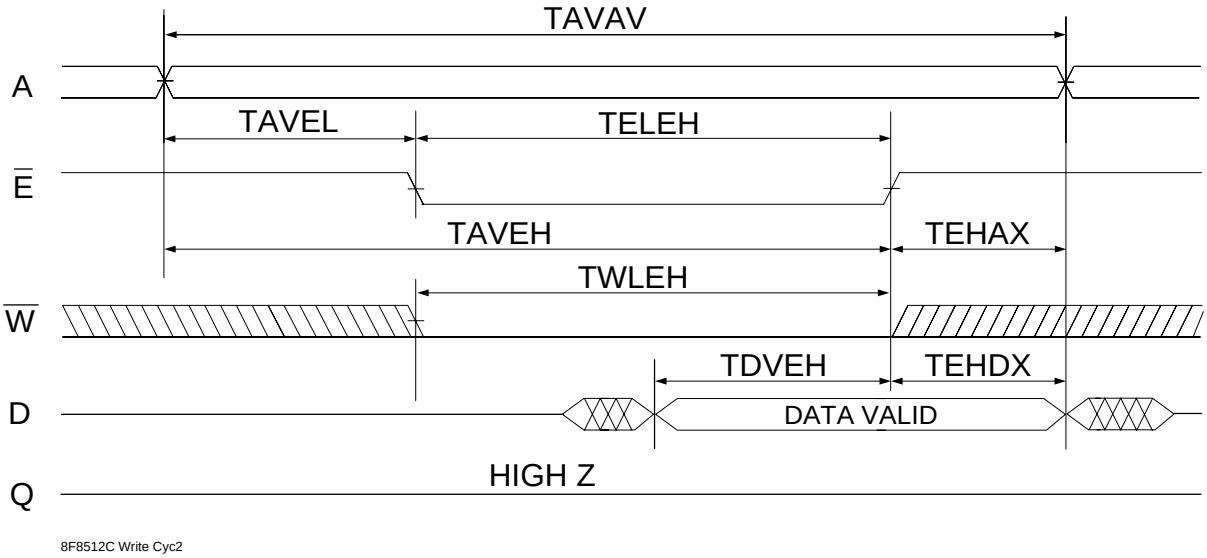


FIG. 7

WRITE CYCLE 2 - $\overline{E}$ CONTROLLED



DATA RETENTION CHARACTERISTICS

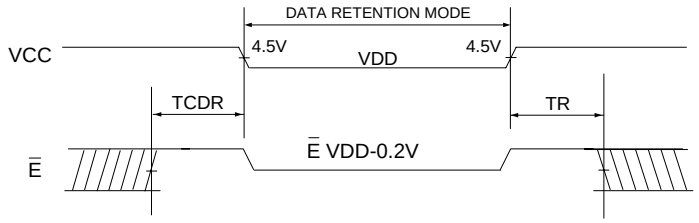
LP 70-100ns Only

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max		Unit
						70°C	85°C	
Data Retention Voltage	VDD	VDD = 0.2V		2	–	–	–	V
Data Retention Quiescent Current	ICCDR	$\overline{E} \geq$ VDD -0.2V	2V	–	10	125	185	µA
		VIN $\geq$ VDD -0.2V	3V	–	20	200	250	µA
Chip Disable to Data Retention Time (1)	TCDR	or VIN $\leq$ 0.2V		0	–	–	–	ns
Operation Recovery Time (1)	TR			TAVAV*	–	–	–	ns

*Read Cycle Time
Note 1: Parameter guaranteed, but not tested.

FIG. 8

DATA RETENTION $\overline{E}$ CONTROLLED



8F8512C Data Retent.

ORDERING INFORMATION

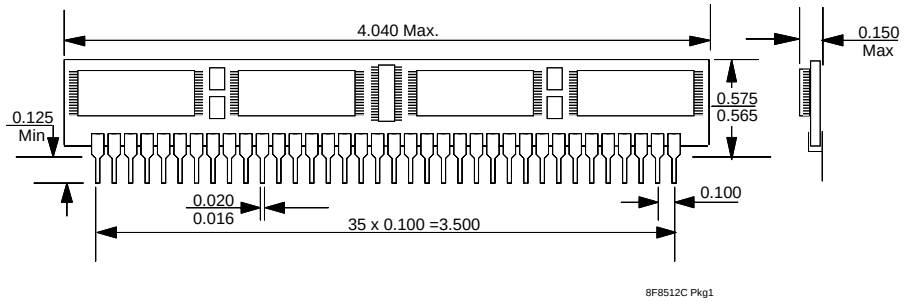
Standard Power	Speed (ns)	Package No.
EDI8F8512C20M6C	20	183
EDI8F8512C25M6C	25	183
EDI8F8512C35M6C	35	183
EDI8F8512C70BSC	70	63
EDI8F8512C85BSC	85	63
EDI8F8512C100BSC	100	63
EDI8F8512C55B6C	55	91
EDI8F8512C70B6C	70	91
EDI8F8512C85B6C	85	91
EDI8F8512C100B6C	100	91

Low Power with Data Retention	Speed (ns)	Package Leads
EDI8F8512LP70BSC	70	63
EDI8F8512LP85BSC	85	63
EDI8F8512LP100BSC	100	63
EDI8F8512LP70B6C	70	91
EDI8F8512LP85B6C	85	91
EDI8F8512LP100B6C	100	91

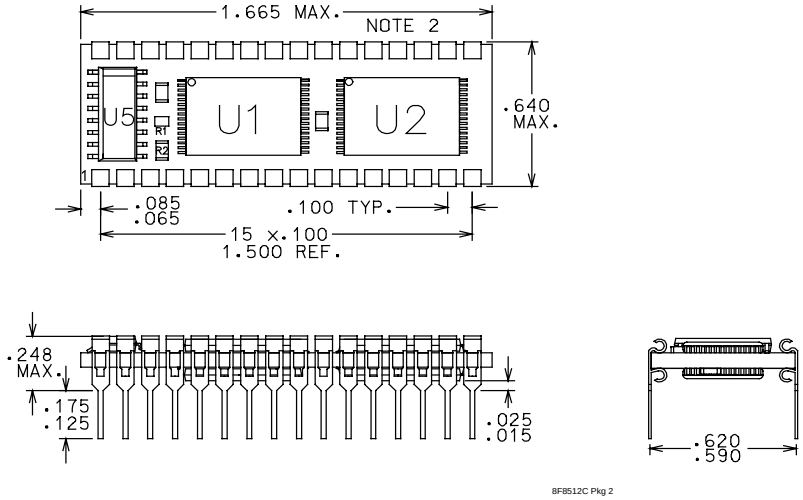
Note:
To order an Industrial grade product substitute the letter C in the Suffix with the letter I, eg. EDI8F8512C70B6C becomes EDI8F8512C70B6I.

PACKAGE DESCRIPTION

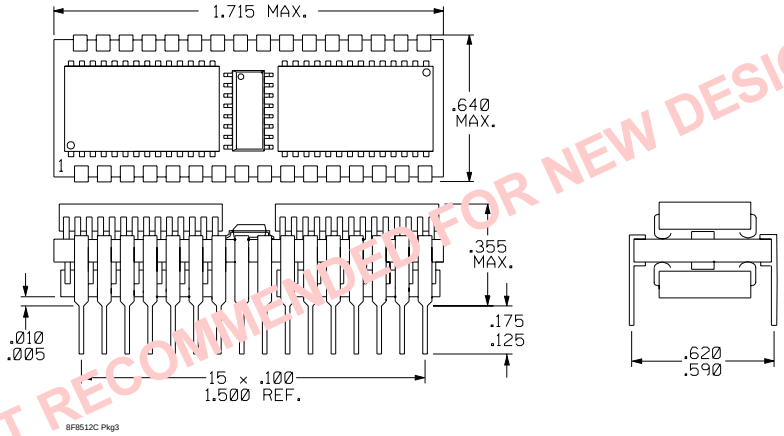
PACKAGE NO. 63: 36 PIN SINGLE-IN-LINE PACKAGE



PACKAGE NO. 91: 32 PIN DUAL-IN-LINE PACKAGE



PACKAGE NO. 183: 32 PIN DUAL-IN-LINE PACKAGE



ALL DIMENSIONS ARE IN INCHES