FAIRCHILD SEMICONDUCTOR®

September 2001

Si6435DQ

30V P-Channel PowerTrench® MOSFET

General Description

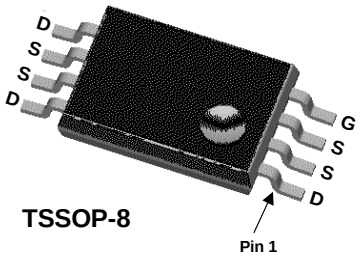
This P-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5V – 20V).

Applications

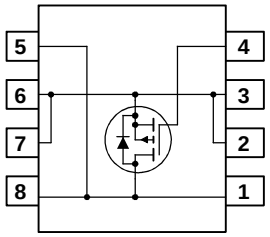
- Battery protection
- DC/DC conversion
- Power management
- Load switch

Features

- –4.5 A, –30 V $R_{DS(ON)}$ = 40 mΩ @ V_{GS} = –10 V
  $R_{DS(ON)}$ = 70 mΩ @ V_{GS} = –4.5 V
- Extended V_{GSS} range (±20V) for battery applications
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low profile TSSOP-8 package



TSSOP-8



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		–30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current – Continuous	(Note 1)	–4.5	A
	– Pulsed		–30	
P_D	Power Dissipation	(Note 1a)	1.3	W
		(Note 1b)	0.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	87	°C/W
		(Note 1b)	114	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
6435	Si6435DQ	13''	16mm	3000 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 µA	–30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		–23		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –24 V, V_{GS} = 0 V			–1	µA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –20 V, V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA	–1	–1.7	–3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		5		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –10 V, I_D = –4.5 A V_{GS} = –4.5 V, I_D = –3.4 A V_{GS}= –10 V, I_D = –4.5A, T_J=125°C		27 42 38	40 70 60	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = –10 V, V_{DS} = –5 V	–30			A
g_{FS}	Forward Transconductance	V_{DS} = –15 V, I_D = –4.5 A		12		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –15 V, V_{GS} = 0 V, f = 1.0 MHz		854		pF
C_{oss}	Output Capacitance			215		pF
C_{rss}	Reverse Transfer Capacitance			112		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –15 V, I_D = –1 A, V_{GS} = –10 V, R_{GEN} = 6 Ω		9	20	ns
t_r	Turn–On Rise Time			14	20	ns
$t_{d(off)}$	Turn–Off Delay Time			29	55	ns
t_f	Turn–Off Fall Time			15	25	ns
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = –1.25 A, dI_F/dt = 100A/µs		19	80	ns
Q_g	Total Gate Charge	V_{DS} = –15 V, I_D = –4.5 A, V_{GS} = –10 V		15	35	nC
Q_{gs}	Gate–Source Charge			2.4		nC
Q_{gd}	Gate–Drain Charge			3		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–1.25	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –1.25 A (Note 2)		–0.75	–1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $R_{\theta JA}$ is 87 °C/W (steady state) when mounted on a 1 inch² copper pad on FR-4.

b) $R_{\theta JA}$ is 114 °C/W (steady state) when mounted on a minimum copper pad on FR-4.

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

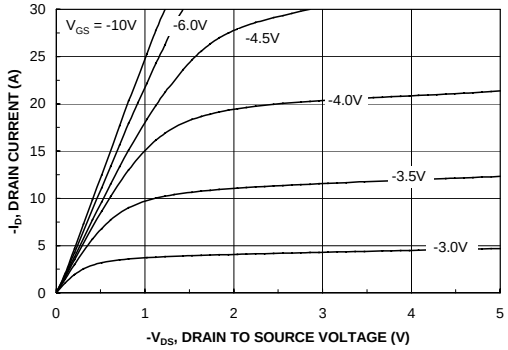


Figure 1. On-Region Characteristics.

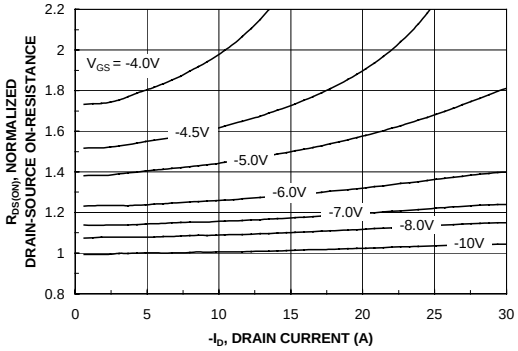


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

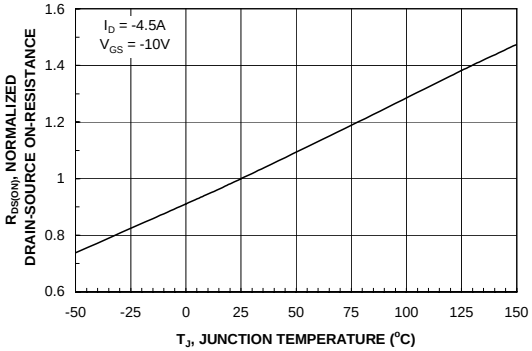


Figure 3. On-Resistance Variation with Temperature.

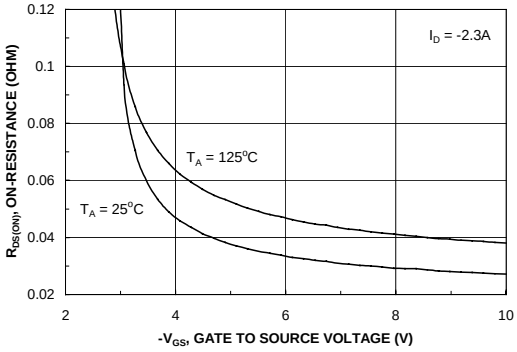


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

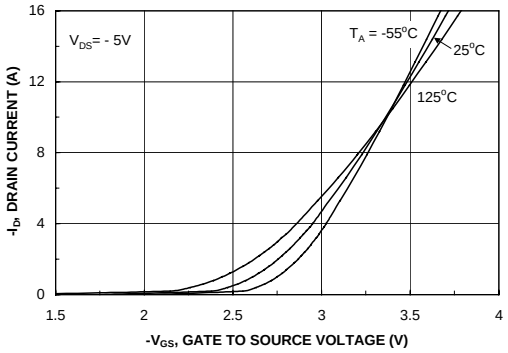


Figure 5. Transfer Characteristics.

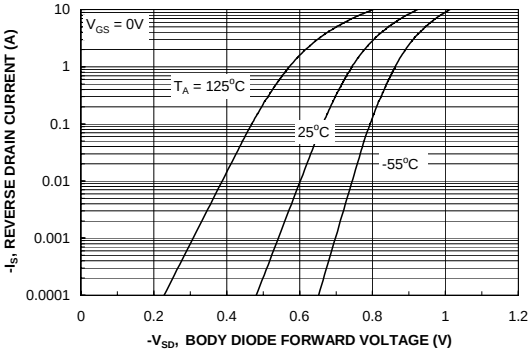


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

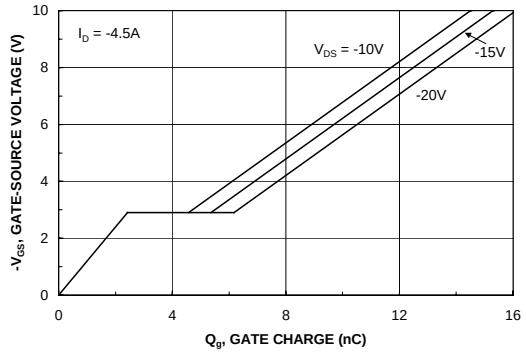


Figure 7. Gate Charge Characteristics.

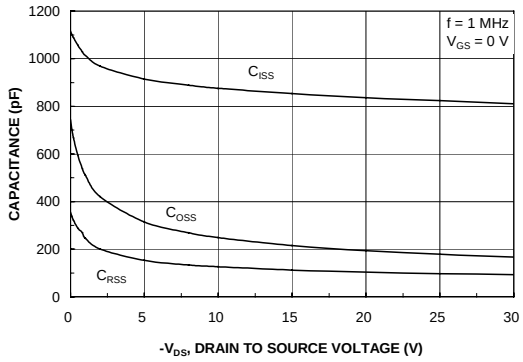


Figure 8. Capacitance Characteristics.

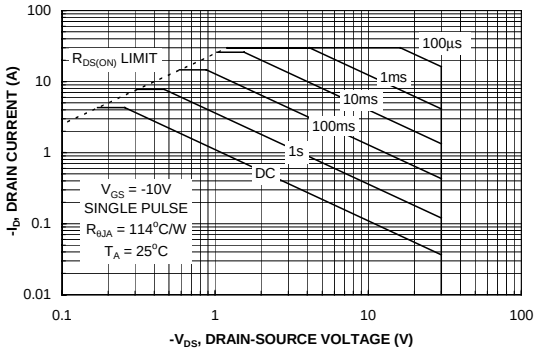


Figure 9. Maximum Safe Operating Area.

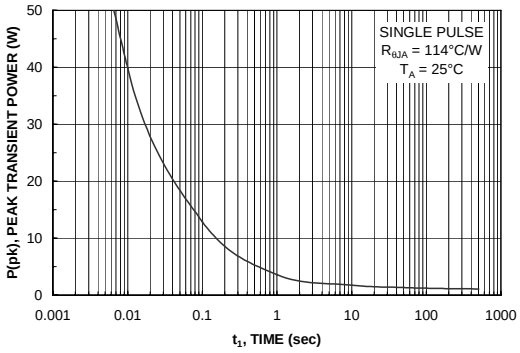


Figure 10. Single Pulse Maximum Power Dissipation.

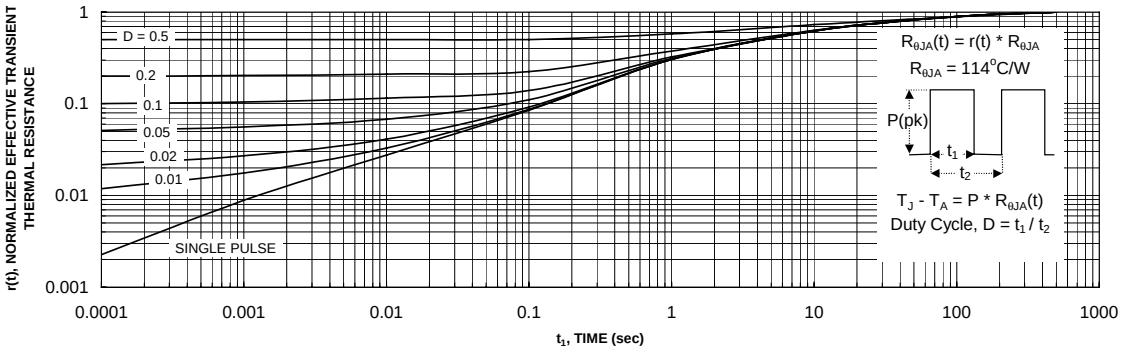


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

TSSOP(8lds) Tape and Reel Data

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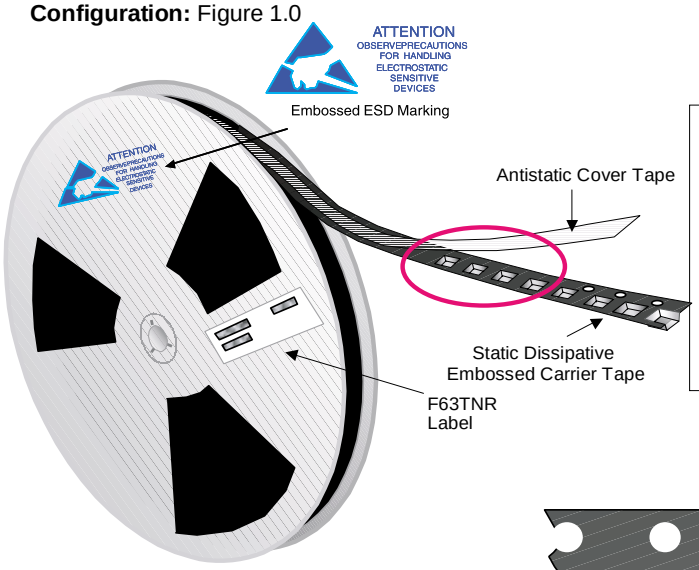
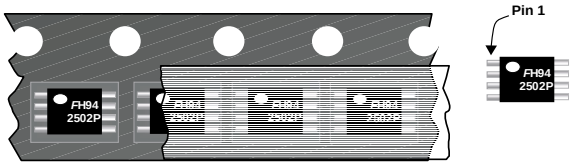
TSSOP(8lds) Packaging Configuration: Figure 1.0



Packaging Description:

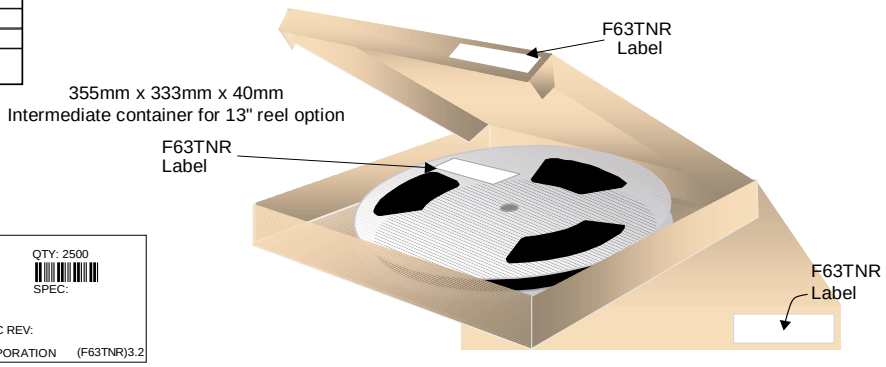
TSSOP-8lds parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are white in color and is made of polystyrene plastic (anti-static coated).

These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains one reel. These boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

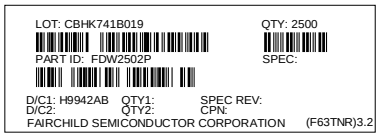


TSSOP-8lds Unit Orientation

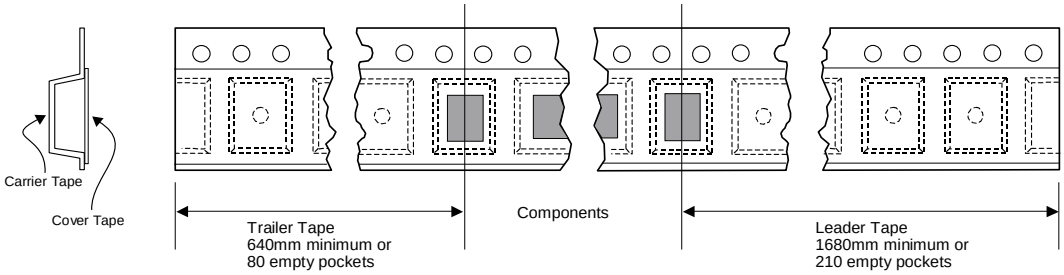
TSSOP (8lds) Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	TNR
Qty per Reel/Tube/Bag	2,500
Reel Size	13" Dia
Box Dimension (mm)	355x333X40
Max qty per Box	5,000
Weight per unit (gm)	0.020
Weight per Reel (kg)	0.426
Note/Comments	



F63TNR Label sample

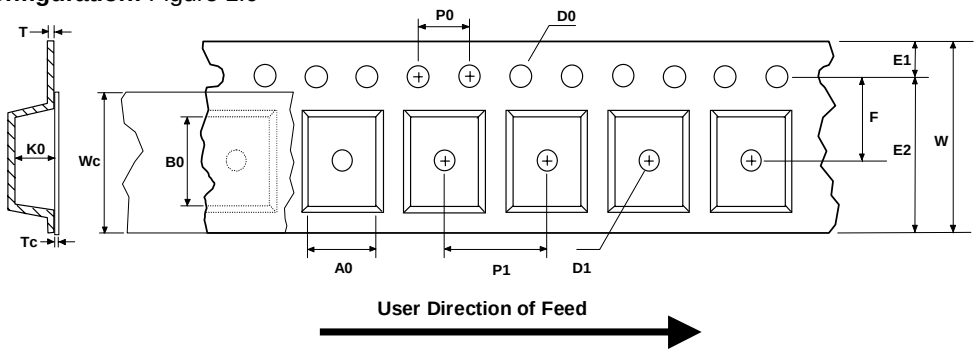


TSSOP(8lds) Tape Leader and Trailer Configuration: Figure 2.0



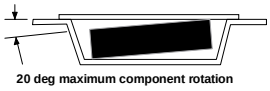
TSSOP(8lds) Tape and Reel Data, continued

TSSOP(8lds) Embossed Carrier Tape
Configuration: Figure 1.0

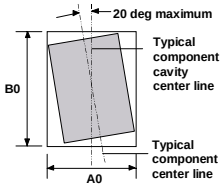


Dimensions are in millimeter														
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
TSSOP(8lds) (16mm)	see notes below	see notes below	16.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	14.25 min	7.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	see notes below	0.450 +/- 0.150	13.0 +/-0.3	0.06 +/-0.02

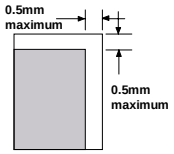
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

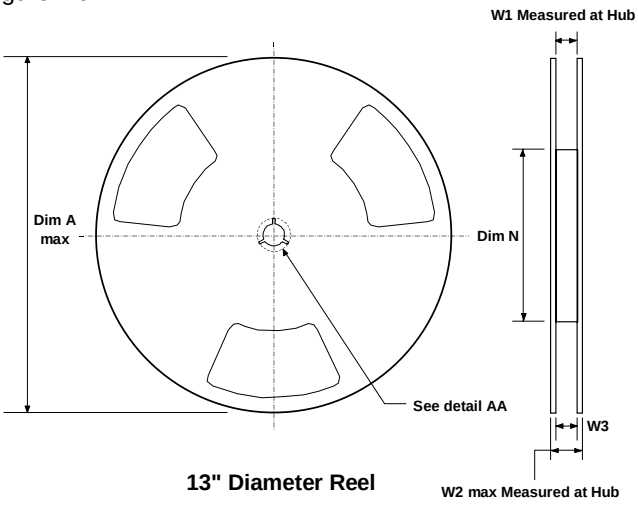


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

TSSOP(8lds) Reel Configuration:
Figure 2.0

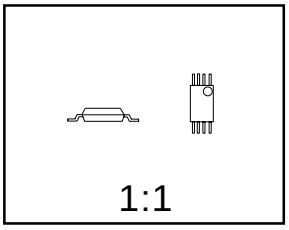


13" Diameter Reel

Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
16mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 101.6	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.626 – 0.764 15.9 – 19.4

TSSOP-8 Package Dimensions

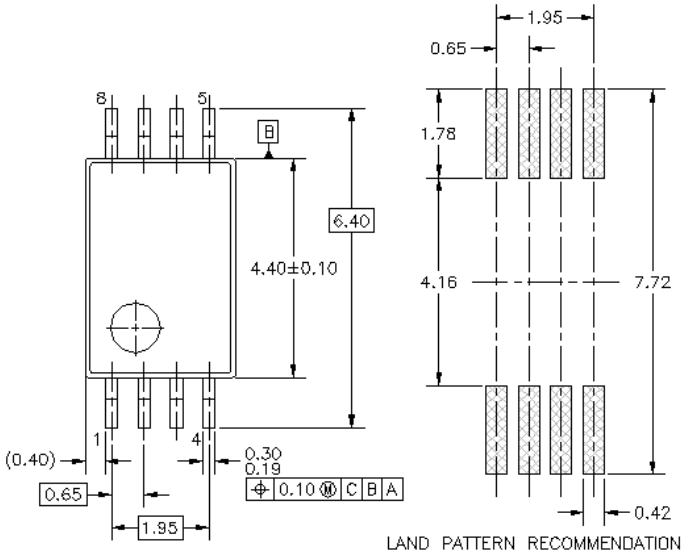
TSSOP-8 (FS PKG Code S4)



Scale 1:1 on letter size paper

Dimensions shown below are in millimeters

Part Weight per unit (gram): 0.0334



NOTES: UNLESS OTHERWISE SPECIFIED

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DenseTrench™	GTO™	Power247™	SuperSOT™-6	
DOME™	HiSeC™	PowerTrench®	SuperSOT™-8	
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E^2CMOS™	LittleFET™	QS™	TinyLogic™	
EnSigna™	MicroFET™	QT Optoelectronics™	TruTranslation™	
FACT™	MicroPak™	Quiet Series™	UHC™	
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

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Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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