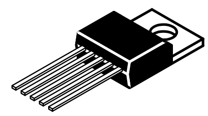
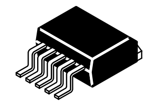




SLVS329A – JUNE 2001 – REVISED MAY 2002

FAST-TRANSIENT RESPONSE 5-A LOW-DROPOUT VOLTAGE REGULATORS

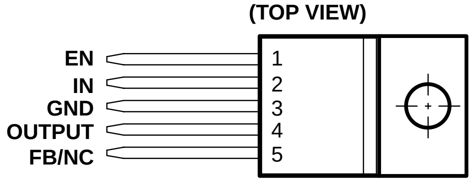
FEATURES

- **5-A Low-Dropout Voltage Regulator**
- **Available in 1.5-V, 1.8-V, 2.5-V, and 3.3-V Fixed-Output and Adjustable Versions**
- **Dropout Voltage Typically 250 mV at 5 A (TPS75633)**
- **Low 125 μA Typical Quiescent Current**
- **Fast Transient Response**
- **3% Tolerance Over Specified Conditions for Fixed-Output Versions**
- **Available in 5-Pin TO–220 and TO–263 Surface-Mount Packages**
- **Thermal Shutdown Protection**

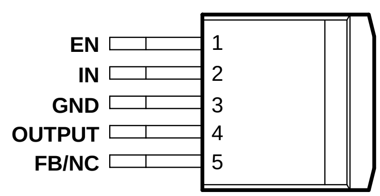
DESCRIPTION

The TPS756xx family of 5-A low dropout (LDO) regulators contains four fixed voltage option regulators and an adjustable voltage option regulator. These devices are capable of supplying 5 A of output current with a dropout of 250 mV (TPS75633). Therefore, the device is capable of performing a 3.3-V to 2.5-V conversion. Quiescent current is 125 μA at full load and drops down to less than 1 μA when the device is disabled. The TPS756xx is designed to have fast transient response for large load current changes.

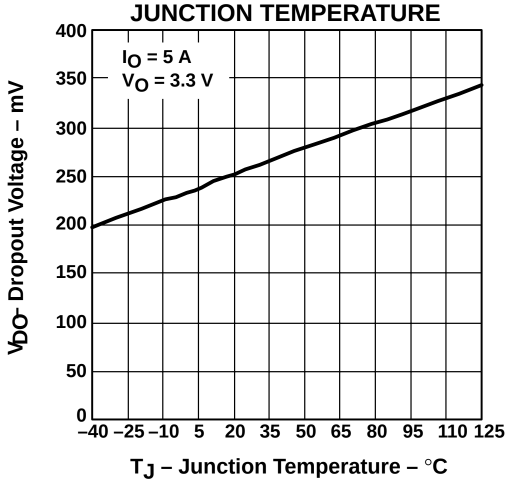
TO–220 (KC) PACKAGE
(TOP VIEW)



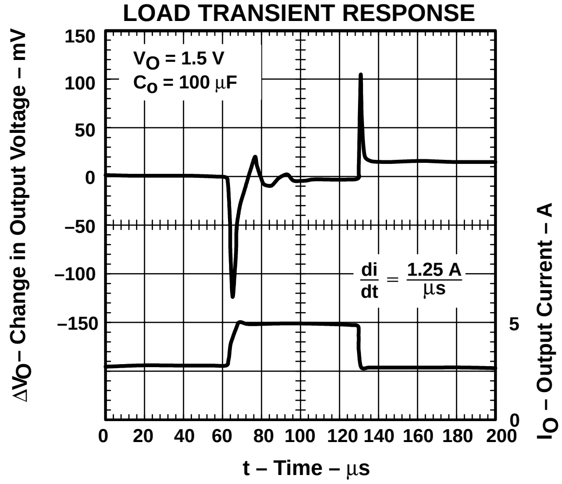
TO–263 (KTT) PACKAGE
(TOP VIEW)



TPS75633
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE



TPS75615
LOAD TRANSIENT RESPONSE



DESCRIPTION (continued)

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 250 mV at an output current of 5 A for the TPS75633) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 125 μA over the full range of output current). These two key specifications yield a significant improvement in operating life for battery-powered systems.

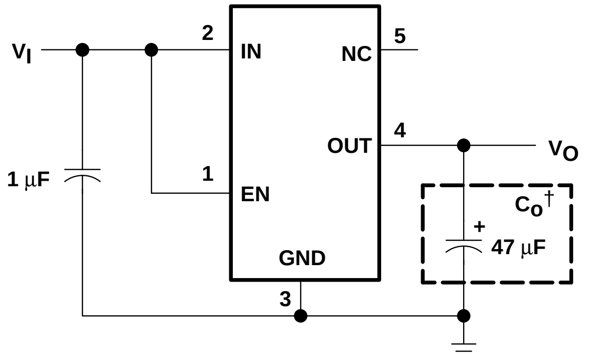
The device is enabled when EN (enable) is connected to a high voltage level (> 2 V). Applying a low voltage level (< 0.7 V) to EN shuts down the regulator, reducing the quiescent current to less than 1 μA at T_J = 25°C.

The TPS756xx is offered in 1.5-V, 1.8-V, 2.5-V, and 3.3-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.22 V to 5 V). Output voltage tolerance is specified as a maximum of 3% over line, load, and temperature ranges. The TPS756xx family is available in a 5-pin TO–220 (KC) and TO–263 (KTT) packages.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (TYP)	TO–220 (KC)	TO–263(KTT)
–40°C to 125°C	3.3 V	TPS75633KC	TPS75633KTT
	2.5 V	TPS75625KC	TPS75625KTT
	1.8 V	TPS75618KC	TPS75618KTT
	1.5 V	TPS75615KC	TPS75615KTT
	Adjustable 1.22 V to 5 V	TPS75601KC	TPS75601KTT

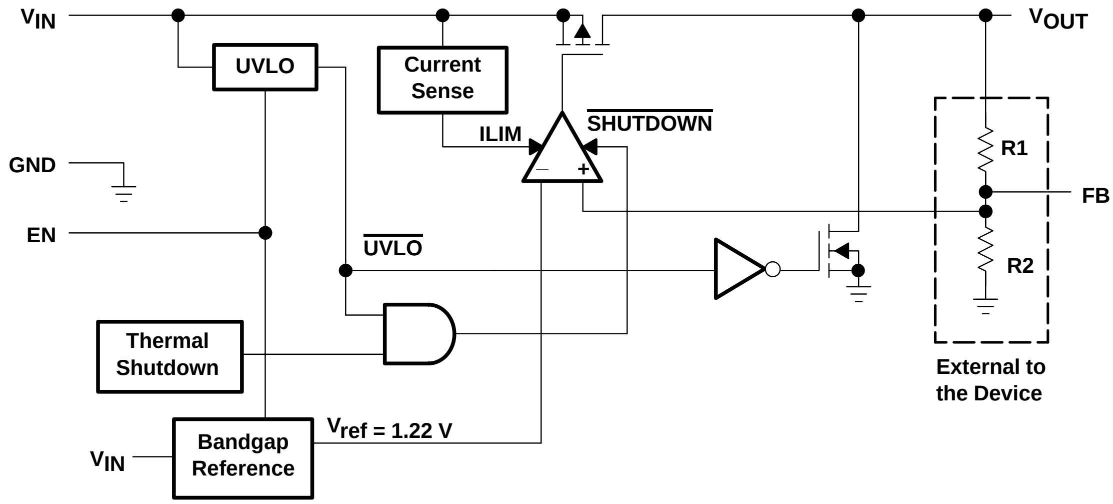
NOTE: The TPS75601 is programmable using an external resistor divider (see application information). The KTT package is available taped and reeled. Add an R suffix to the device type (e.g., TPS75601KTTR) to indicate tape and reel.



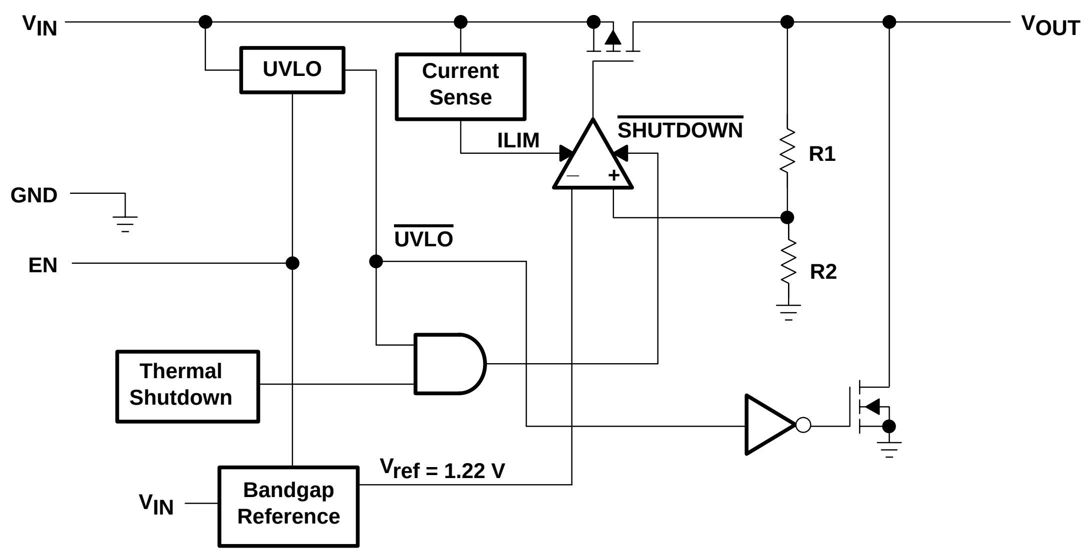
† See application information section for capacitor selection details.

Figure 1. Typical Application Configuration (For Fixed Output Options)

functional block diagram—adjustable version



functional block diagram—fixed version



Terminal Functions (TPS756xx)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
EN	1	I	Enable input
FB/NC	5	I	Feedback input voltage for adjustable device/no connection for fixed options
GND	3		Regulator ground
IN	2	I	Input voltage
OUTPUT	4	O	Regulated output voltage

detailed description

The TPS756xx family includes four fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, and 3.3 V), and an adjustable regulator, the TPS75601 (adjustable from 1.22 V to 5 V). The bandgap voltage is typically 1.22 V.

pin functions

enable (EN)

The EN terminal is an input which enables or shuts down the device. If EN is a low voltage level (< 0.7 V), the device will be in shutdown or sleep mode. When EN goes to a high voltage level (> 2 V), the device will be enabled.

feedback (FB)

FB is an input terminal used for the adjustable-output option and must be connected to the output terminal either directly, in order to generate the minimum output voltage of 1.22 V, or through an external feedback resistor divider for other output voltages. The FB connection should be as short as possible. It is essential to route it in such a way to minimize/avoid noise pickup. Adding RC networks between FB terminal and V_O to filter noise is not recommended because it may cause the regulator to oscillate.

input voltage (IN)

The V_{IN} terminal is an input to the regulator.

output voltage (OUTPUT)

The V_{OUTPUT} terminal is an output from the regulator.

absolute maximum ratings over operating junction temperature range (unless otherwise noted)†

Input voltage range‡, V_I . . . . –0.3 V to 6 V
Voltage range at EN . . . . –0.3 V to 6 V
Peak output current . . . . Internally limited
Continuous total power dissipation . . . . See Dissipation Rating Tables
Output voltage, V_O (OUTPUT, FB) . . . . 5.5 V
Operating junction temperature range, T_J . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
ESD rating, HBM . . . . 2 kV
ESD rating, CDM . . . . 500 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE

PACKAGE	$R_{\theta JC}$ (°C/W)	$R_{\theta JA}$ (°C/W)§
TO–220	2	58.7¶
TO–263	2	38.7#

§ For both packages, the $R_{\theta JA}$ values were computed using JEDEC high K board (2S2P) with 1 ounce internal copper plane and ground plane. There was no air flow across the packages.
¶ $R_{\theta JA}$ was computed assuming a vertical, free standing TO-220 package with pins soldered to the board. There is no heatsink attached to the package.
# $R_{\theta JA}$ was computed assuming a horizontally mounted TO-263 package with pins soldered to the board. There is no copper pad underneath the package.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I†	2.8	5.5	V
Output voltage range, V_O	1.22	5	V
Output current, I_O	0	5	A
Operating virtual junction temperature, T_J	–40	125	°C

† To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.

electrical characteristics over recommended operating junction temperature range (T_J = –40°C to 125°C), $V_I = V_{O(typ)}$ + 1 V, I_O = 1 mA, EN = V_I, C_o = 100 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (see Note 2)	Adjustable voltage	1.22 V ≤ V_O ≤ 5.5 V, T_J = 25°C		V_O		V
		1.22 V ≤ V_O ≤ 5.5 V	0.97 V_O		1.03 V_O	
		1.22 V ≤ V_O ≤ 5.5 V, T_J = 0 to 125°C (see Note 1)	0.97 V_O		1.03 V_O	V
	1.5 V Output	T_J = 25°C, 2.8 V < V_I < 5.5 V		1.5		V
		2.8 V ≤ V_I ≤ 5.5 V	1.455		1.545	
	1.8 V Output	T_J = 25°C, 2.8 V < V_I < 5.5 V		1.8		
		2.8 V ≤ V_I ≤ 5.5 V	1.746		1.854	
	2.5 V Output	T_J = 25°C, 3.5 V < V_I < 5.5 V		2.5		V
		3.5 V ≤ V_I ≤ 5.5 V	2.425		2.575	
	3.3 V Output	T_J = 25°C, 4.3 V < V_I < 5.5 V		3.3		V
		4.3 V ≤ V_I ≤ 5.5 V	3.201		3.399	
Quiescent current (GND current) (see Notes 2 and 3)		T_J = 25°C		125		µA
					200	
Output voltage line regulation ($\Delta V_O/V_O$) (see Note 3)		V_O + 1 V ≤ V_I ≤ 5.5 V, T_J = 25°C		0.04		%/V
		V_O + 1 V ≤ V_I < 5.5 V			0.1	
Load regulation (see Note 2)				0.35		%/V
Output noise voltage	TPS75615	BW = 300 Hz to 50 kHz, T_J = 25°C, V_I = 2.8 V		35		µVrms
Output current limit		V_O = 0 V	5.5	10	14	A
Thermal shutdown junction temperature				150		°C
Standby current		EN = 0, T_J = 25°C		0.1		µA
		EN = 0			10	µA
FB input current	TPS75601	FB = 1.5 V	–1		1	µA
Power supply ripple rejection	TPS75615	f = 100 Hz, T_J = 25°C, V_I = 2.8 V, I_O = 5 A		60		dB

NOTES: 1. The adjustable option operates with a 2% tolerance over T_J = 0 to 125°C.
2. I_O = 1 mA to 5 A
3. If V_O < 2.5 V then V_{Imin} = 2.8 V, V_{Imax} = 5.5 V:

$$\text{Line regulator (mV)} = (\%/\text{V}) \times \frac{V_O\left(V_{Imax} - 2.8\ \text{V}\right)}{100} \times 1000$$

If V_O ≥ 2.5 V then $V_{Imin} = V_O$ + 1 V, V_{Imax} = 5.5 V:

$$\text{Line regulator (mV)} = (\%/\text{V}) \times \frac{V_O\left(V_{Imax} - \left(V_O + 1\ \text{V}\right)\right)}{100} \times 1000$$

electrical characteristics over recommended operating junction temperature range (T_J = –40°C to 125°C), $V_I = V_{O(typ)}$ + 1 V, I_O = 1 mA, EN = 0 V, C_o = 100 μF (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input current ($\overline{EN}$)		EN = V_I	–1		1	μA
		EN = 0 V	–1	0	1	μA
High level EN input voltage			2			V
Low level EN input voltage					0.7	V
V_O	Dropout voltage, (3.3 V output) (see Note 3)	I_O = 5 A, V_I = 3.2 V, T_J = 25°C		250		mV
		I_O = 5 A, V_I = 3.2 V			500	
	Discharge transistor current	V_O = 1.5 V, T_J = 25°C	10	25		mA
V_I	UVLO	T_J = 25°C V_I rising	2.2		2.75	V
	UVLO hysteresis	T_J = 25°C V_I falling		100		mV

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	2, 3
		vs Junction temperature	4, 5
	Ground current	vs Junction temperature	6
	Power supply ripple rejection	vs Frequency	7
	Output spectral noise density	vs Frequency	8
z_o	Output impedance	vs Frequency	9
V_{DO}	Dropout voltage	vs Input voltage	10
		vs Junction temperature	11
V_I	Minimum required input voltage	vs Output voltage	12
	Line transient response		13, 15
	Load transient response		14, 16
V_O	Output voltage and enable voltage	vs Time (start-up)	17
	Equivalent series resistance	vs Output current	19, 20

TYPICAL CHARACTERISTICS

TPS75633
OUTPUT VOLTAGE vs OUTPUT CURRENT

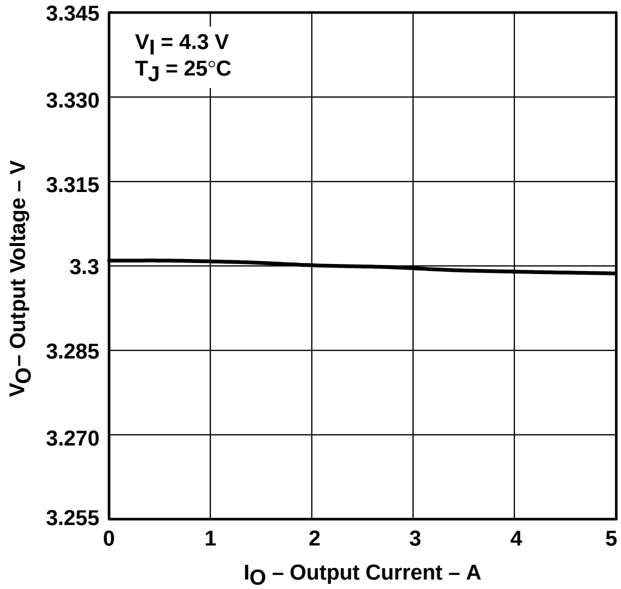


Figure 2

TPS75615
OUTPUT VOLTAGE vs OUTPUT CURRENT

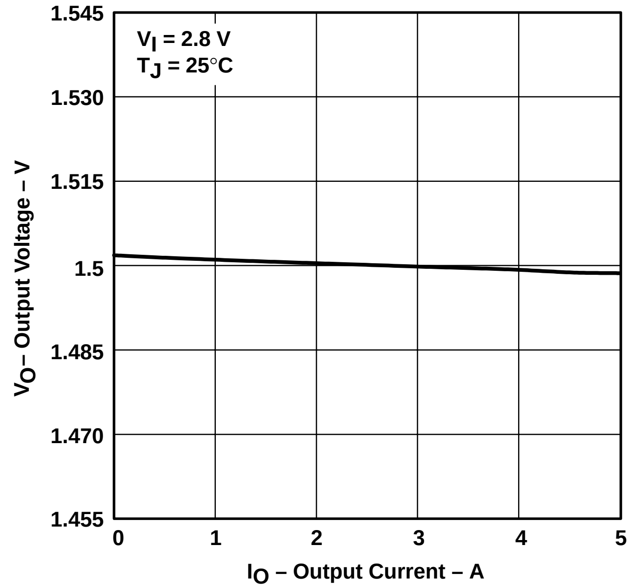


Figure 3

TPS75633
OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

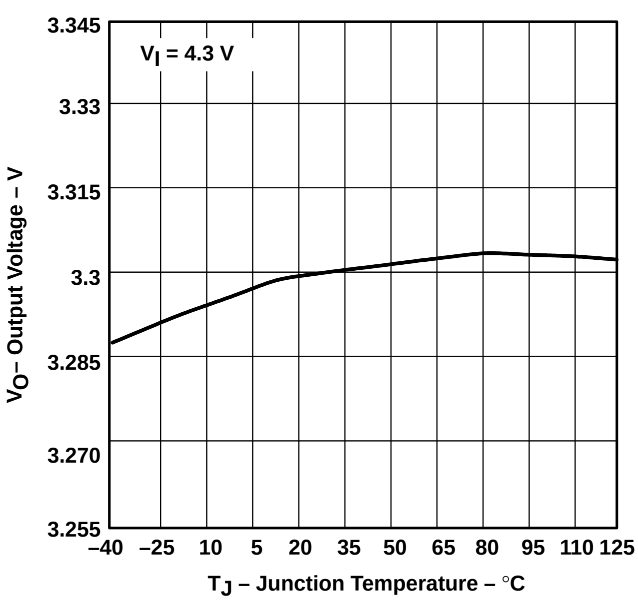


Figure 4

TPS75615
OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

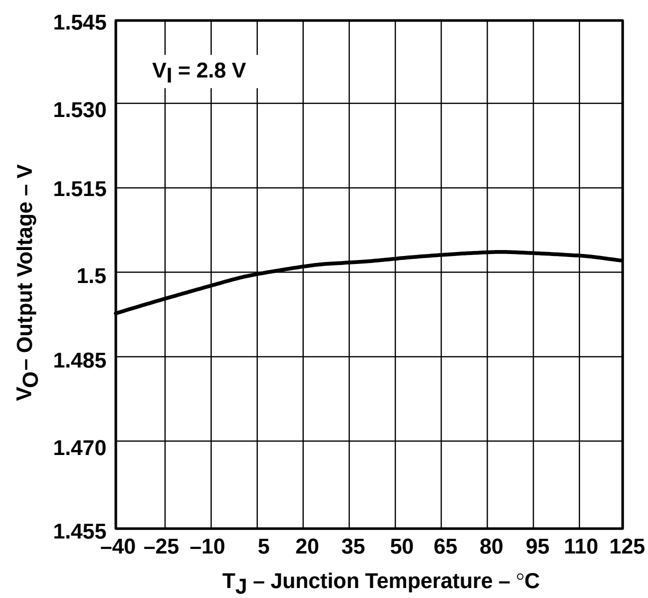


Figure 5

TYPICAL CHARACTERISTICS

TPS756xx
GROUND CURRENT
vs
JUNCTION TEMPERATURE

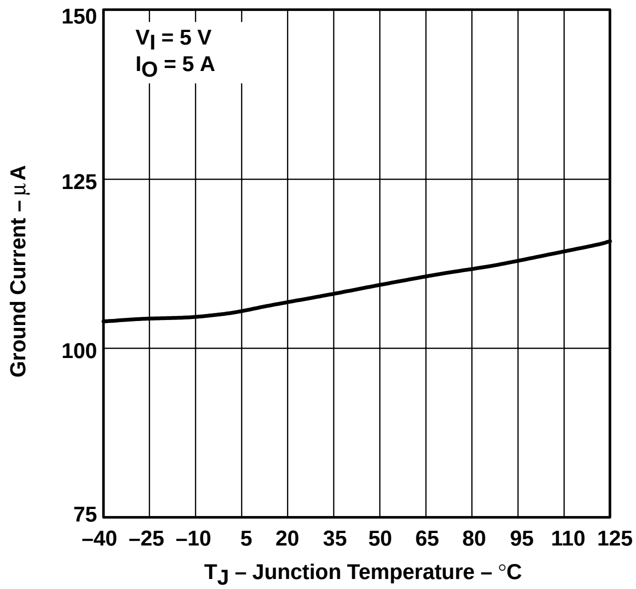


Figure 6

TPS75633
POWER SUPPLY RIPPLE REJECTION
vs
FREQUENCY

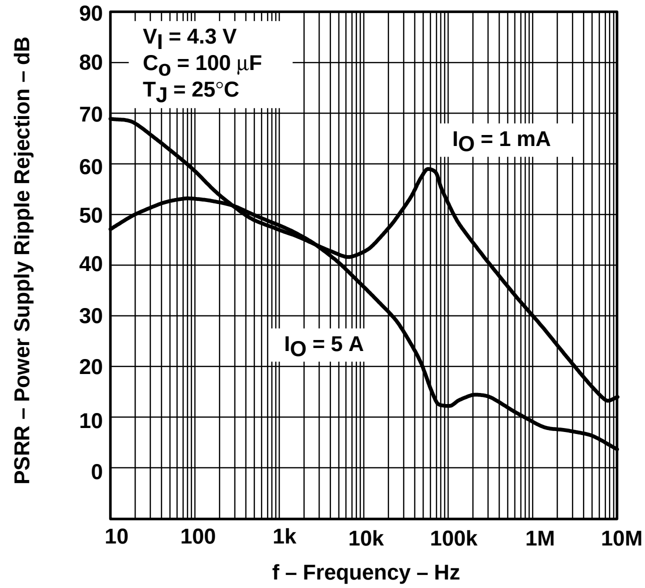


Figure 7

TPS75633
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

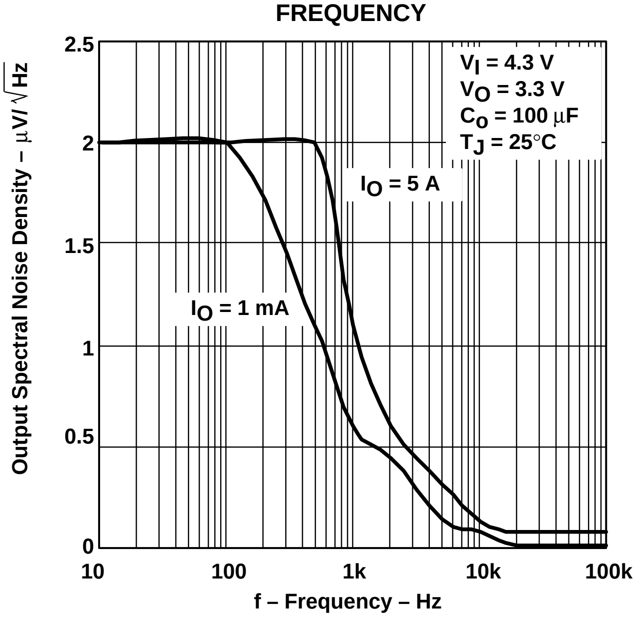


Figure 8

TPS75633
OUTPUT IMPEDANCE
vs
FREQUENCY

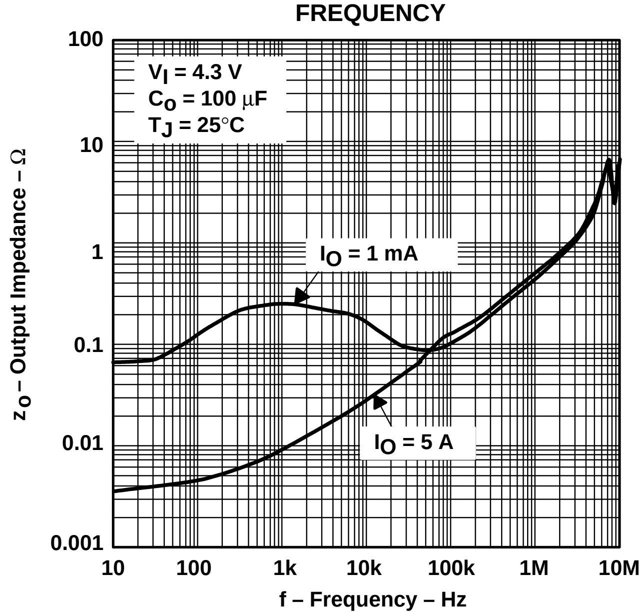


Figure 9

TYPICAL CHARACTERISTICS

TPS75601
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

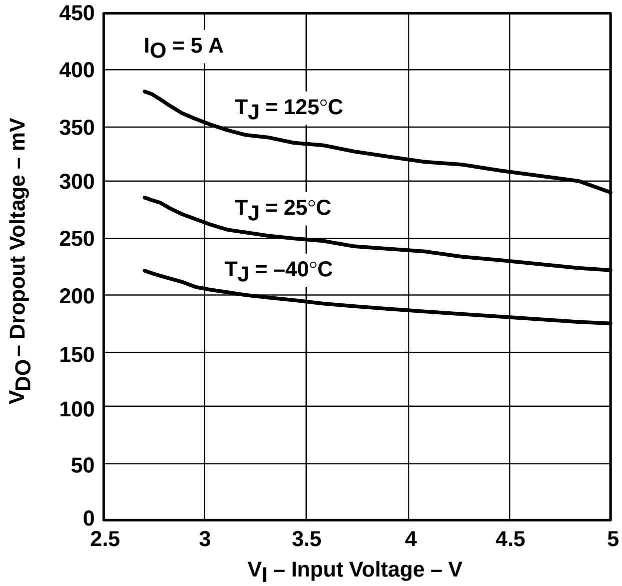


Figure 10

TPS75633
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

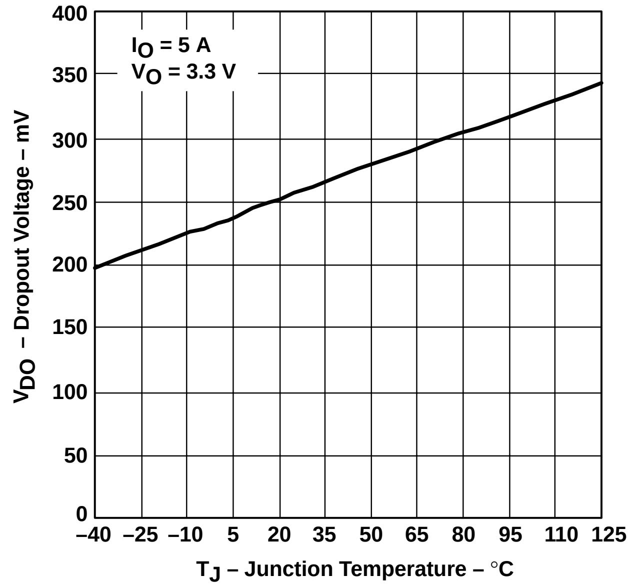


Figure 11

MINIMUM REQUIRED INPUT VOLTAGE
vs
OUTPUT VOLTAGE

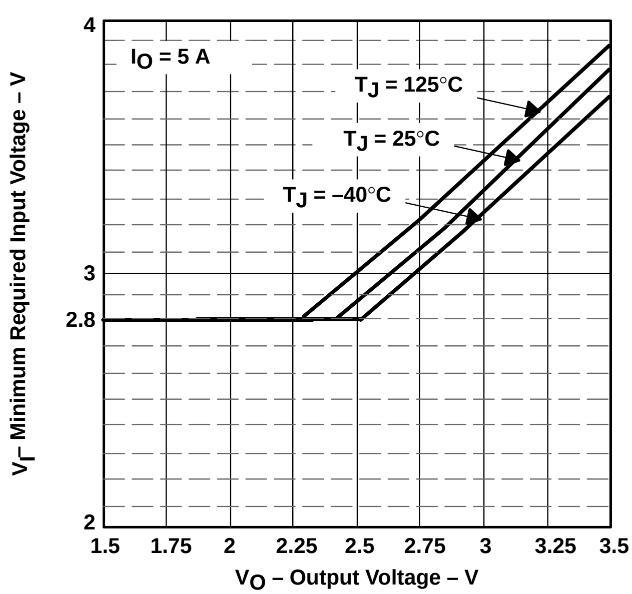


Figure 12

TPS75615
LINE TRANSIENT RESPONSE

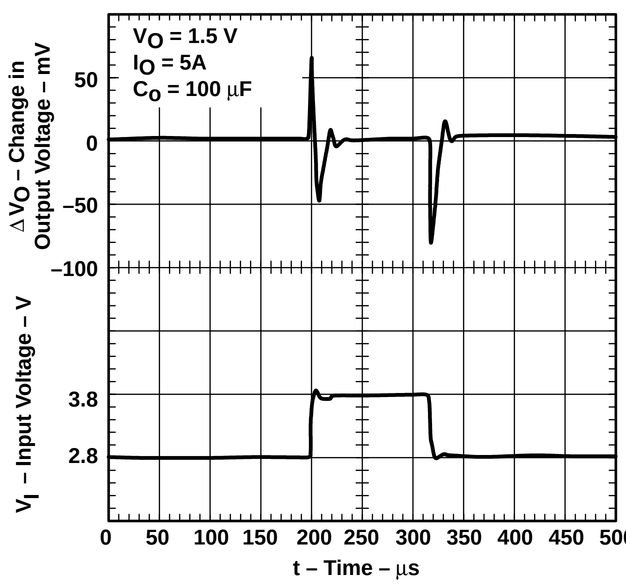


Figure 13

TYPICAL CHARACTERISTICS

TPS75615
LOAD TRANSIENT RESPONSE

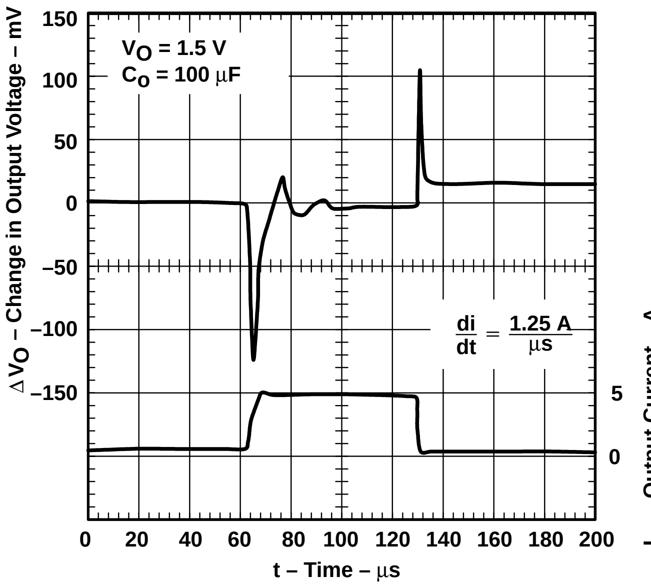


Figure 14

TPS75633
LINE TRANSIENT RESPONSE

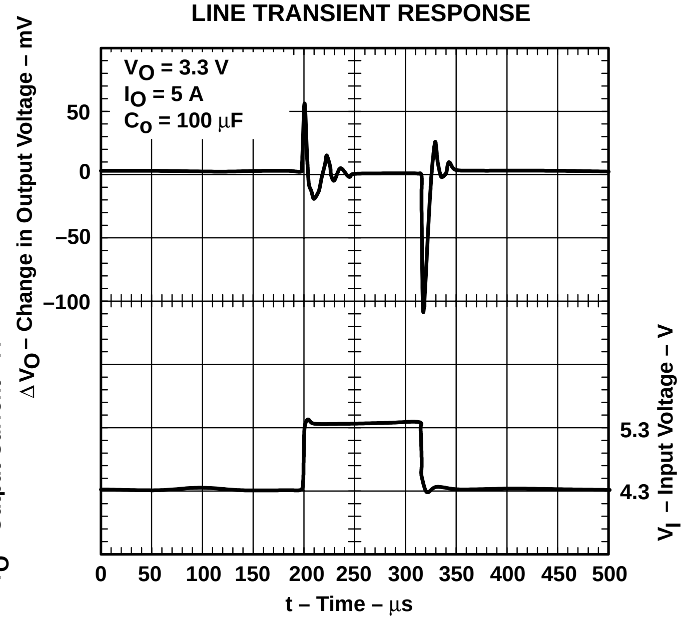


Figure 15

TPS75633
LOAD TRANSIENT RESPONSE

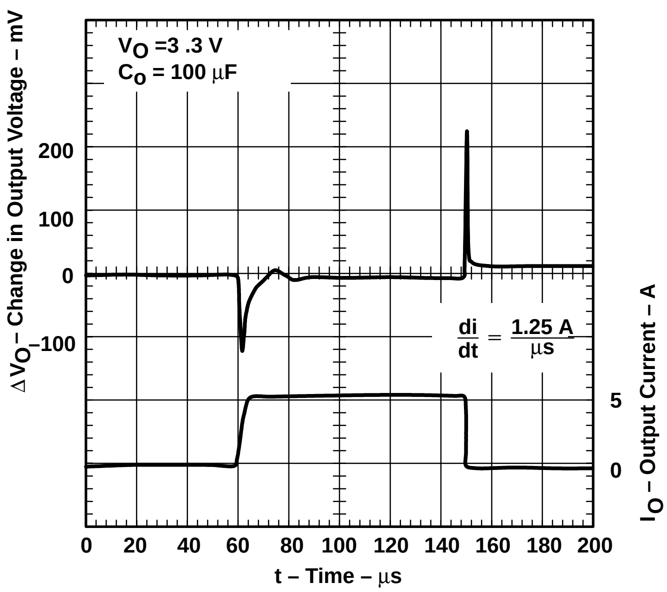


Figure 16

TPS75633
OUTPUT VOLTAGE AND ENABLE VOLTAGE
vs
TIME (START-UP)

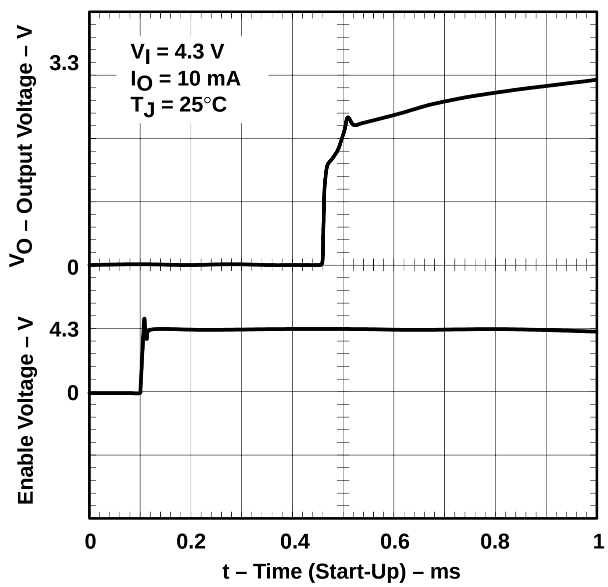


Figure 17

TYPICAL CHARACTERISTICS

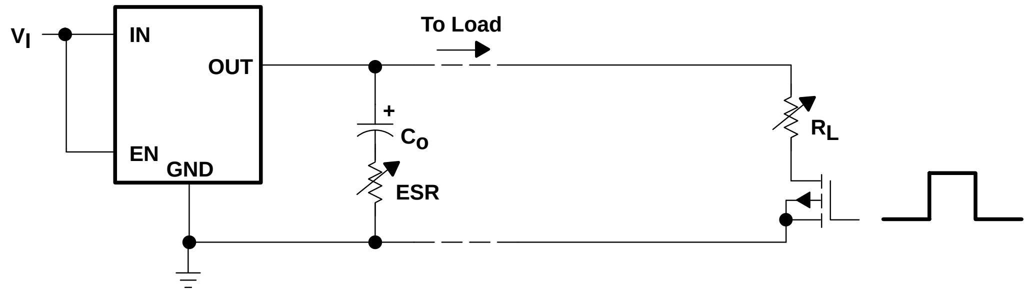


Figure 18. Test Circuit for Typical Regions of Stability (Figures 19 and 20) (Fixed Output Options)

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

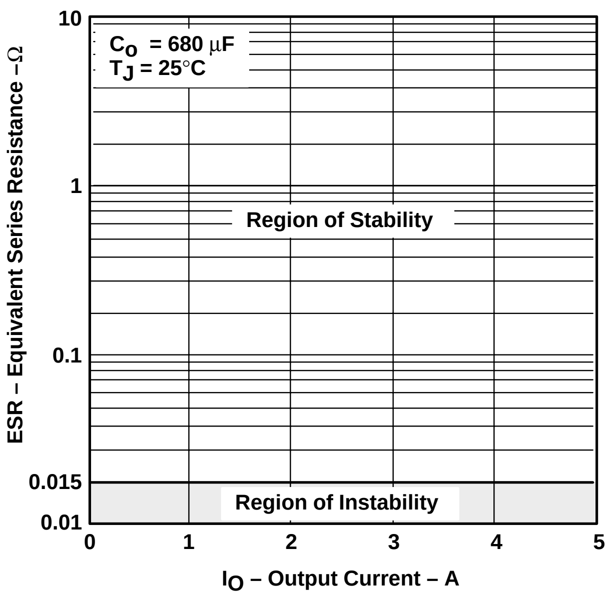


Figure 19

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

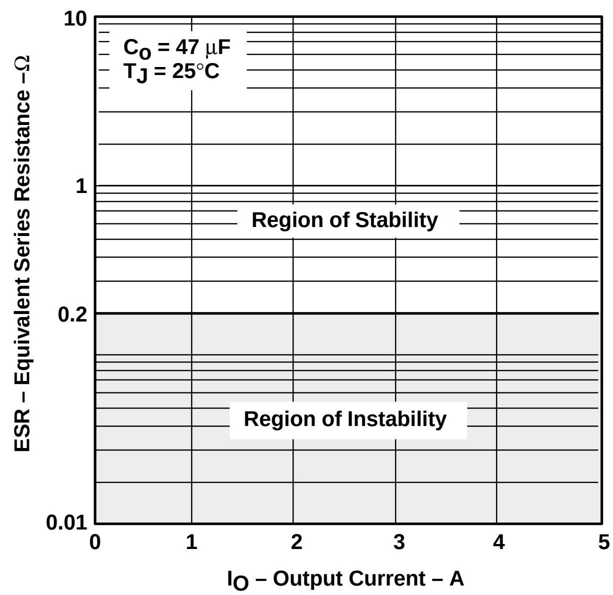


Figure 20

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

THERMAL INFORMATION

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature ($T_J$max) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature (T_J) does not exceed the maximum junction temperature ($T_J$max). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power ($P_{D(max)}$) consumed by a linear regulator is computed as:

$$P_D max = \left(V_{I(avg)} - V_{O(avg)}\right) \times I_{O(avg)} + V_{I(avg)} \, x \, I_{(Q)} \tag{1}$$

Where:

$V_{I(avg)}$ is the average input voltage.

$V_{O(avg)}$ is the average output voltage.

$I_{O(avg)}$ is the average output current.

$I_{(Q)}$ is the quiescent current.

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{I(avg)}$ x $I_{(Q)}$ can be neglected. The operating junction temperature is computed by adding the ambient temperature (T_A) and the increase in temperature due to the regulator's power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ($R_{\theta JC}$), the case to heatsink ($R_{\theta CS}$), and the heatsink to ambient ($R_{\theta SA}$). Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance.

Figure 21 illustrates these thermal resistances for (a) a TO–220 package attached to a heatsink, and (b) a TO–263 package mounted on a JEDEC High-K board.

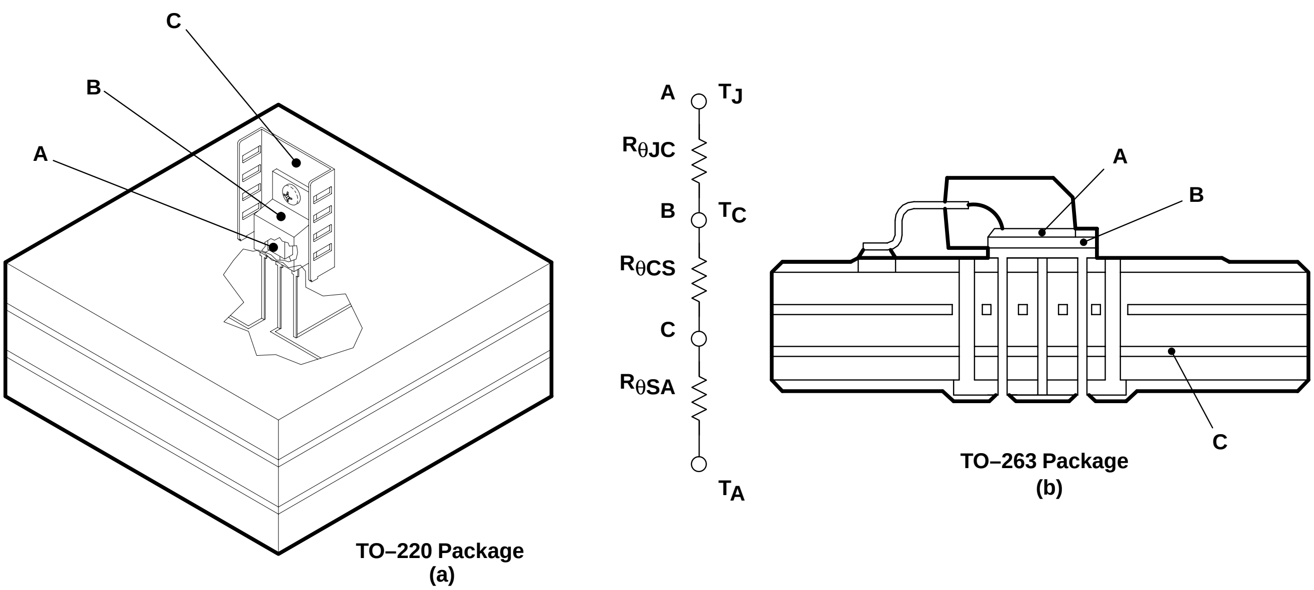


Figure 21. Thermal Resistances

THERMAL INFORMATION

Equation 2 summarizes the computation:

$$T_J = T_A + P_D max \times \left(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}\right) \tag{2}$$

The $R_{\theta JC}$ is specific to each regulator as determined by its package, lead frame, and die size provided in the regulator's data sheet. The $R_{\theta SA}$ is a function of the type and size of heatsink. For example, *black body radiator* type heatsinks, like the one attached to the TO–220 package in Figure 21(a), can have $R_{\theta CS}$ values ranging from 5 °C/W for very large heatsinks to 50 °C/W for very small heatsinks. The $R_{\theta CS}$ is a function of how the package is attached to the heatsink. For example, if a thermal compound is used to attach a heatsink to a TO–220 package, $R_{\theta CS}$ of 1°C/W is reasonable.

Even if no external *black body radiator* type heatsink is attached to the package, the board on which the regulator is mounted will provide some heatsinking through the pin solder connections. Some packages, like the TO–263 and TI's TSSOP PowerPAD™ packages, use a copper plane underneath the package or the circuit board's ground plane for additional heatsinking to improve their thermal performance. Computer aided thermal modeling can be used to compute very accurate approximations of an integrated circuit's thermal performance in different operating environments (e.g., different types of circuit boards, different types and sizes of heatsinks, and different air flows, etc.). Using these models, the three thermal resistances can be combined into one thermal resistance between junction and ambient ($R_{\theta JA}$). This $R_{\theta JA}$ is valid only for the specific operating environment used in the computer model.

Equation 2 simplifies into equation 3:

$$T_J = T_A + P_D max \times R_{\theta JA} \tag{3}$$

Rearranging equation 3 gives equation 4:

$$R_{\theta JA} = \frac{T_J - T_A}{P_D max} \tag{4}$$

Using equation 3 and the computer model generated curves shown in Figures 22 and 25, a designer can quickly compute the required heatsink thermal resistance/board area for a given ambient temperature, power dissipation, and operating environment.

THERMAL INFORMATION

TO–220 power dissipation

The TO–220 package provides an effective means of managing power dissipation in through-hole applications. The TO–220 package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. A heatsink can be used with the TO–220 package to effectively lower the junction-to-ambient thermal resistance.

To illustrate, the TPS75625 in a TO–220 package was chosen. For this example, the average input voltage is 3.3 V, the average output voltage is 2.5 V, the average output current is 3 A, the ambient temperature 55°C, the air flow is 150 LFM, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is:

$$P_D max = (3.3 - 2.5)\ V \times 3\ A = 2.4\ W \quad (5)$$

Substituting $T_J$max for T_J into equation 4 gives equation 6:

$$R_{\theta JA} max = (125 - 55)°C/2.4\ W = 29°C/W \quad (6)$$

From Figure 22, $R_{\theta JA}$ vs Heatsink Thermal Resistance, a heatsink with $R_{\theta SA}$ = 22°C/W is required to dissipate 2.4 W. The model operating environment used in the computer model to construct Figure 22 consisted of a standard JEDEC High-K board (2S2P) with a 1 oz. internal copper plane and ground plane. Since the package pins were soldered to the board, 450 mm^2 of the board was modeled as a heatsink. Figure 23 shows the side view of the operating environment used in the computer model.

THERMAL RESISTANCE
vs
HEATSINK THERMAL RESISTANCE

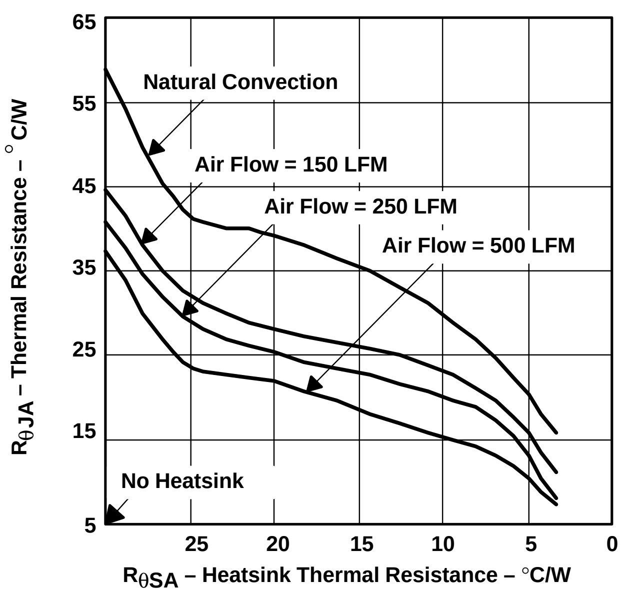


Figure 22

THERMAL INFORMATION

TO–220 power dissipation (continued)

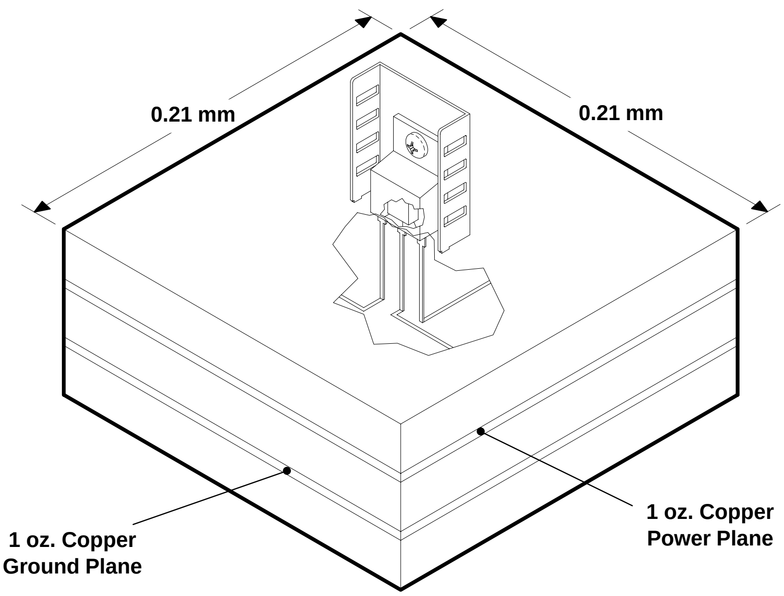


Figure 23

From the data in Figure 22 and rearranging equation 4, the maximum power dissipation for a different heatsink $R_{\theta SA}$ and a specific ambient temperature can be computed (see Figure 24).

POWER DISSIPATION LIMIT
vs
HEATSINK THERMAL RESISTANCE

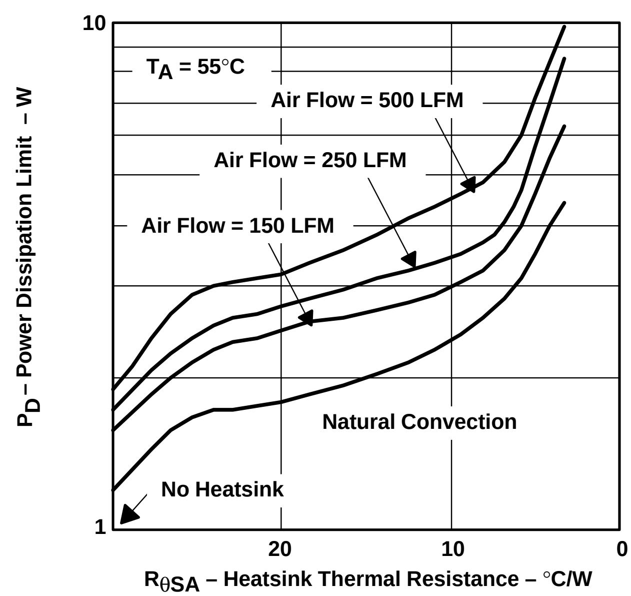


Figure 24

THERMAL INFORMATION

TO–263 power dissipation

The TO–263 package provides an effective means of managing power dissipation in surface-mount applications. The TO–263 package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the TO–263 package enhances the thermal performance of the package.

To illustrate, the TPS75625 in a TO–263 package was chosen. For this example, the average input voltage is 3.3 V, the average output voltage is 2.5 V, the average output current is 3 A, the ambient temperature 55°C, the air flow is 150 LFM, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is:

$$P_D max = (3.3 - 2.5)\ V \times 3\ A = 2.4\ W \tag{5}$$

Substituting $T_J max$ for T_J into equation 4 gives equation 6:

$$R_{\theta JA} max = (125 - 55)°C/2.4\ W = 29°C/W \tag{6}$$

From Figure 25, $R_{\theta JA}$ vs Copper Heatsink Area, the ground plane needs to be 2 cm^2 for the part to dissipate 2.4 W. The model operating environment used in the computer model to construct Figure 25 consisted of a standard JEDEC High-K board (2S2P) with a 1 oz. internal copper plane and ground plane. The package is soldered to a 2 oz. copper pad. The pad is tied through thermal vias to the 1 oz. ground plane. Figure 26 shows the side view of the operating environment used in the computer model.

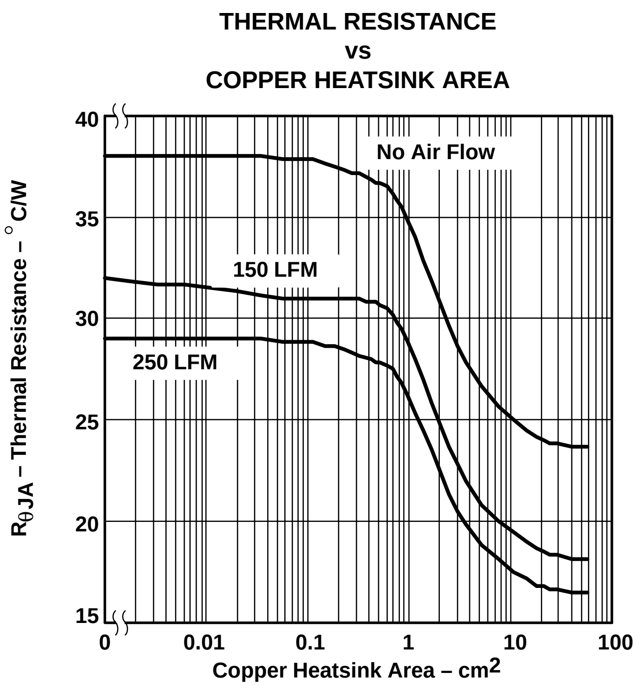


Figure 25

THERMAL INFORMATION

TO–263 power dissipation (continued)

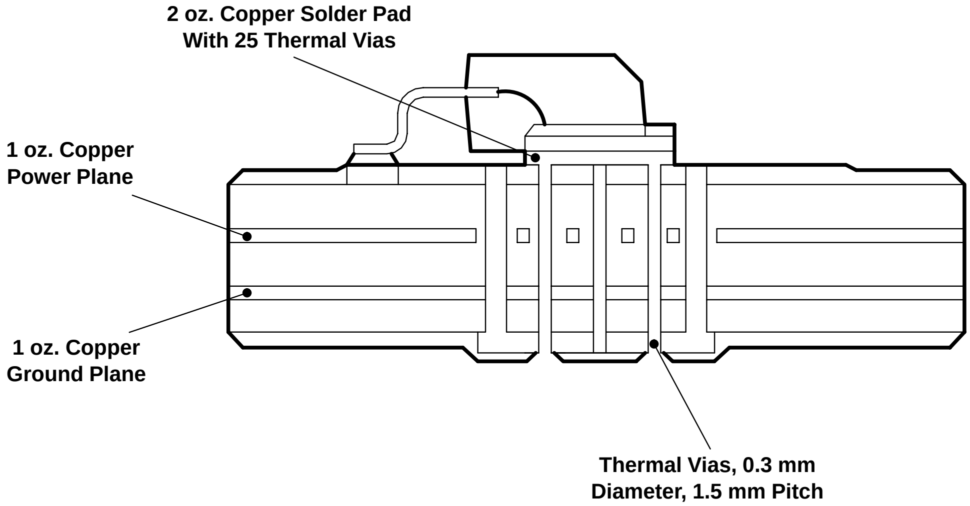


Figure 26

From the data in Figure 25 and rearranging equation 4, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed (see Figure 27).

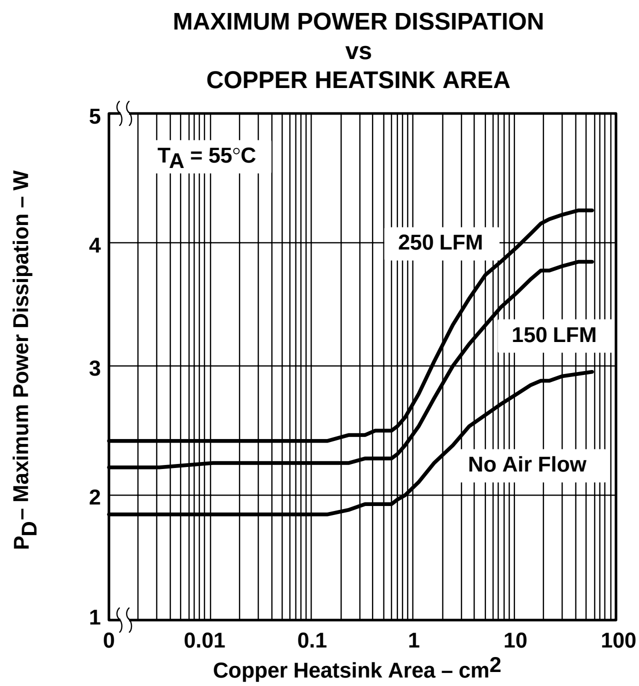


Figure 27

APPLICATION INFORMATION

programming the TPS75601 adjustable LDO regulator

The output voltage of the TPS75601 adjustable regulator is programmed using an external resistor divider as shown in Figure 28. The output voltage is calculated using:

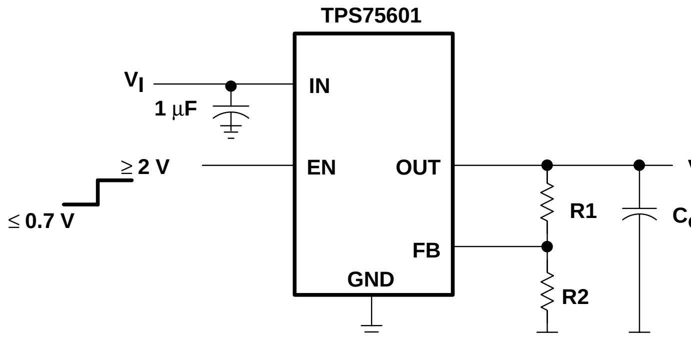
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{7}$$

Where:

V_{ref} = 1.224 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 40-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 40 µA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \tag{8}$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	31.6	30.1	kΩ
3.3 V	51	30.1	kΩ
3.6 V	58.3	30.1	kΩ

Figure 28. TPS75601 Adjustable LDO Regulator Programming

regulator protection

The TPS756xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS756xx also features internal current limiting and thermal protection. During normal operation, the TPS756xx limits output current to approximately 10 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

APPLICATION INFORMATION

input capacitor

For a typical application, a ceramic input bypass capacitor (0.22 µF–1 µF) is recommended to ensure device stability. This capacitor should be as close as possible to the input pin. Due to the impedance of the input supply, large transient currents will cause the input voltage to droop. If this droop causes the input voltage to drop below the UVLO threshold, the device will turn off. Therefore, it is recommended that a larger capacitor be placed in parallel with the ceramic bypass capacitor at the regulator's input. The size of this capacitor depends on the output current, response time of the main power supply, and the main power supply's distance to the regulator. At a minimum, the capacitor should be sized to ensure that the input voltage does not drop below the minimum UVLO threshold voltage during normal operating conditions.

output capacitor

As with most LDO regulators, the TPS756xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 47 µF with an ESR (equivalent series resistance) of at least 200 mΩ. As shown in Figure 29, most capacitor and ESR combinations with a product of 47e–6 x 0.2 = 9.4e–6 or larger will be stable, provided the capacitor value is at least 47 µF. Solid tantalum electrolytic and aluminum electrolytic capacitors are all suitable, provided they meet the requirements described in this section. Larger capacitors provide a wider range of stability and better load transient response.

This information along with the ESR graphs, Figures 19, 20, and 29, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet these guidelines.

OUTPUT CAPACITANCE
vs
EQUIVALENT SERIES RESISTANCE

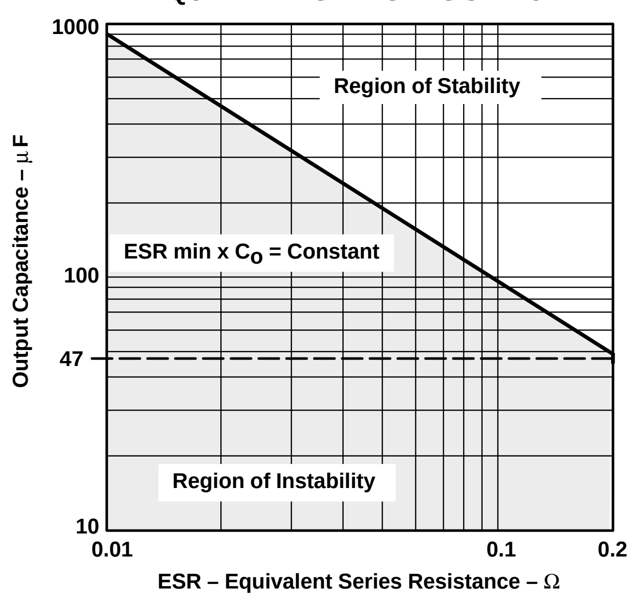
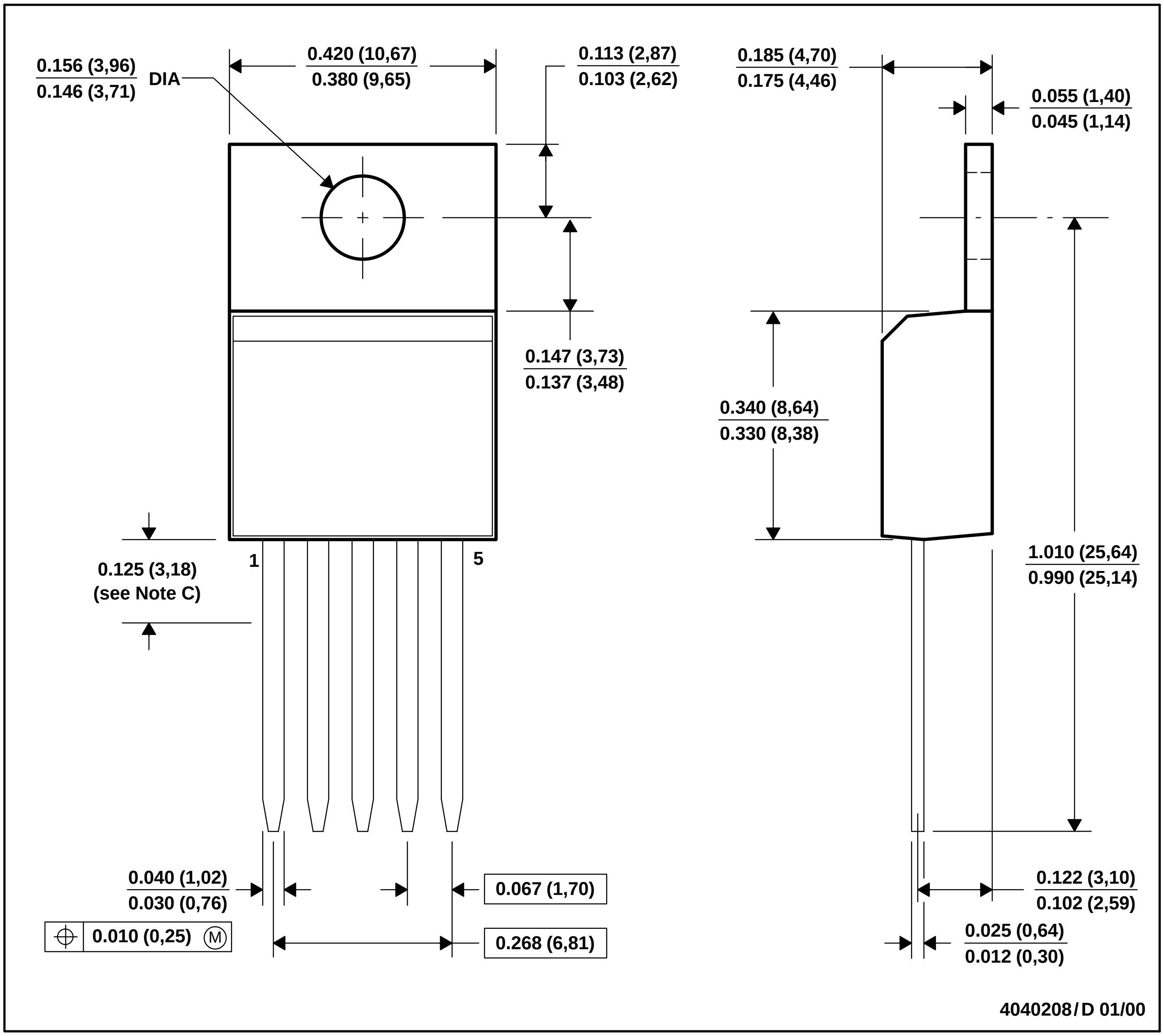


Figure 29

MECHANICAL DATA

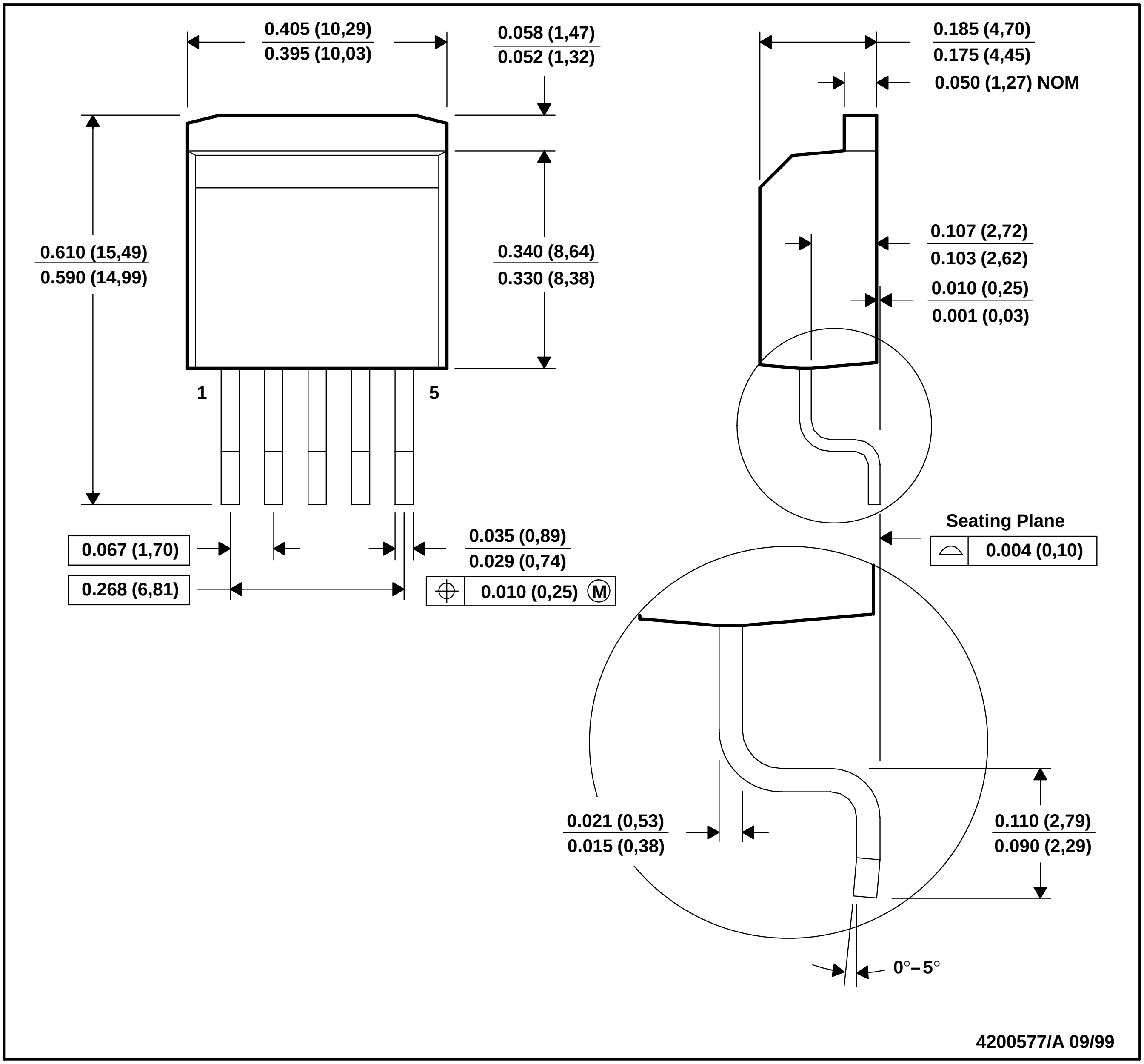
KC (R-PSFM-T5) **PLASTIC FLANGE-MOUNT**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. All lead dimensions apply before solder dip.
E. The center lead is in electrical contact with the mounting tab.

MECHANICAL DATA

KTT (R-PSFM-G5) **PLASTIC FLANGE-MOUNT**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).

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