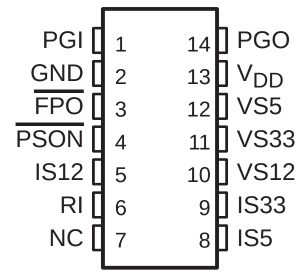
- **Overvoltage Protection and Lockout for 12 V, 5 V, and 3.3 V**
- **Overcurrent Protection and Lockout for 12 V, 5 V, and 3.3 V**
- **Undervoltage Protection and Lockout for 12 V, and Undervoltage Detect for 5 V and 3.3 V**
- **Fault-Protection Output With Open Drain Output Stage**
- **Open-Drain, Power Good Output Signal for Power-Good Input, 3.3 V and 5 V**
- **300-ms Power-Good Delay**
- **75-ms Delay for 5-V and 3.3-V Power Supply Short-Circuit Turnon Protection**
- **2.3 ms $\overline{\text{PSON}}$ Control to $\overline{\text{FPO}}$ Turnoff Delay**
- **38 ms $\overline{\text{PSON}}$ Control Debounce**
- **Wide Supply Voltage Range From 4.5 V to 15 V**

**D OR N PACKAGE**
**(TOP VIEW)**

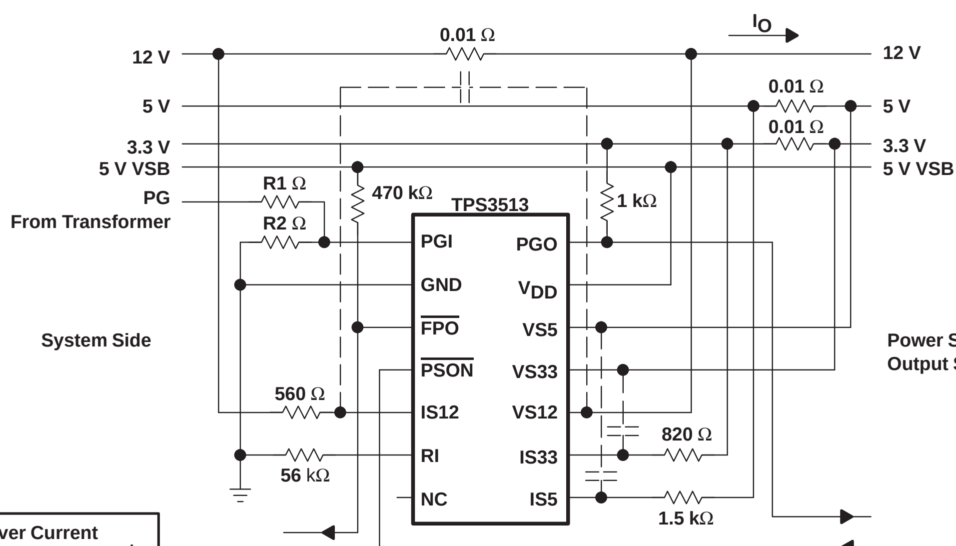



NC – No internal connection

## description

The TPS3513 is designed to optimize PC switching power supply system with minimum external components. It provides undervoltage lockout (UVLO), protection circuits, power good indicator, and on/off control.

## typical application




| | Max Output Current | Over Current Protection Trip Point† |
|---|---|---|
| 12 V | 6 A | 9.2 A |
| 5 V | 16 A | 24.6 A |
| 3.3 v | 9 A | 13.5 A |

† Over current protection trip point can be programmable.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## description (continued)

UVLO thresholds are 4.45 V (on) and 3.65 V (off). Overcurrent protection (OCP) and overvoltage protection (OVP) monitor 3.3 V, 5 V, and 12 V. When an OC or OV condition is detected, the power-good output (PGO) is asserted low and the fault protection output (FPO) is latched high. PSON from low-to-high resets the latch. The OCP function will be enabled 75 ms after PSON goes low, and a debounce of typically 38 ms. A built-in 2.3-ms delay with 38-ms debounce from PSON to FPO output is enabled at turnoff.

An external resistor is connected between the RI pin and the GND pin. This will introduce an accurate $I_{(ref)}$ for OCP function. The $I_{(ref)}$ range is from 12.5 µA to 62.5 µA. The formula for choosing RI resistor is $V_{(RI)}/I_{(ref)}$. Three OCP comparators and the $I_{(ref)}$ section are supplied by VS12. The current draw from the VS12 pin is less than 1 mA.

The power good feature monitors PGI, 3.3 V and 5 V, and issues a power good signal when the output is ready.

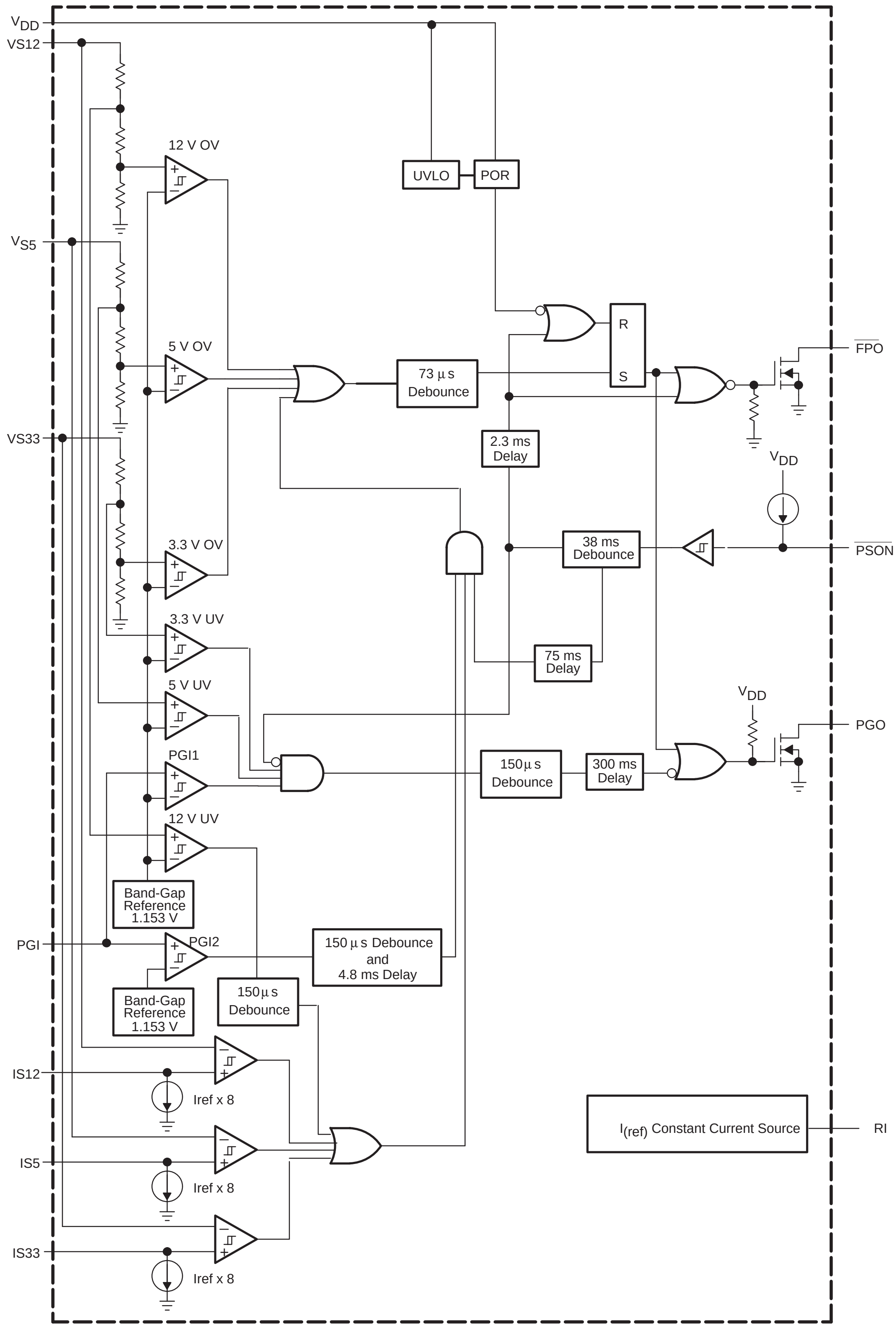
The TPS3513 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

| PGI | $\overline{\text{PSON}}$ | UV CONDITION 3.3 V / 5 V | OV CONDITIONS | UV CONDITION 12 V OC CONDITIONS | $\overline{\text{FPO}}$ | PGO |
|---|---|---|---|---|---|---|
| < 0.9 V | L | No | No | No | L | L |
| < 0.9 V | L | No | No | Yes | L | L |
| < 0.9 V | L | No | Yes | No | H | L |
| < 0.9 V | L | No | Yes | Yes | H | L |
| < 0.9 V | L | Yes | No | No | L | L |
| < 0.9 V | L | Yes | No | Yes | L | L |
| < 0.9 V | L | Yes | Yes | No | H | L |
| < 0.9 V | L | Yes | Yes | Yes | H | L |
| 1.0 V < PGI < 1.1 V | L | No | No | No | L | L |
| 1.0 V < PGI < 1.1 V | L | No | No | Yes | H | L |
| 1.0 V < PGI < 1.1 V | L | No | Yes | No | H | L |
| 1.0 V < PGI < 1.1 V | L | No | Yes | Yes | H | L |
| 1.0 V < PGI < 1.1 V | L | Yes | No | No | H | L |
| 1.0 V < PGI < 1.1 V | L | Yes | No | Yes | H | L |
| 1.0 V < PGI < 1.1 V | L | Yes | Yes | No | H | L |
| 1.0 V < PGI < 1.1 V | L | Yes | Yes | Yes | H | L |
| >1.2 V | L | No | No | No | L | H |
| >1.2 V | L | No | No | Yes | H | L |
| >1.2 V | L | No | Yes | No | H | L |
| >1.2 V | L | No | Yes | Yes | H | L |
| >1.2 V | L | Yes | No | No | H | L |
| >1.2 V | L | Yes | No | Yes | H | L |
| >1.2 V | L | Yes | Yes | No | H | L |
| >1.2 V | L | Yes | Yes | Yes | H | L |
| x | H | x | x | x | H | L |

x = don't care
$\overline{\text{FPO}}$ = L means: fault is not latched
$\overline{\text{FPO}}$ = H means: fault is latched
PGO = L means: fault
PGO = H means: No fault

## schematic


VDD
VS12
12 V OV
UVLO
POR
VS5
R
5 V OV
73 µs Debounce
S
FPO
VS33
2.3 ms Delay
VDD
3.3 V OV
38 ms Debounce
PSON
3.3 V UV
75 ms Delay
5 V UV
VDD
PGO
PGI1
150µs Debounce
300 ms Delay
12 V UV
Band-Gap Reference 1.153 V
PGI
PGI2
150 µs Debounce and 4.8 ms Delay
150µs Debounce
Band-Gap Reference 1.153 V
IS12
Iref x 8
I(ref) Constant Current Source
RI
IS5
Iref x 8
IS33
Iref x 8

## timing requirements

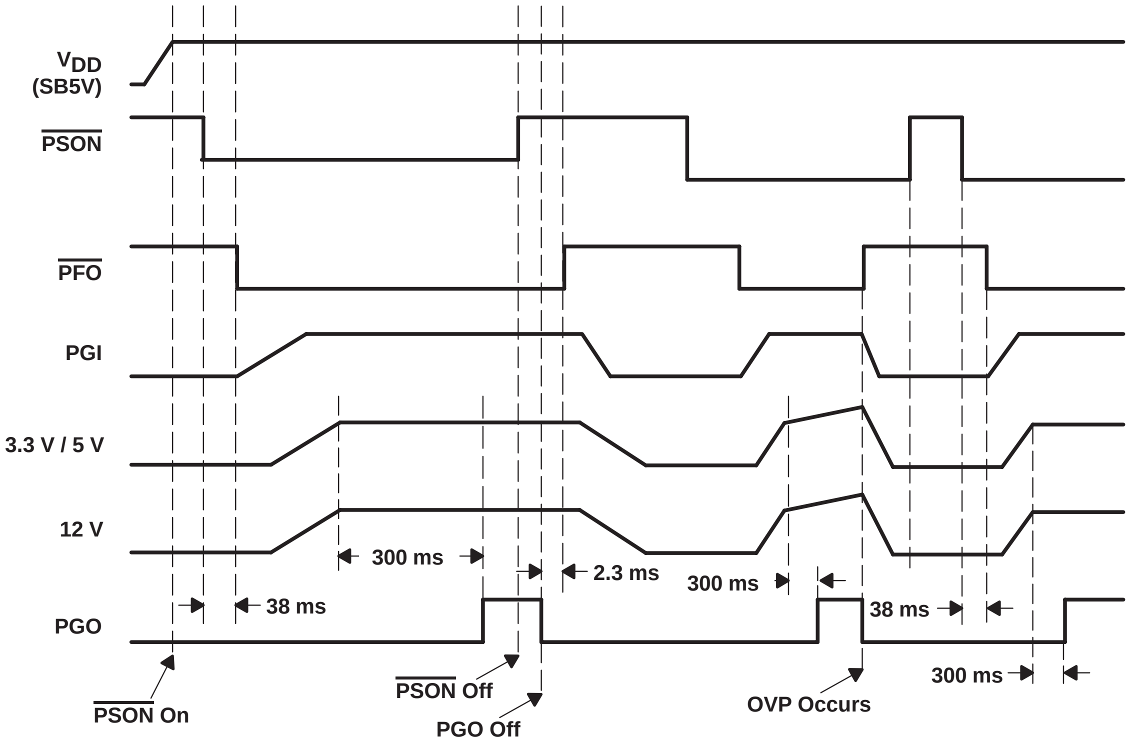



**Figure 1. AC Turnon and Overvoltage Protect**

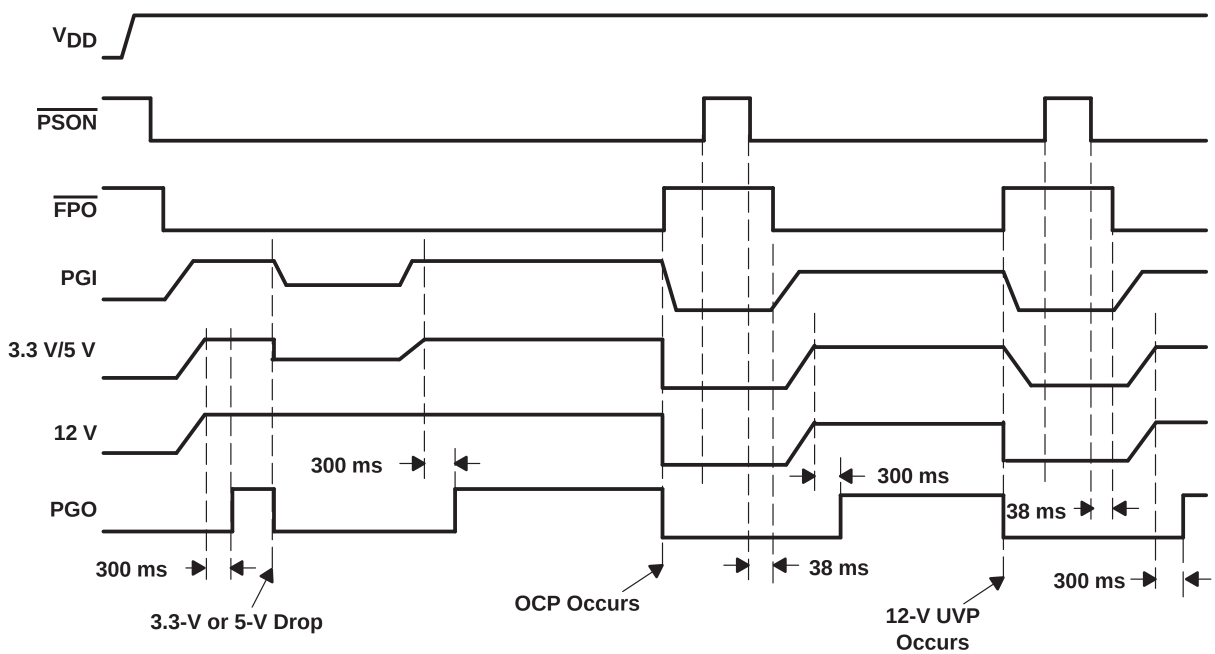



**Figure 2. Overcurrent and Undervoltage Detect/Protect**

## Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| $\overline{FPO}$ | 3 | O | Inverted fault protection output, open-drain, output stage |
| GND | 2 | | Ground |
| IS12 | 5 | I | 12-V overcurrent protection |
| IS5 | 8 | I | 5-V overcurrent protection |
| IS33 | 9 | I | 3.3-V overcurrent protection |
| NC | 7 | | No internal connection |
| PGI | 1 | I | Power-good input |
| PGO | 14 | O | Power-good output, open drain output stage |
| $\overline{PSON}$ | 4 | I | On/off control |
| RI | 6 | I | Current sense setting |
| $V_{DD}$ | 13 | I | Supply voltage |
| VS12 | 10 | I | 12-V overvoltage/undervoltage protection |
| VS33 | 11 | I | 3.3-V overvoltage protect/undervoltage detect |
| VS5 | 12 | I | 5-V overvoltage protect/undervoltage detect |

## detailed description

### power-good and power-good delay

A PC power supply is commonly designed to provide a power-good signal, which is defined by the computer manufacturers. PGO is a power-good signal and should be asserted high by the PC power supply to indicate that the 5-VDC and 3.3-VDC outputs are above the undervoltage threshold limit. At this time the converter should be able to provide enough power to assure continuous operation within the specification. Conversely, when either the 5-VDC or the 3.3-VDC output voltages fall below the undervoltage threshold, or when main power has been removed for a sufficiently long time so that power supply operation is no longer assured, PGO should be deasserted to a low state.

The power-good (PGO), DC enable ($\overline{PSON}$), and the 5-V/3.3-V supply rails are shown in Figure 3.

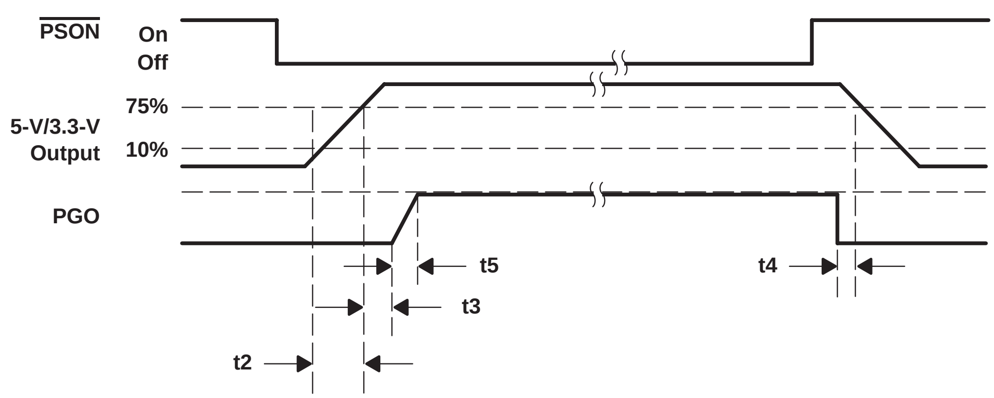



**Figure 3. Timing of $\overline{PSON}$ and PGO**

Although there is no requirement to meet specific timing parameters, the following signal timings are recommended:

2 ms ≤ t2 ≤ 20 ms, 100 ms < t3 < 2000 ms, t4 > 1 ms, t5 ≤ 10 ms

**power-good and power-good delay (continued)**

Furthermore, motherboards should be designed to comply with the above recommended timing. If timings other than these are implemented or required, this information should be clearly specified.

The TPS3513 family of power-supply supervisors provides a power-good output (PGO) for the 3.3-V and 5-V supply voltage rails and a separate power-good input (PGI). An internal timer is used to generate a 300-ms power-good delay.

If the voltage signals at PGI, VS33, and VS5 rise above the undervoltage threshold, the open-drain, power-good output (PGO) will go high after a delay of 300 ms. When the PGI voltage or any of the 3.3-V, 5-V rail drops below the undervoltage threshold, PGO will be disabled immediately.

**power-supply remote on/off ($\overline{\text{PSON}}$) and fault protect output ($\overline{\text{FPO}}$)**

Since the latest personal computer generation focuses on easy turnon and power saving functions, the PC power supply will require two characteristics. One is a dc power supply remote on/off function; the other is standby voltage to achieve very low power consumption of the PC system. Thus, the main power needs to be shut down.

The power supply remote on/off ($\overline{\text{PSON}}$) is an active-low signal that turns on all of the main power rails including the 3.3-V, 5-V, –5-V, and –12-V power rails. When this signal is held high by the PC motherboard or left open circuited, the signal of the fault protect output ($\overline{\text{FPO}}$) also goes high. Thus, the main power rails should not deliver current and should be held at 0 V.

When the $\overline{\text{FPO}}$ signal is held high due to an occurring fault condition, the fault status will be latched and the outputs of the main power rails should not deliver current and should be held at 0 V. Toggling the power-supply remote on/off ($\overline{\text{PSON}}$) from low-to-high will reset the fault-protection latch. During this fault condition only the standby power is not affected.

When $\overline{\text{PSON}}$ goes from high to low or low-to-high, the 38-ms debounce block will be active to avoid that a glitch on the input will disable/enable the $\overline{\text{FPO}}$ output. During this period, the undervoltage function is disabled to prevent turnon failure.

Power should be delivered to the rails only if the $\overline{\text{PSON}}$ signal is held at ground potential, thus, $\overline{\text{FPO}}$ is active low. The $\overline{\text{FPO}}$ pin can be connected to 5 VDC (or up to 15 VDC) through a pullup resistor.

**under-voltage protection**

The TPS3513 provides undervoltage protection (UVP) for the 12-V rail and undervoltage detect for the 3.3-V and 5-V rails. When an undervoltage condition appears at the VS12 input pin for more than 150 µs, the $\overline{\text{FPO}}$ output goes high and PGO goes low. Also, this fault condition will be latched until $\overline{\text{PSON}}$ is toggled from low-to-high or VDD is removed.

In flyback or forward type off-line switching power supplies, usually designed for small power, the overload protection design is very simple. Most of these type of power supplies are only sensing the input current for an overload condition. The trigger-point needs to be set much higher than the maximum load in order to prevent false turnon.

However, this will cause one critical issue. In case that the connected load is larger than the maximum allowable load but smaller than the trigger-point, the system will always become over-heated and cause failure and damage.

## detailed description (continued)

### overcurrent protection

In bridge or forward type, off-line switching power supplies, usually designed for medium to large power, the overload protection design needs to be very precise. Most of these types of power supplies are sensing the output current for an overload condition. The trigger-point needs to be set higher than the maximum load in order to prevent false turnon.

The TPS3513 provides overcurrent protection (OCP) for the 3.3-V, 5-V, and 12-V rails. When an over current condition appears at the OCP comparator input pins for more than 73 µs, the $\overline{FPO}$ output goes high and PGO goes low. Also, this fault condition will be latched until $\overline{PSON}$ is toggled from low-to-high or VDD is removed.

The resistor connected between the RI pin and the GND pin will introduce an accurate $I_{(ref)}$ for the OCP function. Of course, a more accurate resistor tolerance will be better. The formula for choosing the RI resistor is $V_{(RI)}/I_{(ref)}$. The $I_{(ref)}$ range is from 12.5 µA to 62.5 mA. Three OCP comparators and the $I_{(ref)}$ section are supplied by VS12. Current drawn from the VS12 pin is less than 1 mA.

Following is an example on calculating OCP for the 12-V rail:

$RI = V_{(RI)}/I_{(ref)} = 1.15\ V/20\ \mu A = 56\ K\Omega$

$I_{(ref)} \times C \times R_{(IS12)} = R_{(sense)} \times I_{(OCP\_Trip)}$

$I_{(OCP\_Trip)} = 20\ \mu A \times 8 \times 560\ \Omega/0.01\ \Omega = 9.2\ A$

C = Current ratio (see recommended operating conditions)

### overvoltage protection

The overvoltage protection (OVP) of the TPS3513 monitors 3.3 V, 5 V, and 12 V. When an overvoltage condition appears at one of the 3.3-V, 5-V, or 12-V input pins for more than 73 µs, the $\overline{FPO}$ output goes high and PGO goes low. Also, this fault condition will be latched until $\overline{PSON}$ is toggled from low-to-high or VDD is removed. During fault conditions, most power supplies have the potential to deliver higher output voltages than those normally specified or required. In unprotected equipment, it is possible for output voltages to be high enough to cause internal or external damage of the system. To protect the system under these abnormal conditions, it is common practice to provide overvoltage protection within the power supply.

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| | |
|---|---|
| Supply voltage, $V_{DD}$ (see Note1) | 16 V |
| Input voltage, $V_I$ ($\overline{PSON}$, IS5, IS33, PGI) (see Note1) | 8 V |
| Input voltage, $V_I$ (VS33, VS5) | 16 V |
| Output voltage: $V_O$ ($\overline{FPO}$) | 16 V |
| $V_O$ (PGO) | 8 V |
| All other pins (see Note 1) | –0.3 V to 16 V |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, $T_A$ | –40°C to 85°C |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |
| Soldering temperature | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| D | 956 mW | 7.65 mW/°C | 612 mW | 497 mW |
| N | 1512 mW | 12.1 mW/°C | 968 mW | 786 mW |

## recommended operating conditions at specified temperature range

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{DD}$ | | 4.5 | 15 | V |
| Input voltage, $V_I$ | $\overline{PSON}$, VS5, VS33, IS5, IS33 | | 7 | V |
| | VS12, IS12 | | 15 | |
| | PGI | | $V_{DD}$ + 0.3 V (max = 7 V) | V |
| Output voltage, $V_O$ | $\overline{FPO}$ | | 15 | V |
| | PGO | | 7 | |
| Output sink current, $I_{O(Sink)}$ | $\overline{FPO}$ | | 20 | mA |
| | PGO | | 10 | |
| Supply voltage rising time, $t_r$ | See Note 2 | 1 | | ms |
| Output current, $I_{O(RI)}$ | RI | 12.5 | 62.5 | µA |
| Operating free-air temperature range, $T_A$ | | –40 | 85 | °C |

NOTE 2: $V_{DD}$ rising and falling slew rate must be less than 14V/ms.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

### over-voltage protection and over-current protection

| | PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Overvoltage threshold | VS33 | | 3.7 | 3.9 | 4.1 | V |
| | | VS5 | | 5.7 | 6.1 | 6.5 | |
| | | VS12 | | 13.2 | 13.8 | 14.4 | |
| | Ratio of current sense sink current to current sense setting pin (RI) source current, $I_{(ref)}$ | | Resistor at RI = 30 kΩ, 0.1% resistor | 7.6 | 8 | 8.4 | |
| $I_{lkg}$ | Leakage current ($\overline{FPO}$) | | $V_{(\overline{FPO})}$ = 5 V | | | 5 | µA |
| $V_{OL}$ | Low-level output voltage ($\overline{FPO}$) | | $I_{(sink)}$ = 20 mA, $V_{DD}$ = 5 V | | | 0.7 | V |
| | Noise deglitch time OVP | | $V_{DD}$ = 5 V | 35 | 73 | 110 | µs |
| $V_{(RI)}$ | Current source reference voltage | | $V_{DD}$ = 5 V | 1.1 | 1.15 | 1.2 | V |

### undervoltage lockout section

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Start threshold voltage | | | | 4.45 | V |
| Minimum operation voltage after start-up | | 3.65 | | | V |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

### PGI and PGO

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT(PGI)}$ | Input threshold voltage | PGI1 | | 1.10 | 1.15 | 1.20 | V |
| | | PGI2 | | 0.9 | 0.95 | 1 | |
| | Undervoltage threshold | VS33 | | 2 | 2.2 | 2.4 | V |
| | | VS5 | | 3.3 | 3.5 | 3.7 | |
| | | VS12 | | 8.5 | 9 | 9.5 | |
| | Input offset voltage for OCP comparators | | | –5 | | 5 | mV |
| $I_{lkg}$ | Leakage current (PGO) | | PGO = 5 V | | | 5 | µA |
| $V_{OL}$ | Low-level output voltage (PGO) | | $I_{(sink)}$ = 10 mA, $V_{DD}$ = 4.5 V | | | 0.4 | V |
| | Short-circuit protection delay | 3.3 V, 5 V | | 49 | 75 | 114 | ms |
| $t_{d(1)}$ | Delay time | PGI to PGO | $V_{DD}$ = 5 V | 200 | 300 | 450 | ms |
| | | PGI to $\overline{\text{FPO}}$ | | 3.2 | 4.8 | 7.2 | |
| | Noise deglitch time | PGI to PGO | $V_{DD}$ = 5 V | 88 | 150 | 225 | µs |
| | | PGI to $\overline{\text{FPO}}$ | | | | | |
| | | 12-V UVP to $\overline{\text{FPO}}$ | | | | | |

### $\overline{\text{PSON}}$ control

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_I$ | Input pullup current | $\overline{\text{PSON}}$ = 0 V | | –120 | | µA |
| $V_{IH}$ | High-level input voltage | | 2.4 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 1.2 | V |
| $t_{(b)}$ | Debounce time ($\overline{\text{PSON}}$) | $V_{DD}$ = 5 V | 24 | 38 | 57 | ms |
| $t_{d(2)}$ | Delay time ($\overline{\text{PSON}}$ to $\overline{\text{FPO}}$) | $V_{DD}$ = 5 V | $t_{b+1.1}$ | $t_b$+2.3 | $t_b$+4 | ms |

### total device

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current | $\overline{\text{PSON}}$ = 5 V | | | 1 | mA |

## TYPICAL CHARACTERISTICS

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

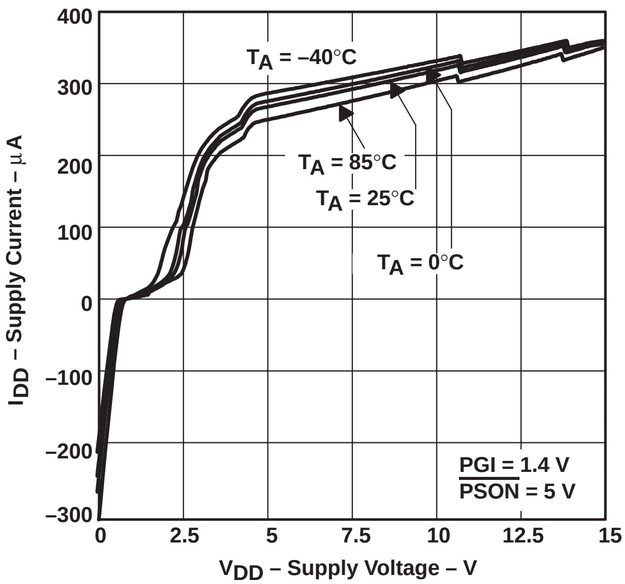



**Figure 4**

**INPUT CURRENT (PSON) vs INPUT VOLTAGE (PSON)**

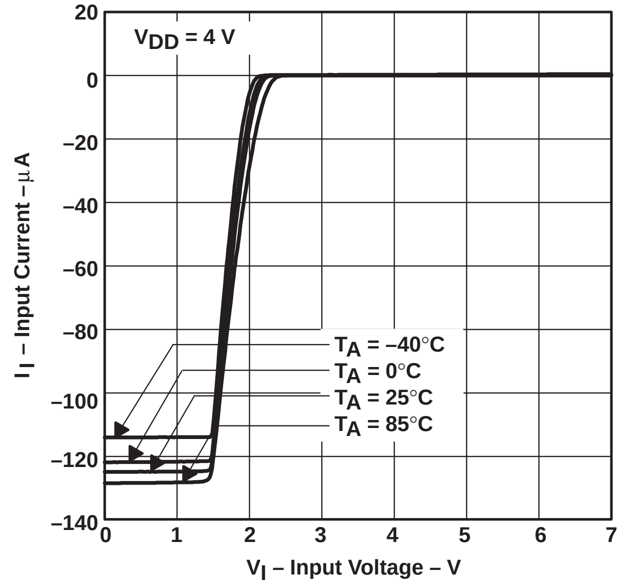



**Figure 5**

**LOW-LEVEL OUTPUT VOLTAGE (FPO) vs LOW-LEVEL OUTPUT CURRENT (FPO)**

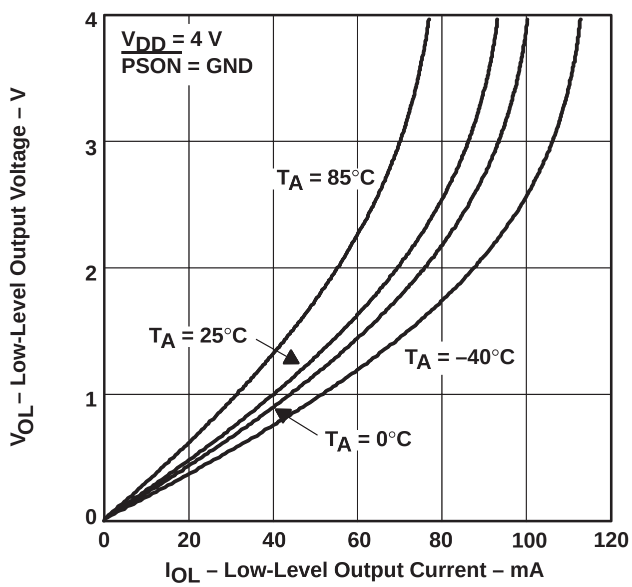



**Figure 6**

**LOW-LEVEL OUTPUT VOLTAGE (FPO) vs LOW-LEVEL OUTPUT CURRENT (FPO)**

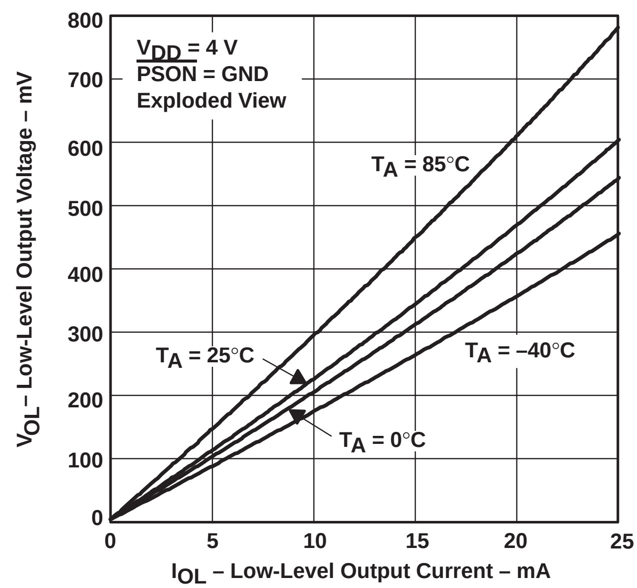



**Figure 7**

## TYPICAL CHARACTERISTICS

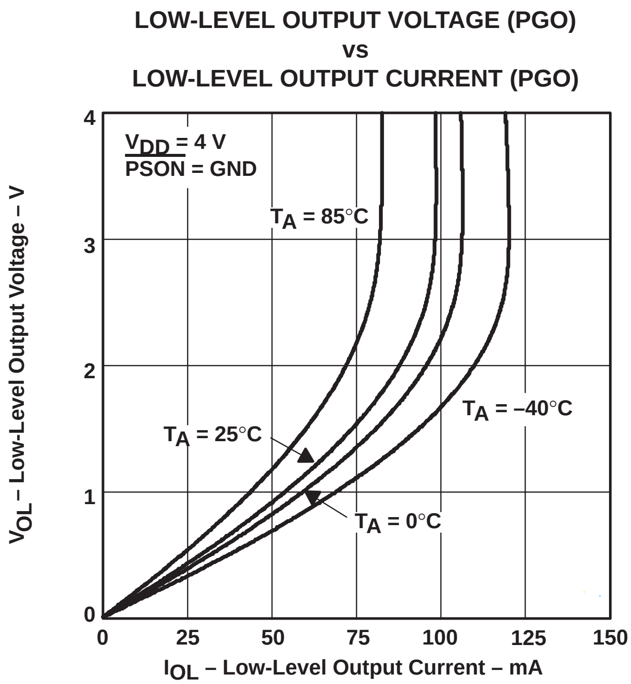



Figure 8

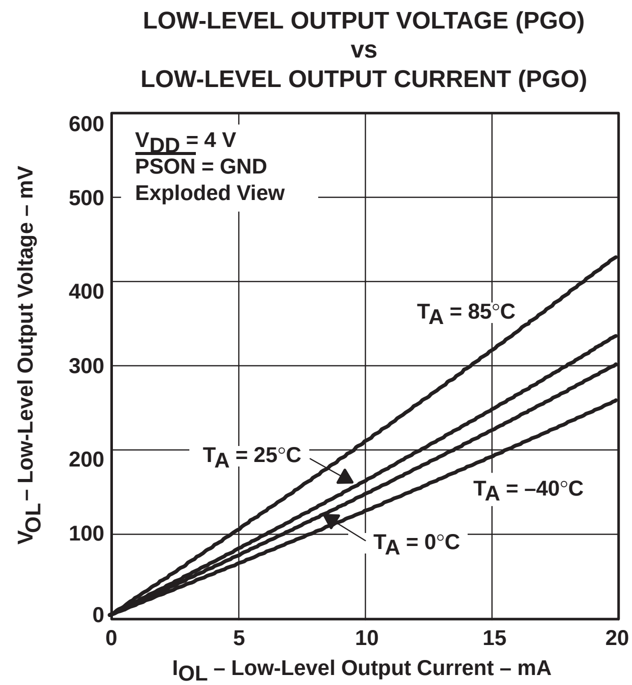



Figure 9

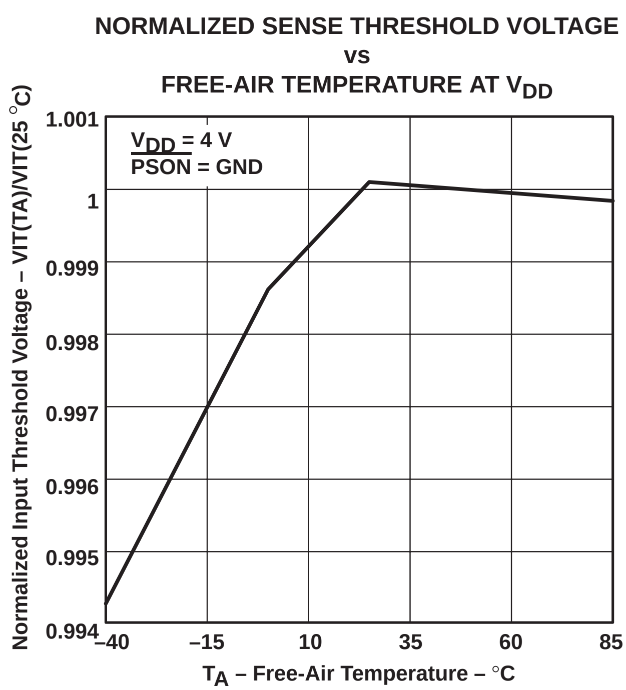



Figure 10

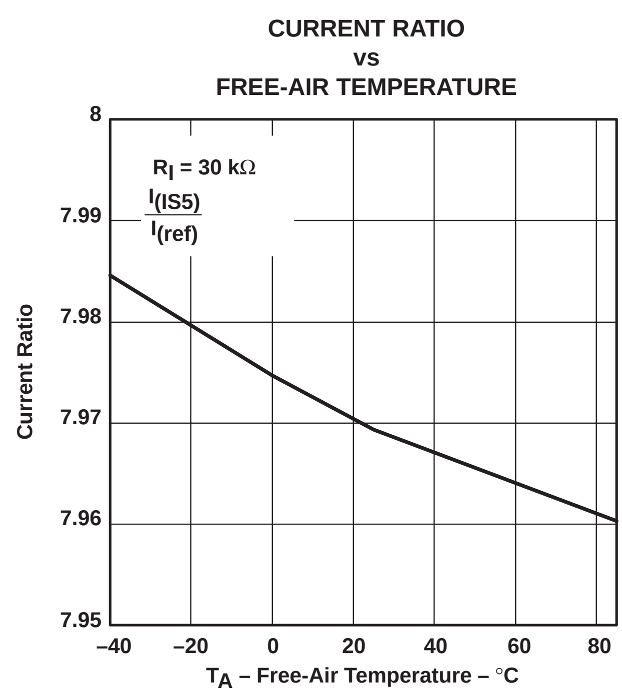


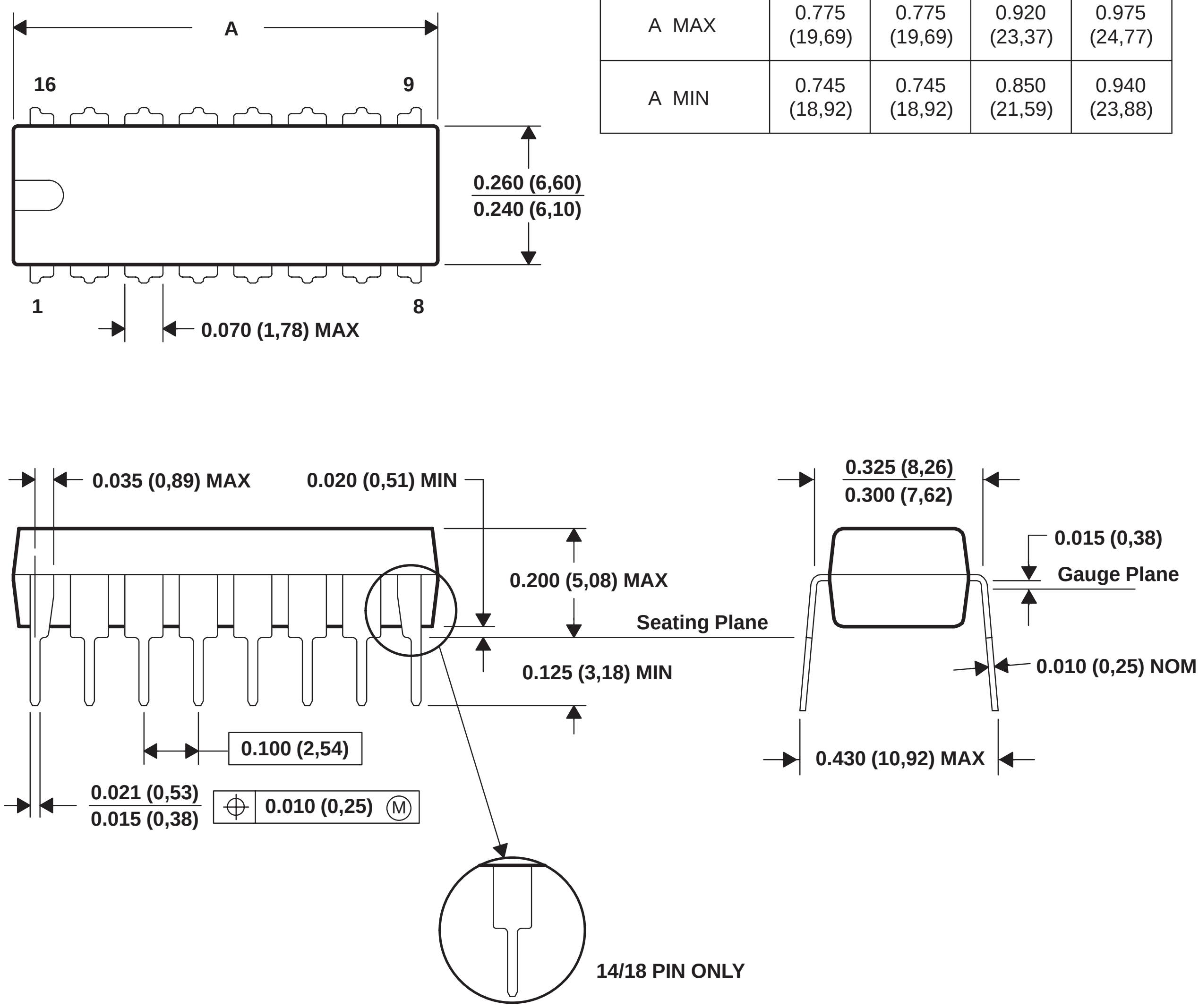

Figure 11

## MECHANICAL DATA

**N (R-PDIP-T**)** **PLASTIC DUAL-IN-LINE PACKAGE**

**16 PINS SHOWN**

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 0.975 (24,77) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |



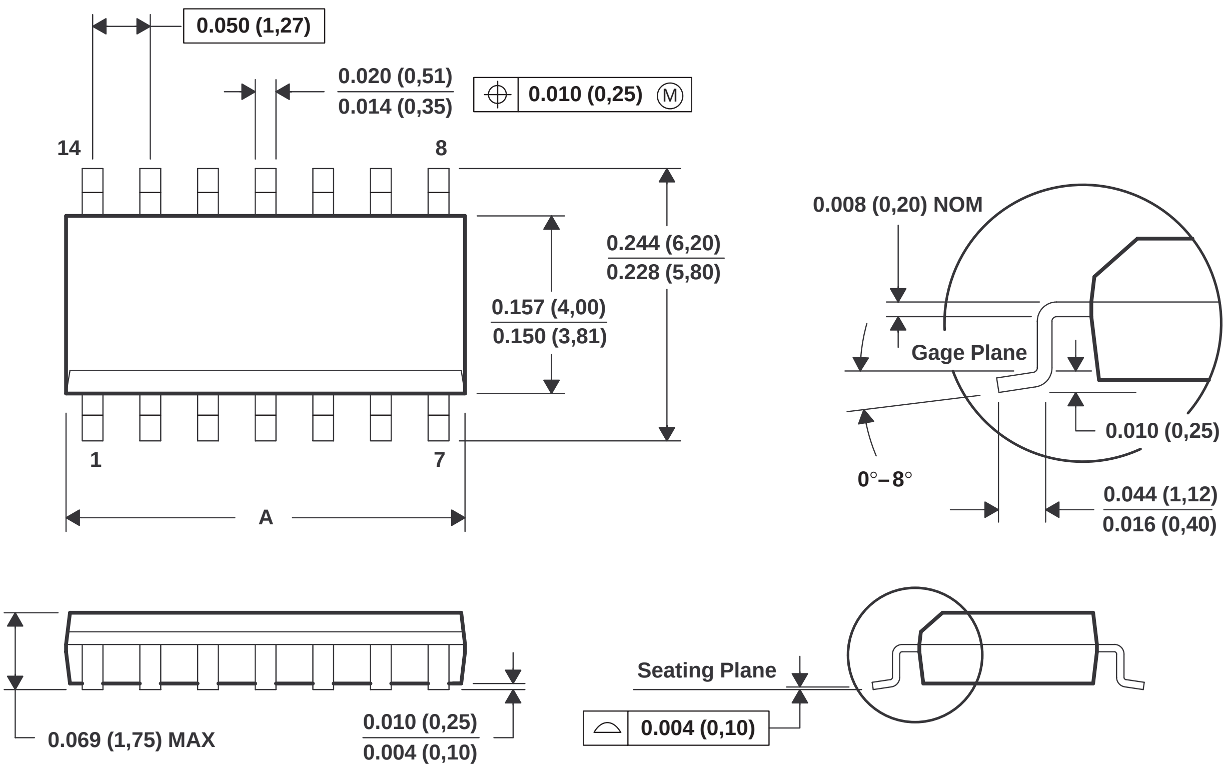

4040049/D 02/00

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).

## MECHANICAL DATA (CONTINUED)

**D (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| PINS ** / DIM | 8 | 14 | 16 |
|---|---|---|---|
| A MAX | 0.197 (5,00) | 0.344 (8,75) | 0.394 (10,00) |
| A MIN | 0.189 (4,80) | 0.337 (8,55) | 0.386 (9,80) |

4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

## IMPORTANT NOTICE



Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265