ULTRALOW-NOISE, HIGH PSRR, FAST RF 250-mA LOW-DROPOUT LINEAR REGULATORS

FEATURES

- **250-mA Low-Dropout Regulator With EN**
- **Available in 1.8-V, 2.5-V, 2.8-V, 3-V, 3.3 V, and Adjustable**
- **High PSRR (65 dB at 10 kHz)**
- **Ultralow Noise (32 μV)**
- **Fast Start-Up Time (50 μs)**
- **Stable With a 2.2-μF Ceramic Capacitor**
- **Excellent Load/Line Transient**
- **Very Low Dropout Voltage (155 mV at Full Load, TPS79430)**
- **Available in MSOP8 and SOT223-6 Packages**

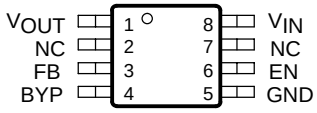
APPLICATIONS

- **Cellular and Cordless Telephones**
- **VCOs**
- **RF**
- **Bluetooth™, Wireless LAN**
- **Handheld Organizers, PDA**

DESCRIPTION

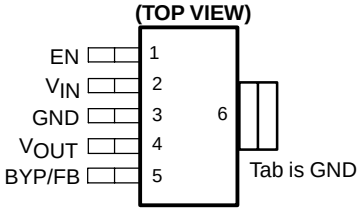
The TPS794xx family of low-dropout (LDO) low-power linear voltage regulators features high power supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in small outline, MSOP8 PowerPAD™ and SOT223–6, packages. Each device in the family is stable with a small 2.2-μF ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (e.g., 155 mV at 250 mA, TPS79430). Each device achieves fast start-up times (approximately 50 μs with a 0.001-μF bypass capacitor) while consuming very low quiescent current (170 μA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 μA. The TPS79428 exhibits approximately 32 μV_{RMS} of output voltage noise with a 0.1-μF bypass capacitor. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR and low noise features as well as the fast response time.

DGN PACKAGE
MSOP PowerPAD
(TOP VIEW)

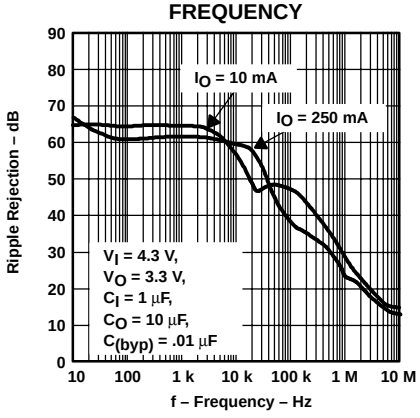


NC – No internal connection

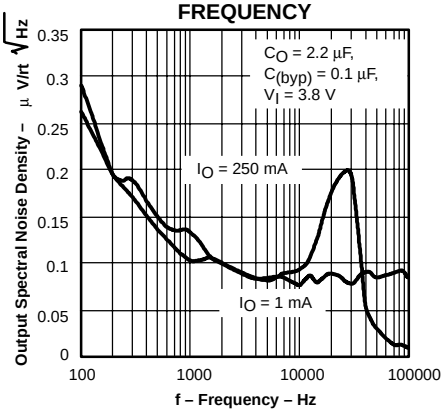
DCQ PACKAGE
SOT223-6
(TOP VIEW)



TPS79433
RIPPLE REJECTION
vs
FREQUENCY



TPS79428
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_J	VOLTAGE	PACKAGE	PART NUMBER(1, 2)	SYMBOL
–40°C to 125°C	Adjustable	MSOP	TPS79401DGNR	AXL
			TPS79401DGNT	
		SOT223-6	TPS79401DCQR	PS79401
			TPS79401DCQ	
	1.8 V	MSOP	TPS79418DGNR	AXM
			TPS79418DGNT	
		SOT223-6	TPS79418DCQR	PS79418
			TPS79418DCQ	
	2.5 V	MSOP	TPS79425DGNR	AYB
			TPS79425DGNT	
		SOT223-6	TPS79425DCQR	PS79425
			TPS79425DCQ	
	2.8 V	MSOP	TPS79428DGNR	AYC
			TPS79428DGNT	
		SOT223-6	TPS79428DCQR	PS79428
			TPS79428DCQ	
	3 V	MSOP	TPS79430DGNR	AYD
			TPS79430DGNT	
		SOT223-6	TPS79430DCQR	PS79430
			TPS79430DCQ	
	3.3 V	MSOP	TPS79433DGNR	AYE
			TPS79433DGNT	
		SOT223-6	TPS79433DCQR	PS79433
			TPS79433DCQ	

(1) The DGNR and DCQR indicates tape and reel of 2500 parts.

(2) The DGNT indicates tape and reel of 250 parts.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

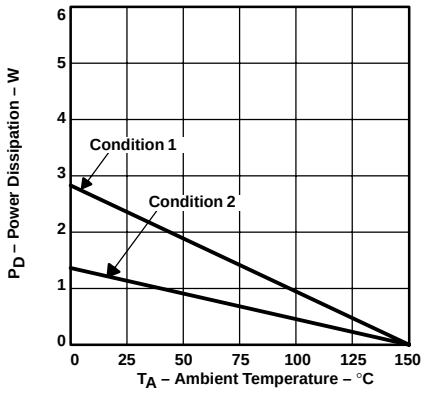
	TPS79401, TPS79425, TPS79418 TPS79428, TPS79430, TPS79433
Input voltage range(2)	–0.3 V to 6 V
Voltage range at EN	–0.3 V to V_I + 0.3 V
Voltage on OUT	–0.3 V to 6 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
ESD rating, CDM	500 V
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

PACKAGE DISSIPATION RATINGS

PACKAGE	AIR FLOW (CFM)	$R_{\theta JC}$ (°C/W)	$R_{\theta JA}$ (°C/W)	$T_A \le 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGN	0	8.47	55.09	2.27 W	1.45 W	1.18 W
	150	8.21	49.97	2.50 W	1.60 W	1.30 W
	250	8.20	48.10	2.60 W	1.66 W	1.35 W



CONDITIONS	PACKAGE	PCB AREA	θJA
1	SOT223	4in² Top Side Only	53°C/W
2	SOT223	0.5in² Top Side Only	110°C/W

Figure 1. SOT223 Power Dissipation

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range EN = V_I, T_J = –40 to 125 °C, $V_I = V_{O(typ)} + 1$ V, I_O = 1 mA, C_O = 10 µF, $C_{(byp)}$ = 0.01 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I Input voltage(1)				2.7		5.5	V
I_O Continuous output current(2)				0		250	mA
T_J Operating junction temperature				–40		125	°C
Output voltage	TPS79401	T_J = 25°C			V_O		V
		0 µA < I_O < 250 mA,	1.22 V ≤ V_O ≤ 5.5 V(3)	0.97 V_O		1.03 V_O	
	TPS79418	T_J = 25°C			1.8		
		0 µA < I_O < 250 mA,	2.8 V ≤ V_I ≤ 5.5 V	1.746		1.854	
	TPS79425	T_J = 25°C			2.5		
		0 µA < I_O < 250 mA,	3.5 V < V_I < 5.5 V	2.425		2.575	
	TPS79428	T_J = 25°C			2.8		
		0 µA < I_O < 250 mA,	3.8 V < V_I < 5.5 V	2.716		2.884	
	TPS79430	T_J = 25°C			3		
		0 µA < I_O < 250 mA,	4 V < V_I < 5.5 V	2.91		3.09	
	TPS79433	T_J = 25°C			3.3		
		0 µA < I_O < 250 mA,	4.3 V < V_I < 5.5 V	3.201		3.399	
Quiescent current (GND current)		0 µA < I_O < 250 mA,	T_J = 25°C		170		µA
		0 µA < I_O < 250 mA				220	
Load regulation		0 µA < I_O < 250 mA,	T_J = 25°C		10		mV

(1) To calculate the minimum input voltage for your maximum output current, use the following formula: $V_I(min) = V_O(max) + V_{DO}$ (max load)
(2) Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.
(3) The minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. The maximum IN voltage is 5.5 V. The maximum continuous output current is 250 mA.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range EN = V_I, T_J = –40 to 125 °C, V_I = $V_{O(typ)}$ + 1 V, I_O = 1 mA, C_o = 10 µF, $C_{(byp)}$ = 0.01 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage line regulation ($\Delta V_O/V_O$)(4)		V_O + 1 V < V_I ≤ 5.5 V, T_J = 25°C			0.05		%/V
		V_O + 1 V < V_I ≤ 5.5 V				0.12	
Output noise voltage (TPS79428)		BW = 100 Hz to 100 kHz, I_O = 250 mA, T_J = 25°C	$C_{(byp)}$ = 0.001 µF		55		μV_{RMS}
			$C_{(byp)}$ = 0.0047 µF		36		
			$C_{(byp)}$ = 0.01 µF		33		
			$C_{(byp)}$ = 0.1 µF		32		
Time, start-up (TPS79428)		R_L – 14 Ω, C_o = 1 µF, T_J = 25°C	$C_{(byp)}$ = 0.001 µF		50		µs
			$C_{(byp)}$ = 0.0047 µF		70		
			$C_{(byp)}$ = 0.01 µF		100		
Output current limit		V_O = 0 V(3)			925		mA
Standby current		EN = 0 V,	2.7 V < V_I < 5.5 V		0.07	1	µA
High level enable input voltage		2.7 V < V_I < 5.5 V		2			V
Low level enable input voltage		2.7 V < V_I < 5.5 V				0.7	V
Input current (EN)		EN = 0		–1		1	µA
Input current (FB)		FB = 1.8 V				1	µA
Power supply ripple rejection	TPS79428	f = 100 Hz, T_J = 25°C,	I_O = 10 mA		65		dB
		f = 100 Hz, T_J = 25°C,	I_O = 250 mA		65		
		f = 10 kHz, T_J = 25°C,	I_O = 250 mA		60		
		f = 100 kHz, T_J = 25°C,	I_O = 250 mA		40		
Dropout voltage(5)	TPS79428	I_O = 250 mA,	T_J = 25°C		155		mV
		I_O = 250 mA				210	
	TPS79430	I_O = 250 mA, T_J = 25°C			155		
		I_O = 250 mA				210	
	TPS79433	I_O = 250 mA, T_J = 25°C			145		mV
		I_O = 250 mA				200	
UVLO threshold		V_{CC} rising		2.25		2.65	V
UVLO hysteresis		T_J = 25°C, V_{CC} rising			100		mV

(4) If V_O ≤ 2.5 V then V_{Imin} = 2.7 V, V_{Imax} = 5.5 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - 2.7\ V\right)}{100} \times 1000$$

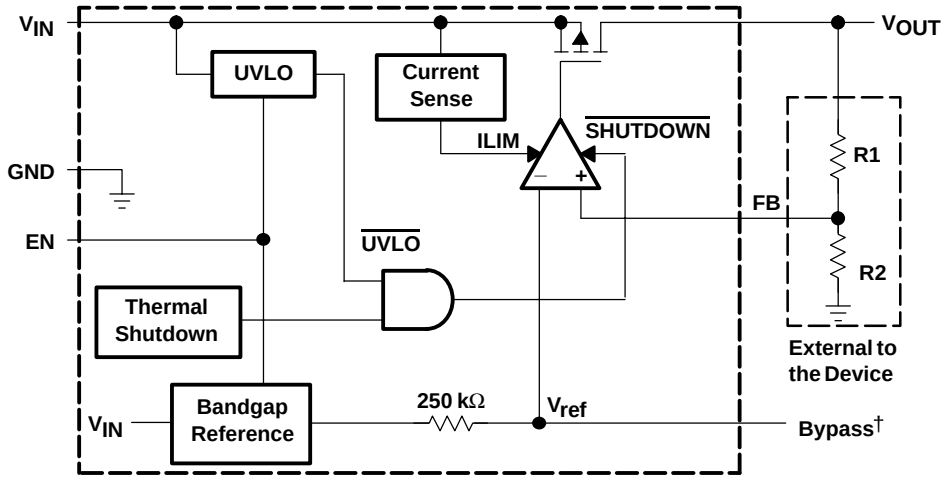
If V_O ≥ 2.5 V then V_{Imin} = V_O + 1 V, V_{Imax} = 5.5 V.

(5) IN voltage equals V_O(typ) – 100 mV; The TPS78418 and TPS79425 dropout voltage are limited by the input voltage range limitations.

Terminal Functions

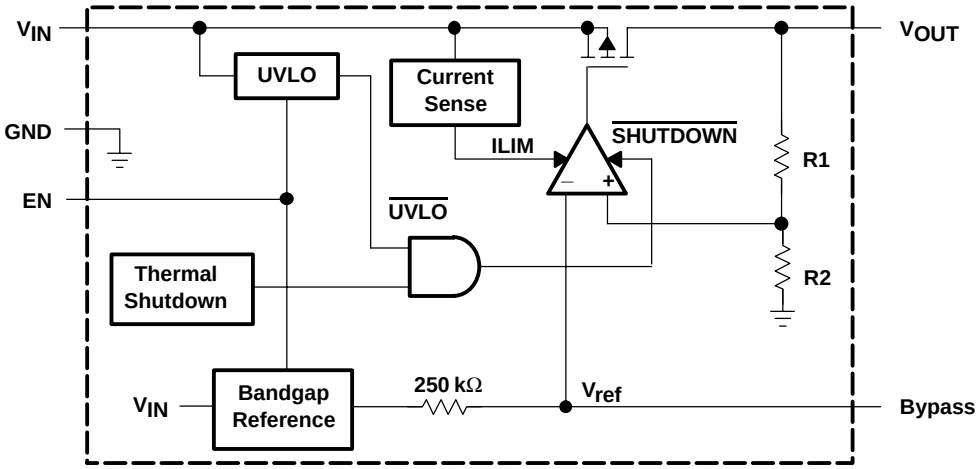
TERMINAL			I/O	DESCRIPTION
NAME	DGN (MSOP)	DCQ (SOT223)		
BYP	4	5		An external bypass capacitor, connected to this terminal, in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise. Not available on the TPS79401DCQ package.
EN	6	1	I	The EN terminal is an input which enables or shuts down the device. When EN goes to a logic high, the device is enabled. When the device goes to a logic low, the device is in shutdown mode.
FB	3	5	I	This terminal is the feedback input voltage for the adjustable device.
GND	5	3, 6		Regulator ground
V_{IN}	8	2	I	The V_{IN} terminal is the input to the device.
NC	2, 7			Regulator ground
V_{OUT}	1	4	O	The V_{OUT} terminal is the regulated output of the device.

FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION



† Not Available on the DCQ package.

FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION



TYPICAL CHARACTERISTICS

TPS79433
OUTPUT VOLTAGE vs OUTPUT CURRENT

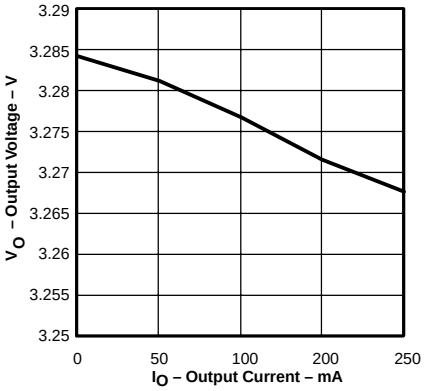


Figure 2

TPS79428
OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

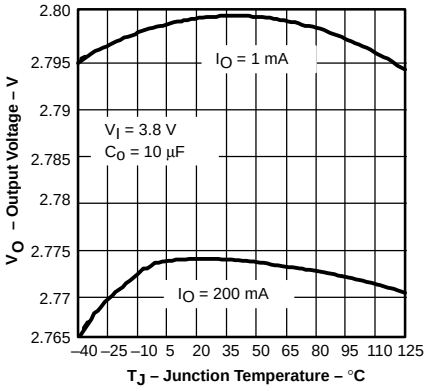


Figure 3

TPS79428
GROUND CURRENT vs FREE-AIR TEMPERATURE

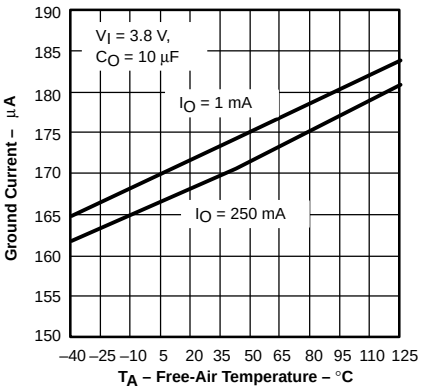


Figure 4

TPS79428
OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

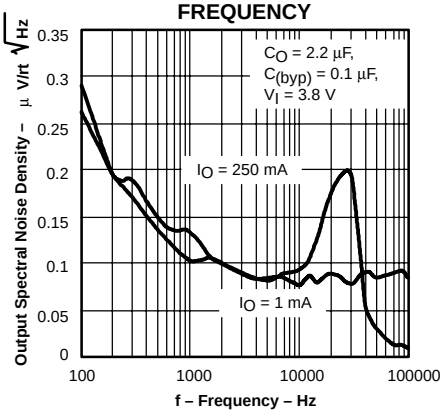


Figure 5

TPS79428
OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

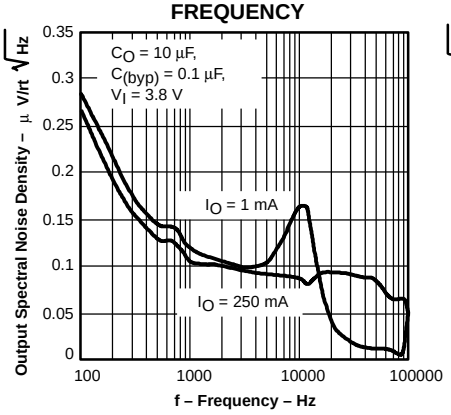


Figure 6

TPS79428
OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

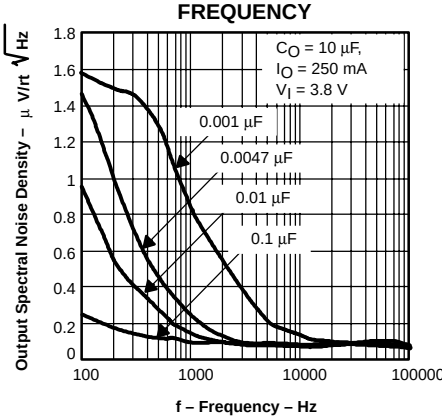


Figure 7

TPS79428
ROOT MEAN SQUARED OUTPUT NOISE vs BYPASS CAPACITOR

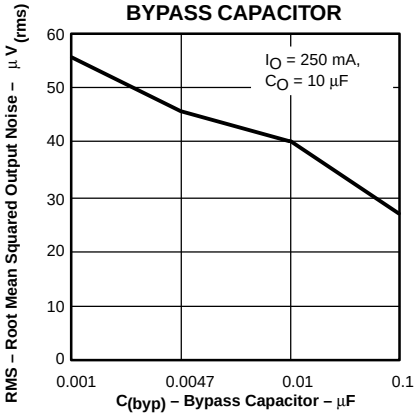


Figure 8

TPS79433
OUTPUT IMPEDANCE vs FREQUENCY

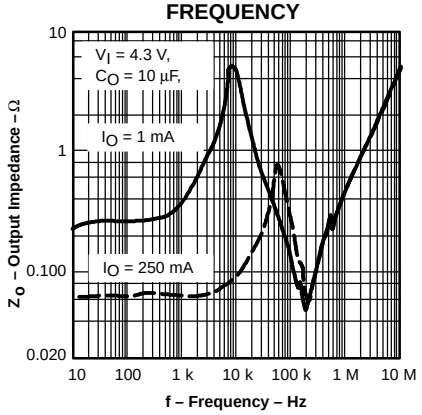


Figure 9

TPS79428
DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

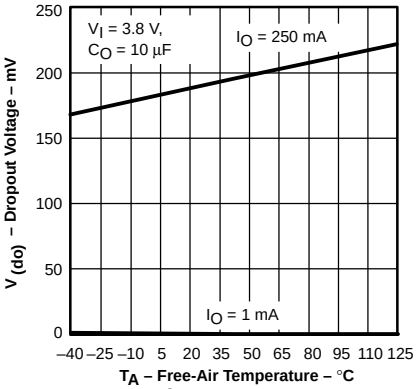


Figure 10

TYPICAL CHARACTERISTICS

TPS79433
RIPPLE REJECTION
vs
FREQUENCY

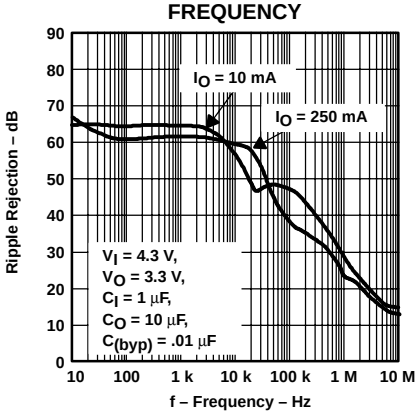


Figure 11

TPS79433
RIPPLE REJECTION
vs
FREQUENCY

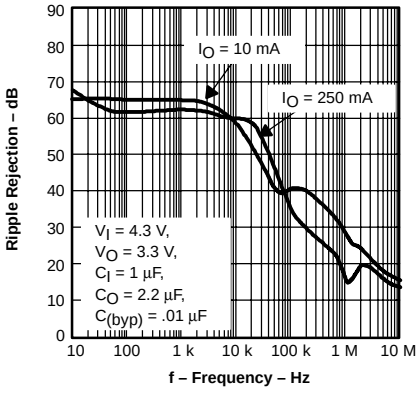


Figure 12

TPS79433
RIPPLE REJECTION
vs
FREQUENCY

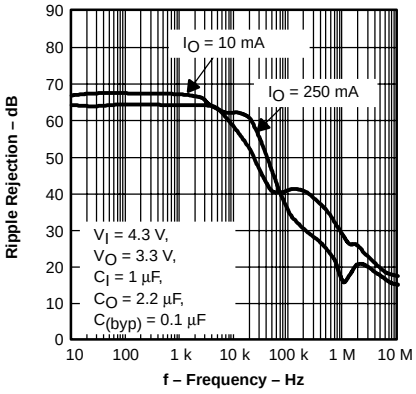


Figure 13

TPS79433
OUTPUT VOLTAGE, ENABLE VOLTAGE
vs
TIME (START-UP)

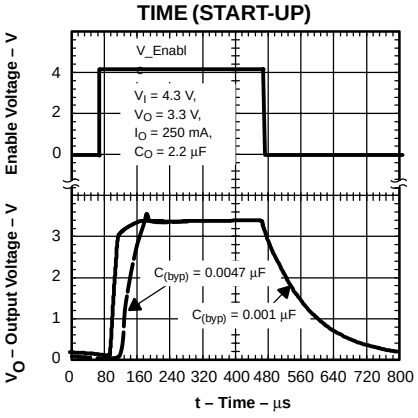


Figure 14

TPS79433
LINE TRANSIENT RESPONSE

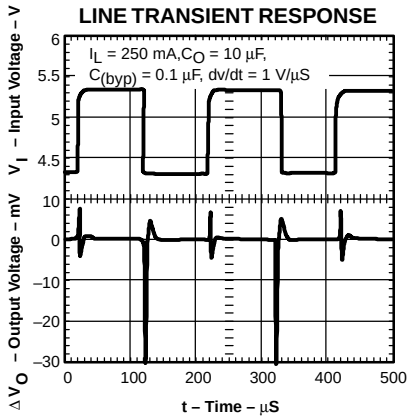


Figure 15

TPS79433
LOAD TRANSIENT RESPONSE

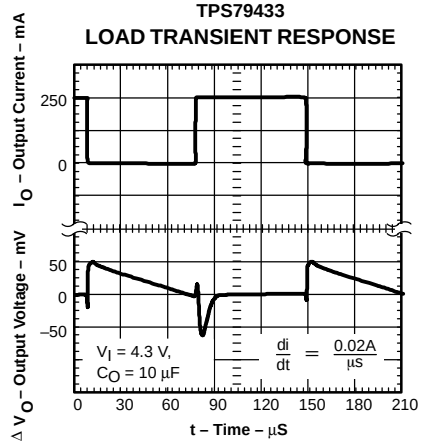


Figure 16

TPS79425
POWER UP / POWER DOWN

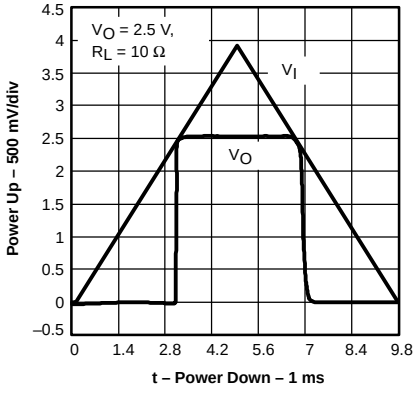


Figure 17

TYPICAL CHARACTERISTICS

TPS79433
DROPOUT VOLTAGE vs OUTPUT CURRENT

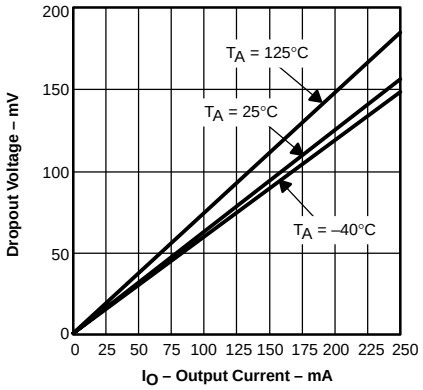


Figure 18

TPS79401
DROPOUT VOLTAGE vs INPUT VOLTAGE

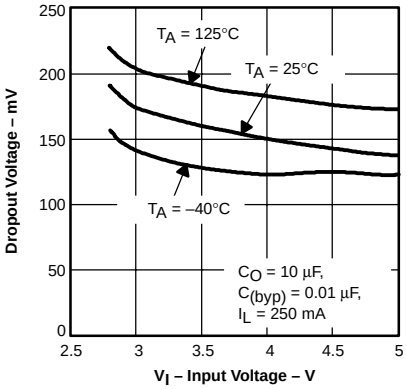


Figure 19

MINIMUM INPUT VOLTAGE vs OUTPUT VOLTAGE

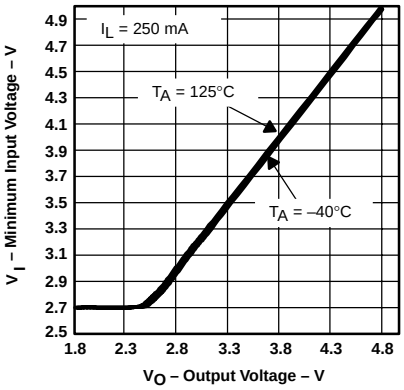


Figure 20

TPS79428
TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

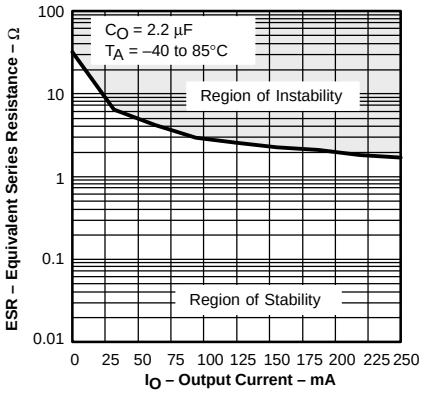


Figure 21

TPS79428
TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

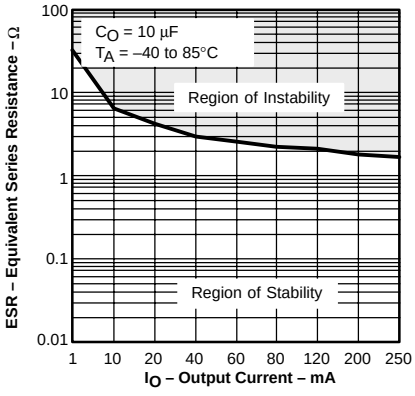
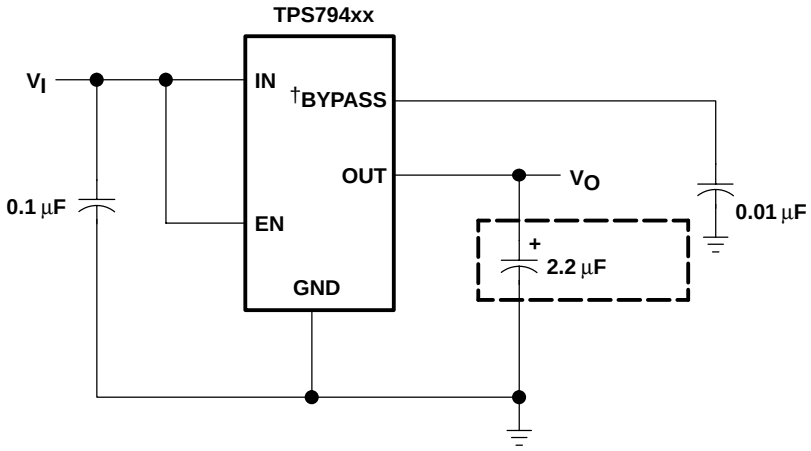


Figure 22

APPLICATION INFORMATION

The TPS794xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 μA typically), and enable input to reduce supply currents to less than 1 μA when the regulator is turned off.

A typical application circuit is shown in Figure 23.



† Not Available on the TPS79401 in the SOT223–6 package.

Figure 23. Typical Application Circuit

EXTERNAL CAPACITOR REQUIREMENTS

A 0.1-μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS794xx, is required for stability. It improves transient response, noise rejection, and ripple rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS794xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 2.2 μF. Any 2.2 μF or larger ceramic capacitor is suitable.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS794xx has a BYPASS pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the BYPASS pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the BYPASS pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current.

For example, the TPS79428 exhibits only 32 μV_{RMS} of output voltage noise using a 0.1-μF ceramic bypass capacitor and a 2.2-μF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 250-kΩ resistor and external capacitor.

BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

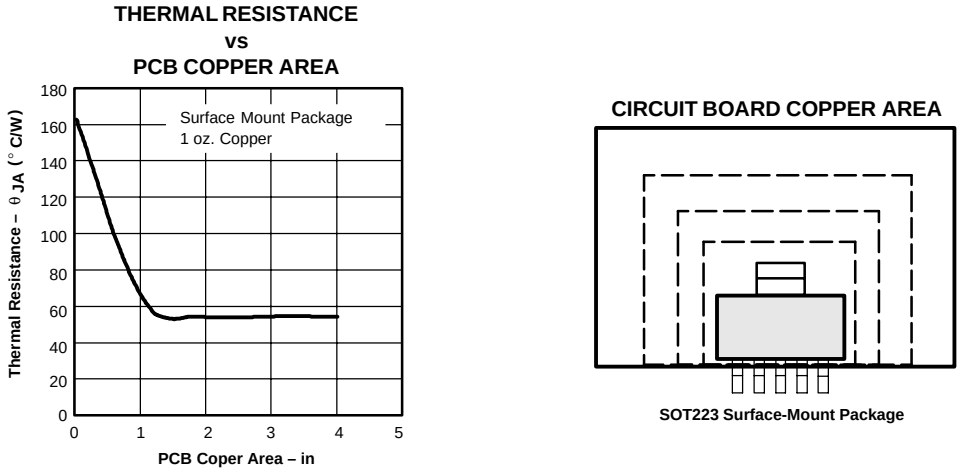


Figure 24. Thermal Resistance vs PCB Area for the Five Lead SOT-223.

POWER DISSIPATION AND JUNCTION TEMPERATURE

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (1)$$

where:

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package. See power dissipation table and Figure 1.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O \quad (2)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

REGULATOR MOUNTING

The tab of the SOT223-6 package is electrically connected to ground. For best thermal performance, the tab of the surface-mount version should be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

Although the tab of the SOT223–6 is electrically grounded, it is not intended to carry any current. The copper pad that acts as a heat sink should be isolated from the rest of the circuit to prevent current flow through the device from the tab to the ground pin. Solder pad footprint recommendations for the devices are presented in an application bulletin *Solder Pad Recommendations for Surface-Mount Devices*, literature number AB–132, available from the TI web site (www.ti.com).

PROGRAMMING THE TPS79401 ADJUSTABLE LDO REGULATOR

The output voltage of the TPS79401 adjustable regulator is programmed using an external resistor divider as shown in Figure 25. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

where

V_{ref} = 1.2246 V typ (the internal reference voltage)

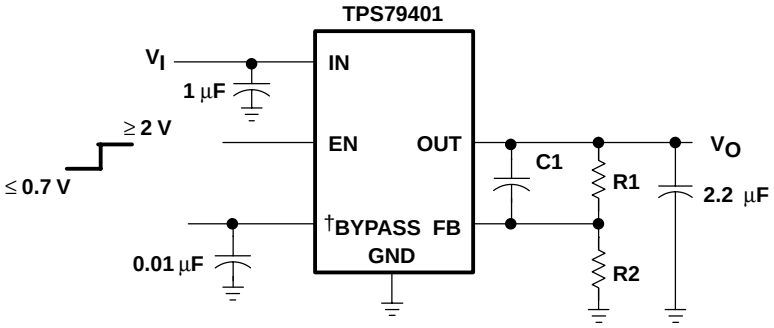
Resistors R1 and R2 should be chosen for approximately 40-μA divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided as leakage current at FB increases the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 40 μA, C1 = 15 pF for stability, and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (4)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. For voltages <1.8 V, the value of this capacitor should be 100 pF. For voltages >1.8 V, the approximate value of this capacitor can be calculated as:

$$C1 = \frac{(3 \times 10^{-7}) \times (R1 + R2)}{(R1 \times R2)} \quad (5)$$

The suggested value of this capacitor for several resistor ratios is shown in the table below. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage <1.8 V is chosen, then the minimum recommended output capacitor is 4.7 μF instead of 2.2 μF.



† Not Available on the DCQ package.

OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	C1
2.5 V	31.6 kΩ	30.1 kΩ	22 pF
3.3 V	49.9 kΩ	30.1 kΩ	15 pF
3.6 V	59 kΩ	30.1 kΩ	15 pF

Figure 25. TPS79401 Adjustable LDO Regulator Programming

REGULATOR PROTECTION

The TPS794xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS794xx features internal current limiting and thermal protection. During normal operation, the TPS794xx limits output current to approximately 925 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage rating of the device. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

TEXAS INSTRUMENTS
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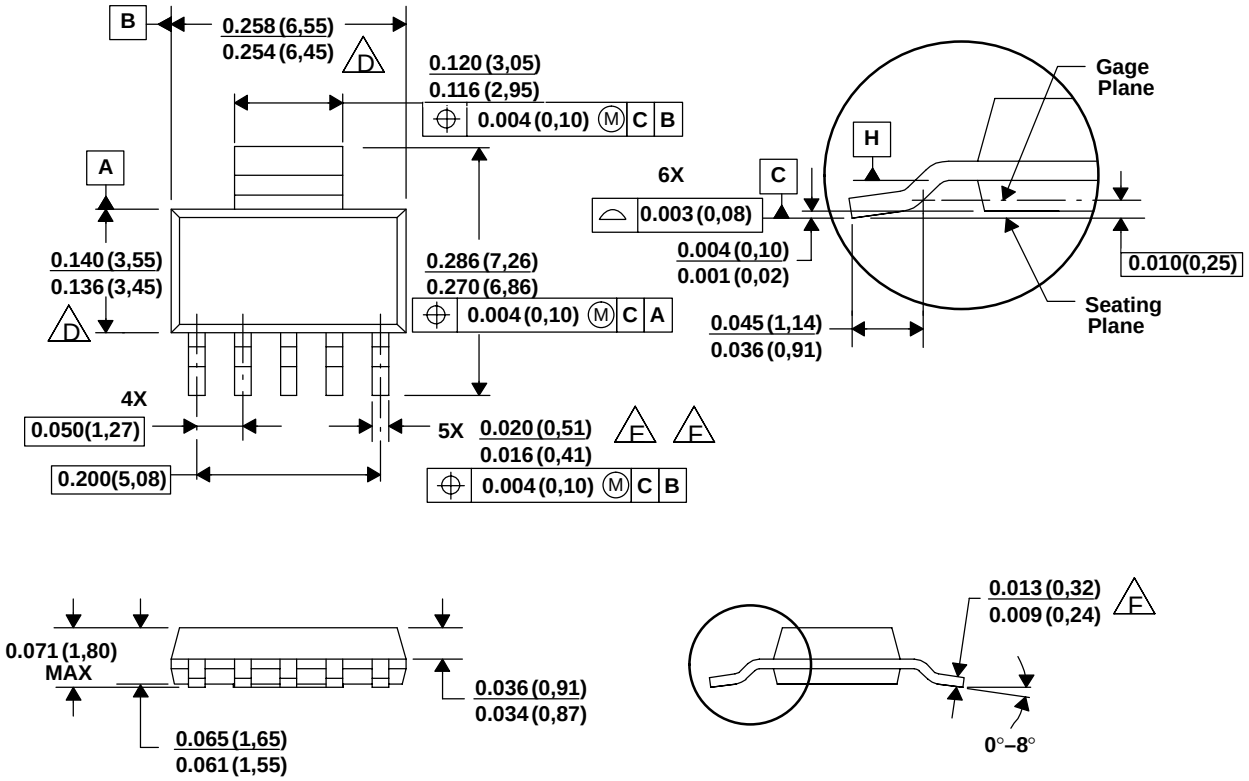
MECHANICAL DATA

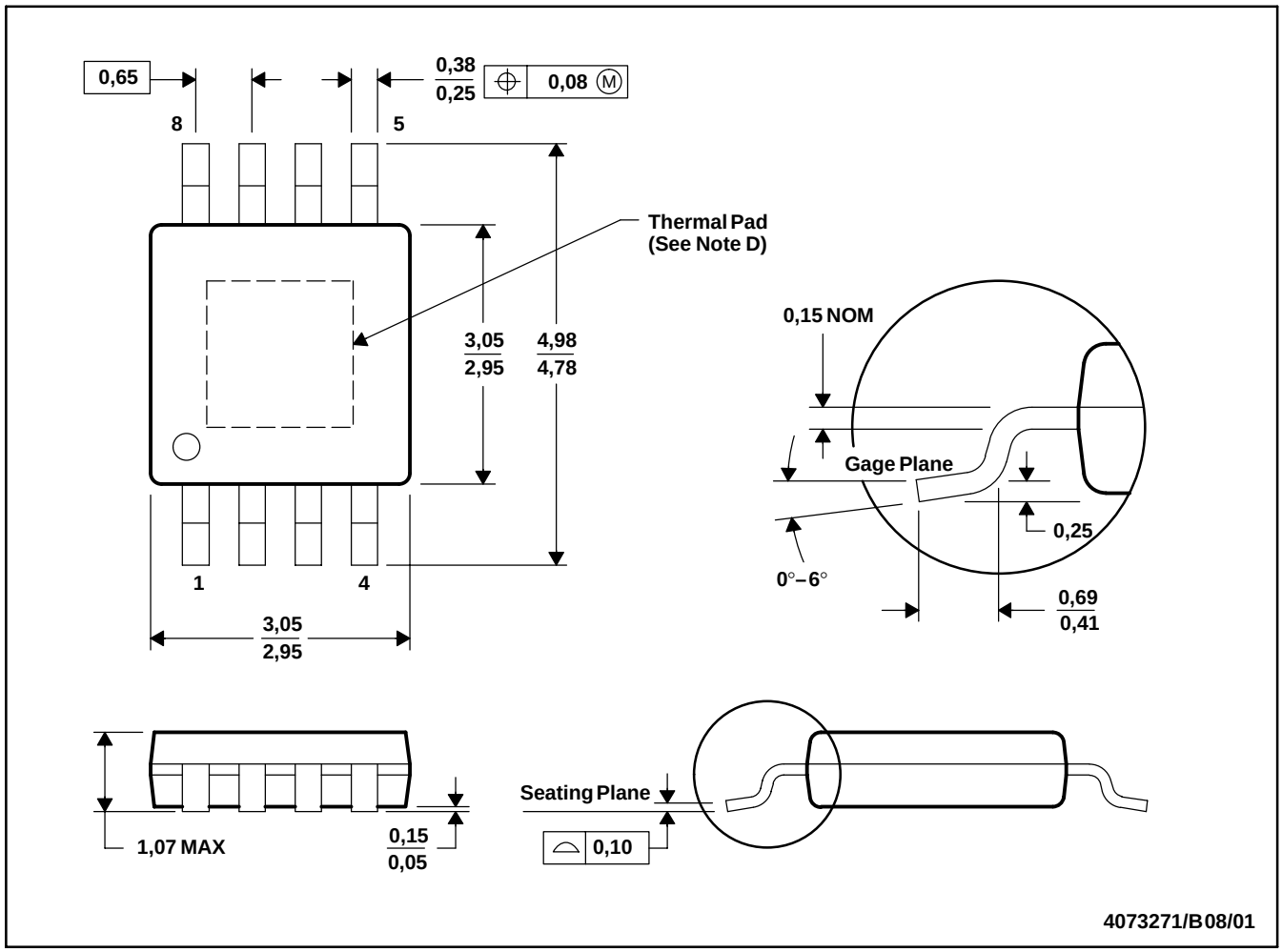
DCQ (R-PDSO-G6) **PLASTIC SMALL-OUTLINE**



NOTES:A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Controlling dimension in inches
D. Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
E. Lead width dimensions does not include dambar protrusion.
F. Lead width and thickness dimensions apply to solder plated leads.
G. Interlead flash allow 0.008 inch max.
H. Gate burr/protrusion max. 0.006 inch.

MECHANICAL DATA

DGN (S-PDSO-G8) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**



NOTES:A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-187

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

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