128M X 72 Bits (1GB) SDRAM 168-Pin Registered DIMM ECC (PC133)

FEATURES

- PC133 Compliant (t_{CYC}=7.5ns@CL=3)
- Burst Mode Operation
- Auto and self refresh capability (8192 cycles/64ms refresh)
- LVTTL compatible inputs and outputs
- +3.3V ± 0.3V power supply
- MRS cycle with address key programs
  - CAS Latency (CL=2 or 3)
  - Burst Length (1, 2, 4, 8)
  - Data Type (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with 256 Byte EEPROM
- ECC

GENERAL DESCRIPTION

The SimpleTech SL72R4L128M8H-A75AV is a 128M x 72 bits Synchronous Dynamic RAM (SDRAM) Dual In-line Memory Module (DIMM).

This module consists of thirty-six CMOS 16M x 4 bits x 4 banks SDRAMs in 54-pin 400-mil TSOP-II packages. The SDRAMs are mounted in stacks of two on a 168-pin glass epoxy substrate using the patented IC Tower stacking technology (Patent Number RE.36,916).

A serial EEPROM using the two pin I^2C protocol is also mounted to provide for the Serial Presence Detects (SPD). PLL circuits supply clocks to the SDRAMs. Decoupling capacitors are also mounted. Damping resistors are added to the data signals. Control and address signals are registered.

The module has gold edge connections and is intended for mounting into 168-pin DIMM edge connector sockets keyed for 3.3V power supply.

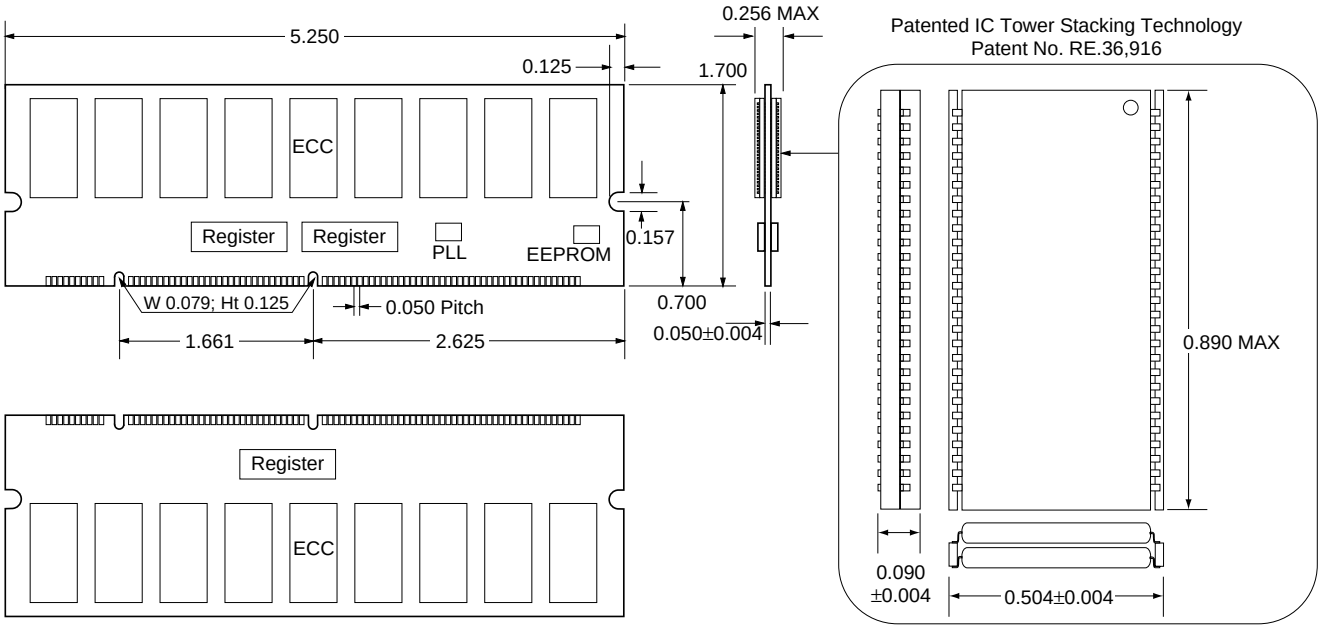
The module is PC133 compliant.

ORDERING INFORMATION

SimpleTech Part Number	Performance				
	CL	t_{RCD}	t_{RP}	t_{RC}	Comment
SL72R4L128M8H-A75AV	3clks	20ns	20ns	67.5ns	PC133 133MHz Parameters

MODULE DIMENSIONS

Units are in inches. Tolerances are ±0.005 unless otherwise specified.



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PIN CONFIGURATION

Pin Symbols

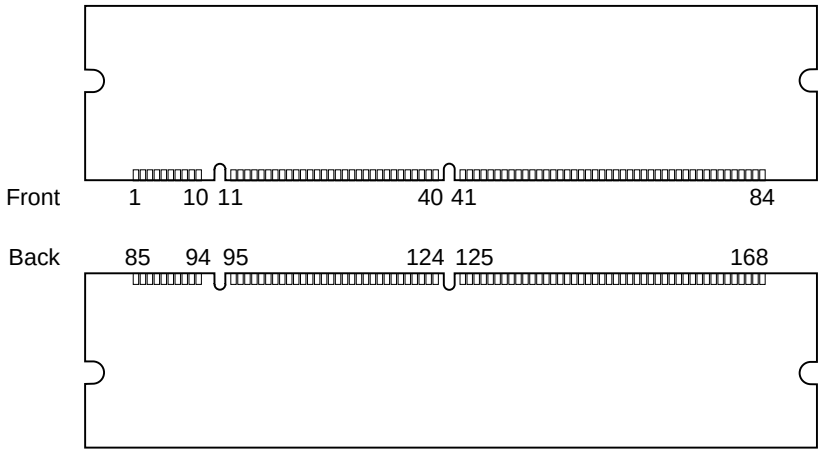
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	NC	49	V_{DD}	73	V_{DD}	97	DQ_{41}	121	A_9	145	NC
2	DQ_0	26	V_{DD}	50	NC	74	DQ_{28}	98	DQ_{42}	122	BA_0	146	NC
3	DQ_1	27	$\overline{WE}$	51	NC	75	DQ_{29}	99	DQ_{43}	123	A_{11}	147	REGE
4	DQ_2	28	$DQMB_0$	52	CB_2	76	DQ_{30}	100	DQ_{44}	124	V_{DD}	148	V_{SS}
5	DQ_3	29	$DQMB_1$	53	CB_3	77	DQ_{31}	101	DQ_{45}	125	CK_1	149	DQ_{53}
6	V_{DD}	30	$\overline{S}_0$	54	V_{SS}	78	V_{SS}	102	V_{DD}	126	A_{12}	150	DQ_{54}
7	DQ_4	31	NC	55	DQ_{16}	79	CK_2	103	DQ_{46}	127	V_{SS}	151	DQ_{55}
8	DQ_5	32	V_{SS}	56	DQ_{17}	80	NC	104	DQ_{47}	128	CKE_0	152	V_{SS}
9	DQ_6	33	A_0	57	DQ_{18}	81	NC	105	CB_4	129	$\overline{S}_3$	153	DQ_{56}
10	DQ_7	34	A_2	58	DQ_{19}	82	SDA	106	CB_5	130	$DQMB_6$	154	DQ_{57}
11	DQ_8	35	A_4	59	V_{DD}	83	SCL	107	V_{SS}	131	$DQMB_7$	155	DQ_{58}
12	V_{SS}	36	A_6	60	DQ_{20}	84	V_{DD}	108	NC	132	A_{13}*	156	DQ_{59}
13	DQ_9	37	A_8	61	NC	85	V_{SS}	109	NC	133	V_{DD}	157	V_{DD}
14	DQ_{10}	38	A_{10}/AP	62	NC	86	DQ_{32}	110	V_{DD}	134	NC	158	DQ_{60}
15	DQ_{11}	39	BA_1	63	CKE_1	87	DQ_{33}	111	$\overline{CAS}$	135	NC	159	DQ_{61}
16	DQ_{12}	40	V_{DD}	64	V_{SS}	88	DQ_{34}	112	$DQMB_4$	136	CB_6	160	DQ_{62}
17	DQ_{13}	41	V_{DD}	65	DQ_{21}	89	DQ_{35}	113	$DQMB_5$	137	CB_7	161	DQ_{63}
18	V_{DD}	42	CK_0	66	DQ_{22}	90	V_{DD}	114	$\overline{S}_1$	138	V_{SS}	162	V_{SS}
19	DQ_{14}	43	V_{SS}	67	DQ_{23}	91	DQ_{36}	115	$\overline{RAS}$	139	DQ_{48}	163	CK_3
20	DQ_{15}	44	NC	68	V_{SS}	92	DQ_{37}	116	V_{SS}	140	DQ_{49}	164	NC
21	CB_0	45	$\overline{S}_2$	69	DQ_{24}	93	DQ_{38}	117	A_1	141	DQ_{50}	165	SA_0
22	CB_1	46	$DQMB_2$	70	DQ_{25}	94	DQ_{39}	118	A_3	142	DQ_{51}	166	SA_1
23	V_{SS}	47	$DQMB_3$	71	DQ_{26}	95	DQ_{40}	119	A_5	143	V_{DD}	167	SA_2
24	NC	48	NC	72	DQ_{27}	96	V_{SS}	120	A_7	144	DQ_{52}	168	V_{DD}

(Asterisk (*) indicates that the pin is not used in this module.)

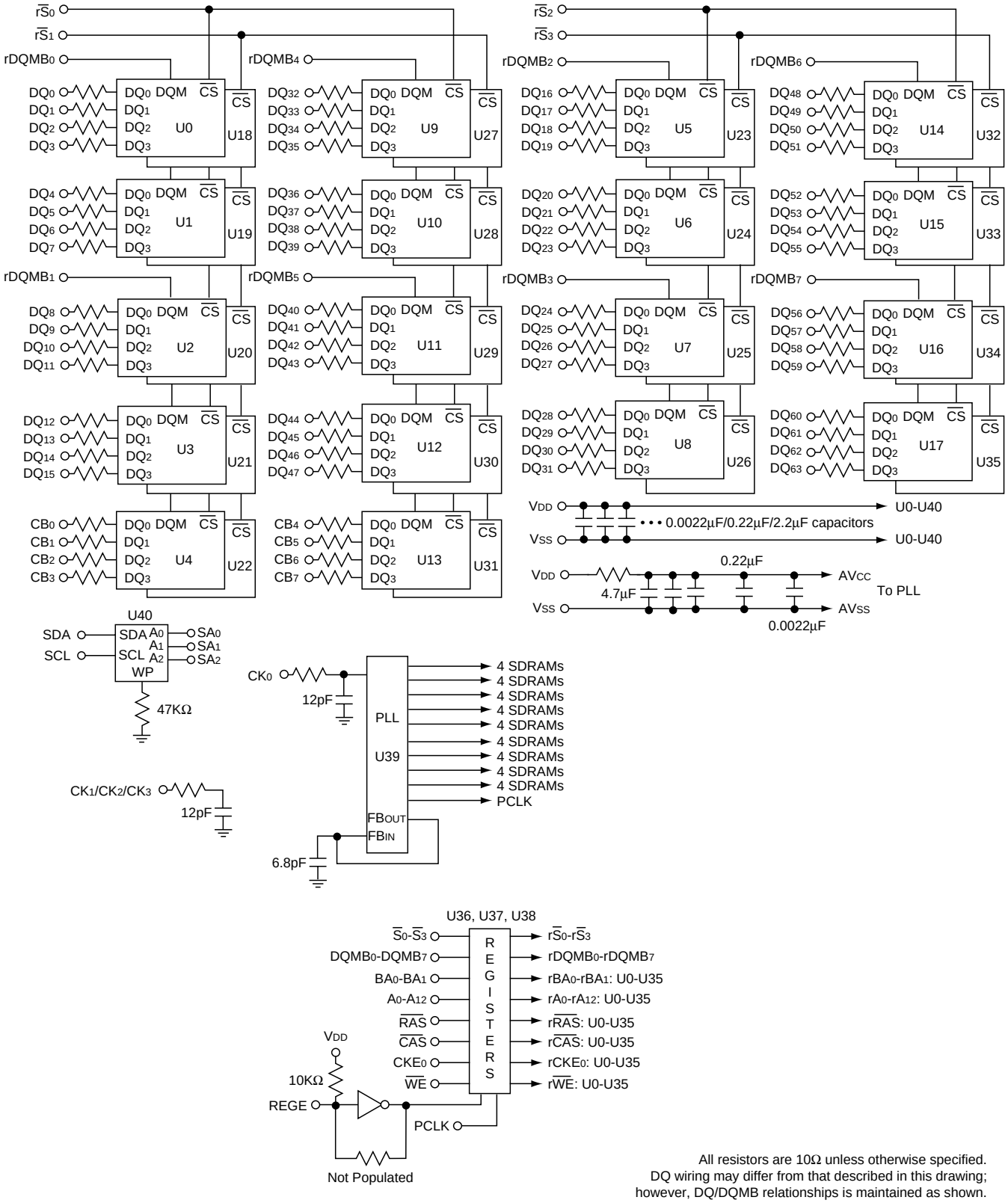
Pin Functions

Pin Symbol	Pin Function
A_0-A_9, A_{12}	Address Inputs
A_{10}/AP	Address/Autoprecharge
BA_0, BA_1	SDRAM Bank Address
DQ_0-DQ_{63}	Data Inputs/Outputs
CB_0-CB_7	Check Bits Inputs/Outputs
$\overline{WE}$	Write Enable
CK_0-CK_3	Clock Inputs
CKE_0, CKE_1	Clock Enables
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$DQMB_0$-$DQMB_7$	Data Mask
$\overline{S}_0$-$\overline{S}_3$	Chip Selects
REGE	Register Enable
SDA	SPD Data Input/Output
SCL	SPD Clock Input
SA_0-SA_2	SPD Address Input
V_{DD}	Power (+3.3V)
V_{SS}	Ground
NC	No Connection

Pin Locations



FUNCTIONAL BLOCK DIAGRAM



All resistors are 10Ω unless otherwise specified.
DQ wiring may differ from that described in this drawing;
however, DQ/DQMB relationships is maintained as shown.

SERIAL PRESENCE DETECTS

Serial PD Interface Protocol: I^2C; Current sink capability of SDA driver ≤3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported	Hex Value
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)	08h
2	Fundamental memory type	SDRAM	04h
3	# of row addresses on this assembly	13	0Dh
4	# of column addresses on this assembly	11	0Bh
5	# of module banks on this assembly	2 banks	02h
6	Data width of this assembly	72 bits	48h
7	…Data width of this assembly (continued)	—	00h
8	Voltage interface standard of this assembly	LVTTL	01h
9	SDRAM cycle time at CL=3 (t_{CYC})	7.5ns	75h
10	SDRAM access time from clock at CL=3 (t_{AC})	5.4ns	54h
11	DIMM configuration type	ECC	02h
12	Refresh rate/type	7.8µs, Self-refresh	82h
13	SDRAM width	4 bits	04h
14	Error Checking DRAM data width	4 bits	04h
15	Min. CLK delay for back-to-back rand. col. addr.	t_{CCD}=1 CLK	01h
16	SDRAM device attributes: burst lengths supported	1,2,4,8	0Fh
17	SDRAM device attributes: # of banks on SDRAM device	4 banks	04h
18	SDRAM device attributes: CAS latency	CAS latency = 2,3	06h
19	SDRAM device attributes: CS latency	CS latency = 0	01h
20	SDRAM device attributes: Write latency	Write Latency = 0	01h
21	SDRAM module attributes	Registered/Buffered/PLL	1Fh
22	SDRAM device attributes: general	V_{CC}10%, B/R, S/W, P/A, A/P	0Eh
23	Minimum clock cycle time at CL=2 (t_{CYC})	10ns	A0h
24	Max. data access time form clock at CL=2 (t_{AC})	6ns	60h
25	Minimum clock cycle time at CL=1 (t_{CYC})	N/A	00h
26	Max. data access time from clock at CL=1 (t_{AC})	N/A	00h
27	Minimum row precharge time (t_{RP})	20ns	14h
28	Minimum row active to row active delay (t_{RRD})	15ns	0Fh
29	Minimum RAS to CAS (t_{RCD})	20ns	14h
30	Minimum RAS pulse width (t_{RAS})	45.0ns	2Dh
31	Module bank density	512MB	80h
32	Min. command and address signal setup time (t_{AS})	1.5ns	15h
33	Min. command and address signal hold time (t_{AH})	0.8ns	08h
34	Min. data signal input setup time (t_{DS})	1.5ns	15h
35	Min. data signal input hold time (t_{DH})	0.8ns	08h
36-61	Superset information (may be used in future)	—	00h
62	SPD revision	2	02h
63	Checksum for bytes 0-62	JEDEC calc	xxh
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code	7Fh
65	Man. JEDEC ID code (continued)	SimpleTech's ID	A8h
66-71	—	—	00h
72	Manufacturing location	SimpleTech USA (1)	01h

continued on the next page

SERIAL PRESENCE DETECTS *(continued)*

Byte #	Function Described	Function Supported	Hex Value
73	Manufacturer's part number	S	53h
74		L	4Ch
75		7	37h
76		2	32h
77		R	52h
78		4	34h
79		L	4Ch
80		1	31h
81		2	32h
82		8	38h
83		M	4Dh
84		8	38h
85		H	48h
86		-	2Dh
87		A	41h
88		7	37h
89		5	35h
90		V	56h
91	PCB Revision code	Eng(00), RevA(01), RevB(02)	01h
92	—	—	00h
93	Manufacturing date	Year(BCD format)	yyh
94	—	Calender Week(BCD format)	wwh
95	Assembly serial number	Tester Number	ssh
96	—	serial#(bits7-0)	ssh
97	—	serial#(bits15-8)	ssh
98	—	serial#(bits23-16)	ssh
99-125	Manufacturer's specific data		xxh
126	Intel specification frequency	100MHz	64h
127	Intel specification details	CLK0; junc temp.TBD; CL2,CL3; concurrent AP	8Fh
128+	—		00h