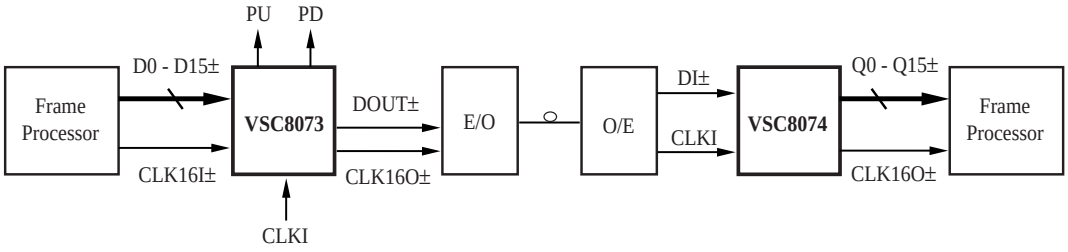
Datasheet
VSC8073

10Gb/s 16-Bit Multiplexer for STS-192 and STM-64 Applications

Features

- Performs 16:1 MUX Between 16 622Mb/s Low-Speed Signals and 10Gbs/High-Speed Signals
- Fully Differential Low-Speed Interface
- Industry Standard –2.0V and –5.2V Power Supplies
- 50Ω Output Drive Capability
- Internal Input Terminations
- Integrated Phase-Frequency Detector
- Industry-Standard 80-Pin PQFP Package

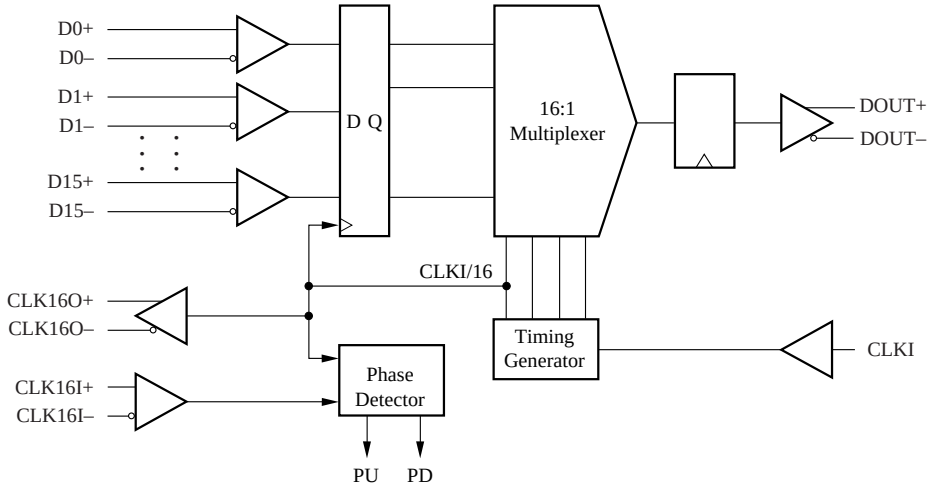
Typical System Block Diagram



General Description

The VSC8073 accepts 16 differential ECL 622Mb/s parallel inputs (**D0-D15±**). Using the 10GHz clock input (**CLKI**), the low-speed parallel inputs are multiplexed into a differential 10Gb/s high-speed output (**DOUT±**). In addition to the data inputs, a differential 622MHz clock output (**CLK16O±**) is provided. The device operates using –5.2V and –2.0V power supplies and is packaged in a thermally-enhanced, standard plastic package.

Functional Block Diagram



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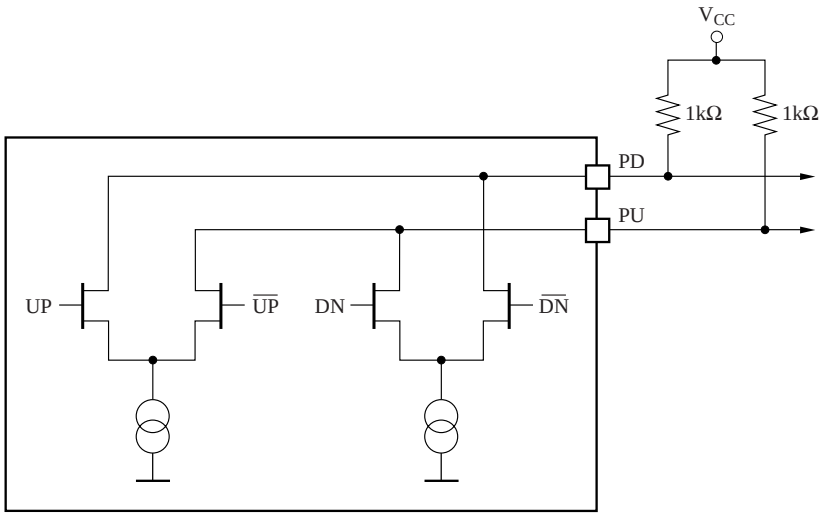
VSC8073 Functional Description

The VSC8073 integrates a 16:1 multiplexer with synchronous timing control with a phase detector. The phase and frequency detector resolves phase timing differences between the frame processor and the bit rate clock, allowing for use with an external Phase Lock-Loop (PLL). The potential difference between PU and PD is proportional to the phase difference between **CLK16I** and internal **CLK/16**. The phase detector gain is 140mv/rad with an external 1kΩ resistance (see Figure 1).

Figure 1: Phase Detector Outputs



Low-Speed Interface

The ECL-compatible parallel data inputs (**D0-D15±**) and parallel data rate clock (**CLK16I±**) are provided with on-chip 50Ω terminations to V_{TT}. ECL-compatible divided differential clocks (**CLK16O±**) are provided and should be externally terminated with 50Ω resistors to V_{TT}. The low speed interfaces, **Q0-Q15±** and **CLK16O±**, are realized using ECL levels as defined in Table 2. The recommended load configuration for the outputs is 50Ω, shown in Figure 2.

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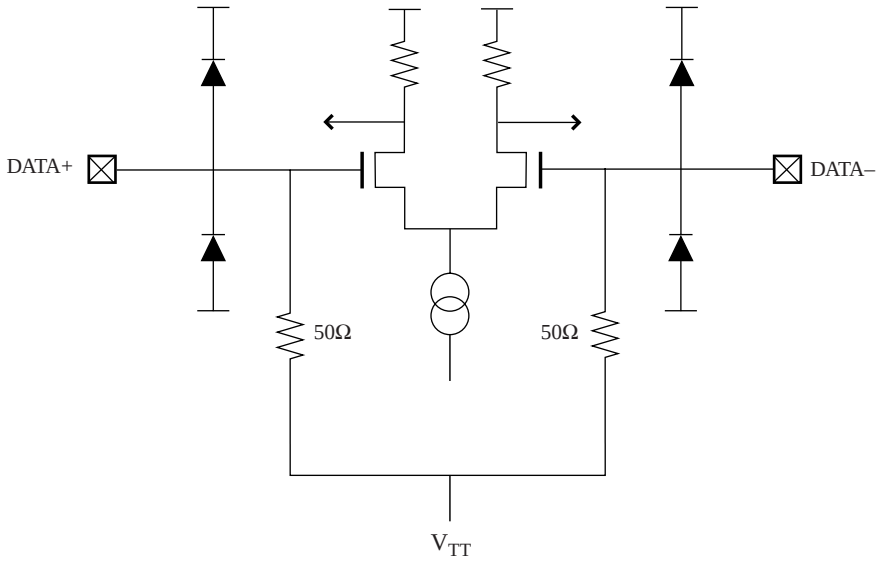
Figure 2: Low-Speed ECL Input Receiver



High-Speed Interface

The high-speed data output drivers are internally terminated through 100Ω resistors to V_{CC}. The bit rate clock (**CLKI**) input is internally terminated with a 50Ω termination to V_{CC}. The serial data outputs (**DOUT±**) are back-terminated with on-chip 100Ω resistors. The internal output driver and termination schemes for the data outputs and clock input are shown in Figures 3 and 4, respectively. The high-speed differential data out (**DOUT±**) requirements appear in Table 3. The high-speed clock input (**CLKI**) requirements appear in Table 4.

Figure 3: High-Speed Data Output Driver

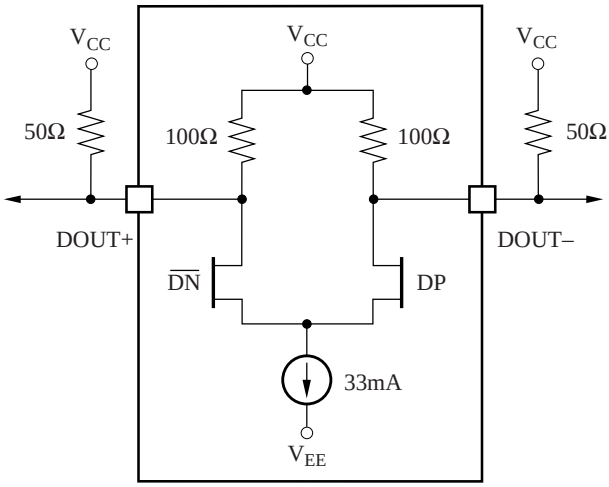


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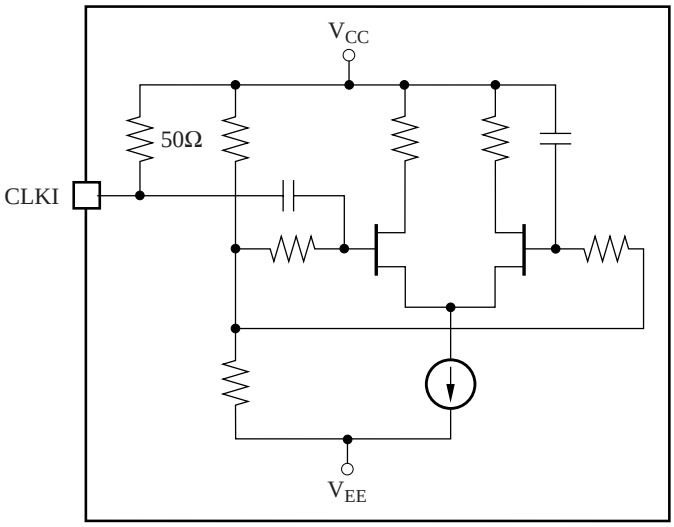
Figure 4: High-Speed Clock Input Receiver



Power Supplies

The device is typically operated from a –5.2V supply (V_{EE}) and –2.0V supply (V_{TT}). V_{CC} is typically held at ground potential. Decoupling of the power supplies is a critical element in maintaining proper operation of the part. It is recommended that V_{CC} be decoupled using a 0.1µF and a 0.01µF capacitor placed in parallel on each V_{CC} pin as close to the package as possible. If room permits, a 0.001µF capacitor should also be placed in parallel with the 0.1µF and 0.01µF capacitors previously mentioned. Recommended capacitors are low-inductance, ceramic SMT X7R devices. A 0603 package should be used for the 0.1µF capacitor; the 0.01µF and 0.001µF capacitors can be either 0603 or 0403 packages.

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AC Characteristics *(Over Recommended Operating Conditions)*

Table 1: AC Timing Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
$t_{CLK16OR}$, $t_{CLK16OF}$	CLK16O Rise and Fall Times	—	250	350	ps	See Figure 7, 20 % to 80%
$t_{CLK16IR}$, $t_{CLK16IF}$	CLK16I Rise and Fall Times	—	300	350	ps	—
t_{CLKI}	High-Speed Input Clock Period	—	100.46	—	ps	See Figure 6
t_{CLK16I}	CLK16I Period	—	1.607	—	ns	See Figure 5
t_{CLKQ}	CLKI to DOUT Delay	—	200	—	ps	See Figure 6
t_{PE}	CLK16I to CLK16O Delay	—	50	—	ps	Differential CLK16I, PU = PD (zero on-chip error)
DC_{HSCLK}	Duty Cycle of High-Speed Clock In	40	—	60	%	—
DC_{LSCLK}	Duty Cycle of Low-Speed Clock In	40	—	60	%	—
t_{DOR}, t_{DOF}	Serial Data Rise and Fall Times	—	35	40	ps	See Figure 7, 20% to 80%
$t_{D0\text{-}D15R}$, $t_{D0\text{-}D15F}$	Data Input Rise and Fall Times	—	300	350	ps	—
t_{DS}	Data Setup to CLK16O	—	—	300	ps	See Figure 5
t_{DH}	Data Hold from CLK16O	300	—	—	ps	See Figure 5
V_{TM}	Threshold Margin	500	600	—	mV	See Figure 6
t_{PM}	Phase Margin	230	260	—	degrees	At $(2^{31}-1)$ PRBS. See Figure 6.
K_{PD}	Phase Detector Gain	—	140	—	mV/rad	1 radian ~ 16ps

Figure 5: VSC8073 AC Timing Waveforms

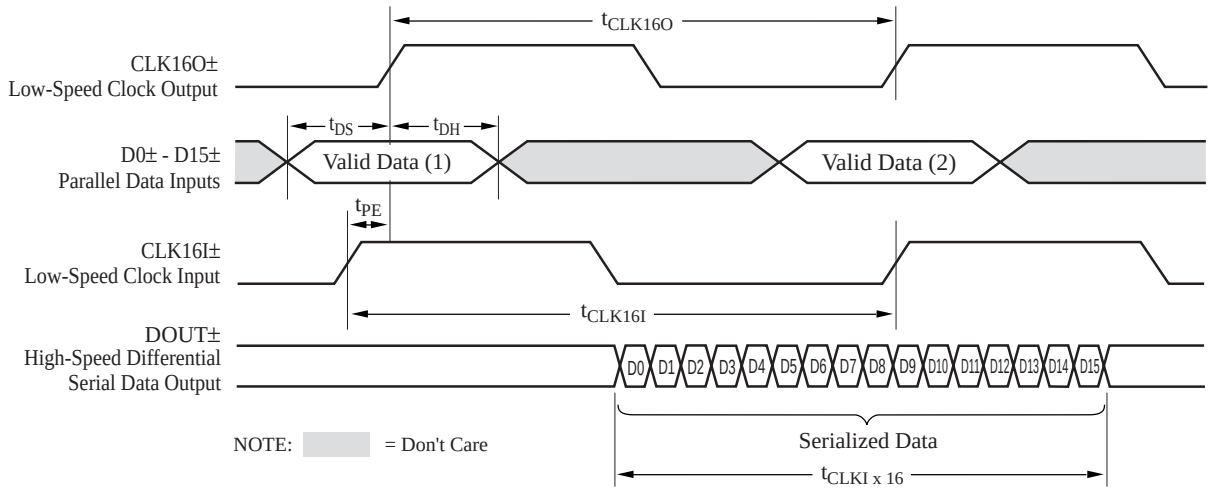

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Figure 6: VSC8073 Output Data Eye

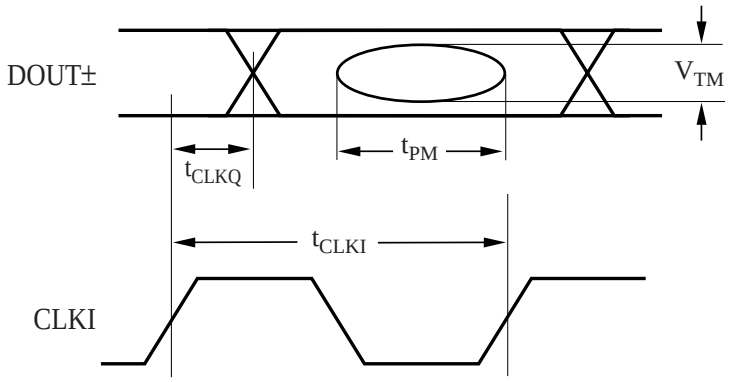
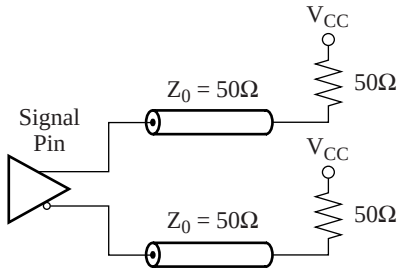
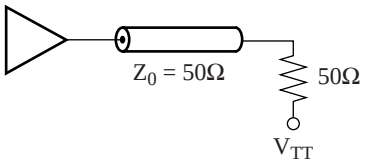


Figure 7: Parametric Measurement Information

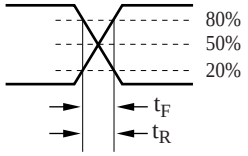
Parametric Test Load Circuit



Serial Output Load



ECL Output Load



Output Rise and Fall Times

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DC Characteristics *(Over Recommended Operating Conditions)*

Table 2: ECL Inputs/Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	–1100	—	–700	mV	50Ω to V_{TT} Load
V_{OL}	Output LOW Voltage	V_{TT}	—	–1620	mV	50Ω to V_{TT} Load
V_{IH}	Input HIGH Voltage	–1165	—	–700	mV	—
V_{IL}	Input LOW Voltage	V_{TT}	—	–1475	mV	—
I_{IH}	Input HIGH Current	—	—	32	mA	V_{IN} = –700mV, V_{TT} = –2.1V
I_{IL}	Input LOW Current	—	—	9	mA	V_{IN} = –1750mV, V_{TT} = –2.1V

Table 3: High-Speed Data Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	–200	—	–100	mV	External to 50Ω to V_{CC}
V_{OL}	Output LOW Voltage	–1100	–900	–750	mV	External to 50Ω to V_{CC}
I_{OH}	Output HIGH Current	—	3	7	mA	—
I_{OL}	Output LOW Current	—	30	37	mA	—
Z_0	Output Impedance	80	100	120	Ω	DC

Table 4: High-Speed Clock Inputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IN}	Input Swing, Single-Ended	—	500	—	mV	Peak-to-Peak
R_{INDC}	DC Value of CLKI	–1.8	—	+1.8	V	—
R_{TERM}	Termination Resistor	40	50	60	Ω	—

Table 5: Power Dissipation

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{EE}	Supply Current	—	700	TBD	mA	Outputs Open
I_{TT}	Termination Current	—	—	860	mA	All Differential Inputs Terminated. R_T = 40Ω
P_D	Power Dissipation	—	4.5	—	W	—

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Absolute Maximum Ratings(1)

ECL Power Supply Voltage, ($\mathbf{V}_{EE}$) ..... –7.0V to +0.7V
Termination Voltage, ECL Input (V_{TT}) ..... –2.5V to +0.5V
DC Input Voltage (low-speed inputs, D0-D15±) ..... V_{TT} – 2.5V to +0.5V
Input Voltage, CLKI(2) ..... –2.8V to +2.8V
Case Temperature Under Bias ..... –55° to + 125°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions

Power Supply Voltage ($\mathbf{V}_{EE}$) ..... –5.2V ±5%
Termination Supply Voltage ($\mathbf{V}_{TT}$)(3) ..... –2.0V ±5%
Operating Case Temperature Range ($\boldsymbol{T}$)(4) ..... 0° to 85°C

Notes: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

(2) Static voltage on CLKI must be within –1.8V to +1.8V.

(3) CAUTION: Do not apply V_{TT} prior to V_{EE}.

(4) Lower limit is ambient temperature and upper limit is case temperature.

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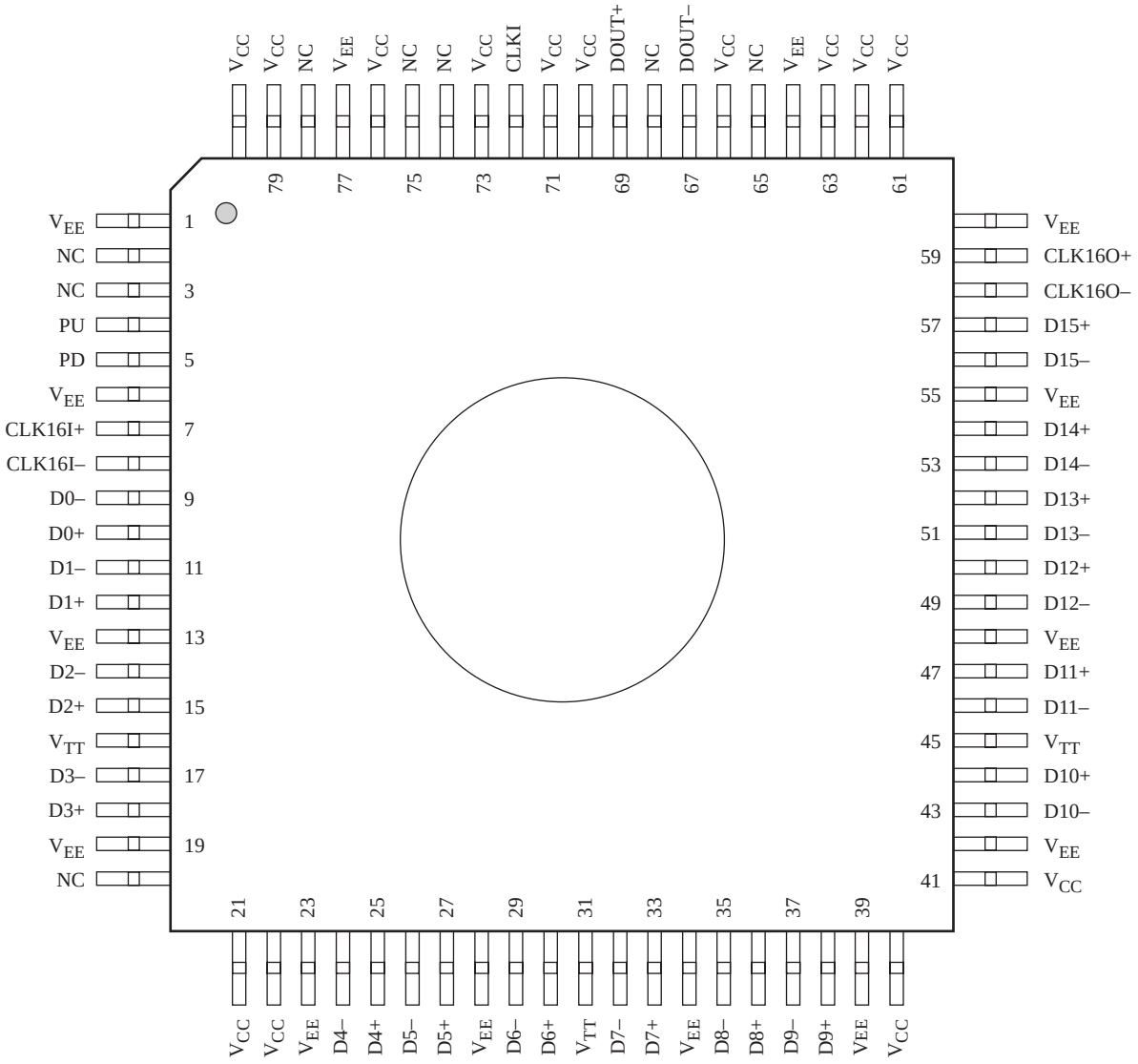
Package Pin Descriptions

Figure 8: Pin Diagram



Top View

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Table 6: Pin Identification

Pin	*I/O*	*Pin Description*
9-12, 14, 15, 17, 18 24-27, 29, 30, 32, 33, 35-38, 43, 44, 46, 47, 49-54, 56, 57	D0-D15±	INPUT—DIFFERENTIAL ECL: Parallel data presented to this port is clocked into the device. The timing of this data is relative to the CLK16O output.
72	CLKI	INPUT—HIGH-SPEED CLOCK: Bit rate input clock. This clock is terminated with 50Ω resistors to V_{CC}, and is AC-coupled on chip.
7, 8	CLK16I±	INPUT—DIFFERENTIAL ECL: Parallel data rate clock.
67, 69	DOUT±	OUTPUT—DIFFERENTIAL HIGH SPEED: Serial data output stream. DOUT+ and DOUT– should be terminated with 50Ω resistors to ground at the load.
58, 59	CLK16O±	OUTPUT—DIFFERENTIAL ECL: Bit rate clock divided by 16.
4, 5	PU, PD	OUTPUT—ANALOG: Phase detector outputs.
21, 22, 40, 41, 61-63, 66, 70, 71, 73, 76, 79, 80	V_{CC}	GROUND
1, 6, 13, 19, 23, 28, 34, 39, 42, 48, 55, 60, 64, 77	V_{EE}	POWER SUPPLY: –5.2 nominal.
16, 31, 45	V_{TT}	POWER SUPPLY: –2.0V nominal.
2, 3, 20, 65, 68, 74, 75, 78	NC	Do not connect, leave open.

Table 7: Pin Descriptions

Pin Number	*Pin Name*	*I/O*	*Level*	*Description*
1	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
2	NC	NA	NA	Do not connect, leave open.
3	NC	NA	NA	Do not connect, leave open.
4	PU	O	—	Phase detector analog output
5	PD	O	—	Phase detector analog output
6	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
7	CLK16I+	I	ECl	Differential divide by 16 clock input
8	CLK16I–	I	ECL	Differential divide by 16 clock input
9	D0–	I	ECL	Low-speed differential parallel data
10	D0+	I	ECL	Low-speed differential parallel data
11	D1–	I	ECL	Low-speed differential parallel data

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Table 7: Pin Descriptions

Pin Number	*Pin Name*	*I/O*	*Level*	*Description*
12	D1+	I	ECL	Low-speed differential parallel data
13	V_{EE}	I	–5.2V	Power at –5.2V nominal
14	D2–	I	ECL	Low-speed differential parallel data
15	D2+	I	ECL	Low-speed differential parallel data
16	V_{TT}	I	–2.0V	Power at –2.0V nominal
17	D3–	I	ECL	Low-speed differential parallel data
18	D3+	I	ECL	Low-speed differential parallel data
19	V_{EE}	I	–5.2V	Power at –5.2V nominal
20	NC	NA	NA	Do not connect, leave open
21	V_{CC}	I	GND	Ground
22	V_{CC}	I	GND	Ground
23	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
24	D4–	I	ECL	Low-speed differential parallel data
25	D4+	I	ECL	Low-speed differential parallel data
26	D5–	I	ECL	Low-speed differential parallel data
27	D5+	I	ECL	Low-speed differential parallel data
28	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
29	D6–	I	ECL	Low-speed differential parallel data
30	D6+	I	ECL	Low-speed differential parallel data
31	V_{TT}	I	–2.0V nom	Power supply at –2.0V nominal
32	D7–	I	ECL	Low-speed differential parallel data
33	D7+	I	ECL	Low-speed differential parallel data
34	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
35	D8–	I	ECL	Low-speed differential parallel data
36	D8+	I	ECL	Low-speed differential parallel data
37	D9–	I	ECL	Low-speed differential parallel data
38	D9+	I	ECL	Low-speed differential parallel data
39	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
40	V_{CC}	I	GND	Ground
41	V_{CC}	I	GND	Ground
42	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
43	D10–	I	ECL	Low-speed differential parallel data
44	D10+	I	ECL	Low-speed differential parallel data
45	V_{TT}	I	–2.0V nom	Power supply at –2.0V nominal
46	D11–	I	ECL	Low-speed differential parallel data
47	D11+	I	ECL	Low-speed differential parallel data

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Table 7: Pin Descriptions

Pin Number	*Pin Name*	*I/O*	*Level*	*Description*
48	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
49	D12–	I	ECL	Low-speed differential parallel data
50	D12+	I	ECL	Low-speed differential parallel data
51	D13–	I	ECL	Low-speed differential parallel data
52	D13+	I	ECL	Low-speed differential parallel data
53	D14–	I	ECL	Low-speed differential parallel data
54	D14+	I	ECL	Low-speed differential parallel data
55	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
56	D15–	I	ECL	Low-speed differential parallel data
57	D15+	I	ECl	Low-speed differential parallel data
58	CLK16O–	O	ECL	Differential divide by 16 clock output
59	CLK16O+	O	ECL	Differential divide by 16 clock output
60	VEE	I	–5.2V nom	Power supply at –5.2V nominal
61	V_{CC}	I	GND	Ground
62	V_{CC}	I	GND	Ground
63	V_{CC}	I	GND	Ground
64	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
65	NC	NA	NA	Do not connect, leave open
66	V_{CC}	I	GND	Ground
67	DOUT–	O	HS	High-speed differential data out
68	NC	NA	NA	Do not connect, leave open
69	DOUT+	O	HS	High-speed differential data out
70	V_{CC}	I	GND	Ground
71	V_{CC}	I	GND	Ground
72	CLKI	I	HS	High-speed clock input
73	V_{CC}	I	GND	Ground
74	NC	NA	NA	Do not connect, leave open
75	NC	NA	NA	Do not connect, leave open
76	V_{CC}	I	GND	Ground
77	V_{EE}	I	–5.2V nom	Power supply at –5.2V nominal
78	NC	NA	NA	Do not connect, leave open
79	V_{CC}	I	GND	Ground
80	V_{CC}	I	GND	Ground

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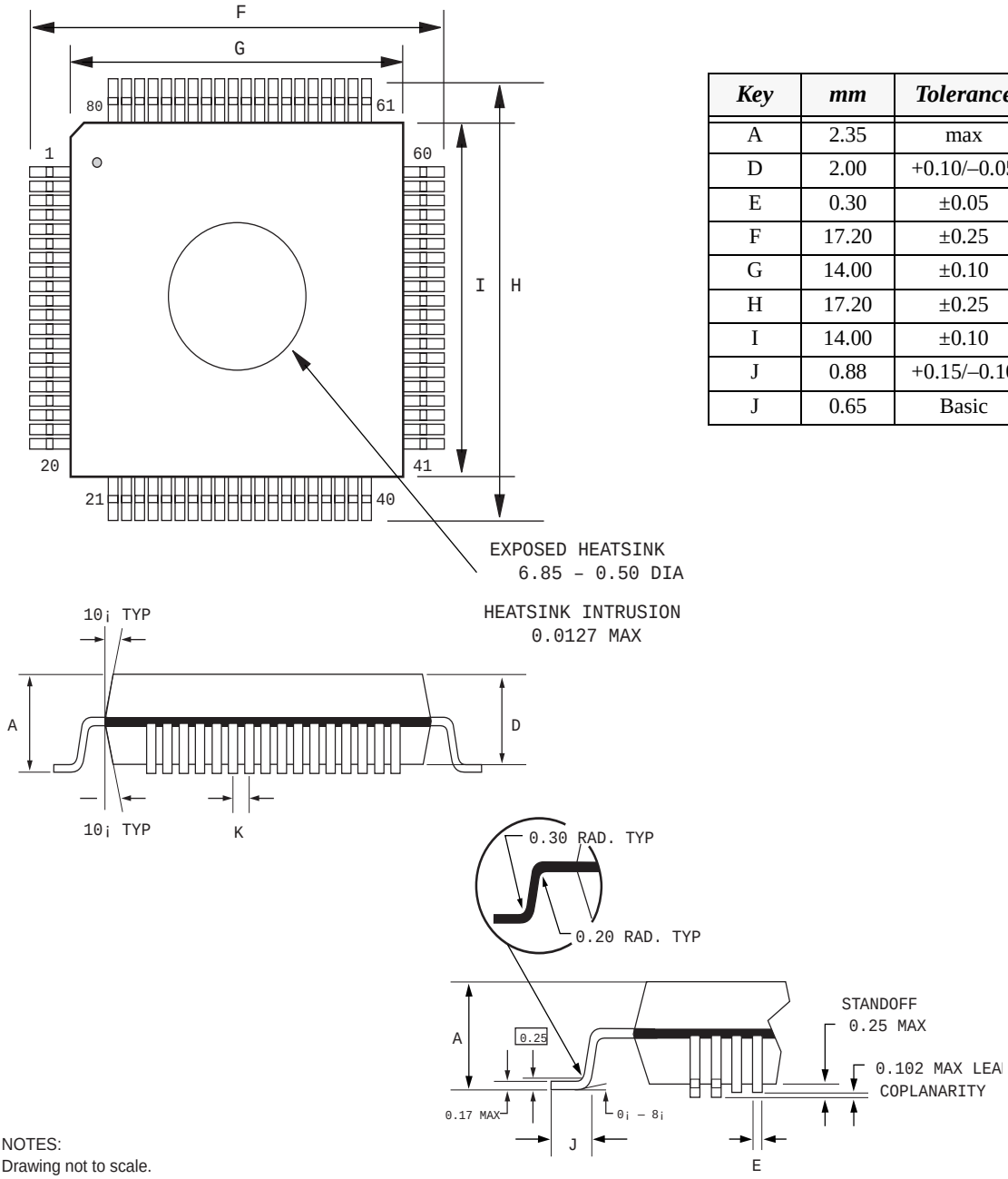
Package Information

80-Pin PQFP Package Drawing



Key	*mm*	*Tolerance*
A	2.35	max
D	2.00	+0.10/–0.05
E	0.30	±0.05
F	17.20	±0.25
G	14.00	±0.10
H	17.20	±0.25
I	14.00	±0.10
J	0.88	+0.15/–0.10
J	0.65	Basic

NOTES:
Drawing not to scale.
All units in mm unless othewise noted.

Package Thermal Conditions

This package has been enhanced with a copper heat slug to provide a low thermal resistance path from the die to the exposed surface of the heat spreader. Refer to Table 8 for thermal resistance.

Table 8: Thermal Resistance

Symbol	*Description*	*°C/W*
θ_{JC}	Thermal resistance from junction-to-case.	2.2
θ_{CA}	Thermal resistance from case-to-ambient with no airflow, including conduction through the leads.	25.8
θ_{JA}	Thermal resistance from junction-to-ambient	28

Thermal Resistance with Airflow

Table 9 shows the thermal resistance with airflow. This thermal resistance value reflects all the thermal paths including through the leads in an environment where the leads are exposed. The temperature difference between the ambient airflow temperature and the case temperature should be the worst-case power of the device multiplied by the thermal resistance.

Table 9: Thermal Resistance with Airflow

Airflow (lfpm)	θ_{CA} *(°C/W)*
100	24
200	21
400	19
600	17

Maximum Ambient Temperature Without Heatsink

The worst-case ambient temperature without the use of a heatsink is given by:

$$T_{A(MAX)} = T_{C(MAX)} - P_{(MAX)}\,\theta_{CA}$$

where,

θ_{CA} = Theta case-to-ambient at appropriate airflow

$T_{A\ (MAX)}$ = Ambient air temperature

$T_{C(MAX)}$ = Case temperature (85°C)

$P_{(MAX)}$ = Power (4.5W)

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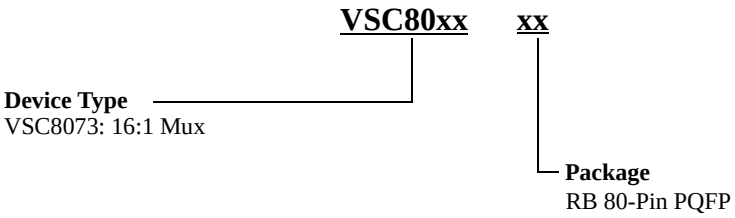
Ordering Information

The order number for this product is formed by a combination of the device number, and package type.



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Warning

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