Sound processor IC

BH3875AKS2

The BH3875AKS2 is a sound control IC for mini-component stereo. 6-ch input selector, vocal fade, volume, surround, 5-band graphic equalizer, dynamic bass, and 5-band spectrum analyzer are integrated into a single chip. Soft switch can reduce the switching noise occurred when volume, vocal fade, surround, and dynamic bass are switched.

●Applications

Mini component stereo, Micro component stereo, CD radio cassette players, and TV.

●Features

1) A single chip IC integrates all functions of volume, tone control, and spectrum analyzer.
2) Soft switching can reduce the noise occured when volume, mode selector, surround, dynamic bass, and gain of graphic equalizer are switched.
3) 6-ch input selector, mode selector, volume, surround, graphic equalizer, dynamic bass, and spectrum analyzer.
4) Built-in matrix surround, pseudo stereo circuit, and band pass filter for spectrum analyzer.
5) Low distortion and low noise due to the BiCMOS process adopting resistance ladder volume.
6) Filters of dynamic bass and biamp can be set freely by the combination of LPF and HPF.

●Absolute maximum ratings (Ta=25°C)

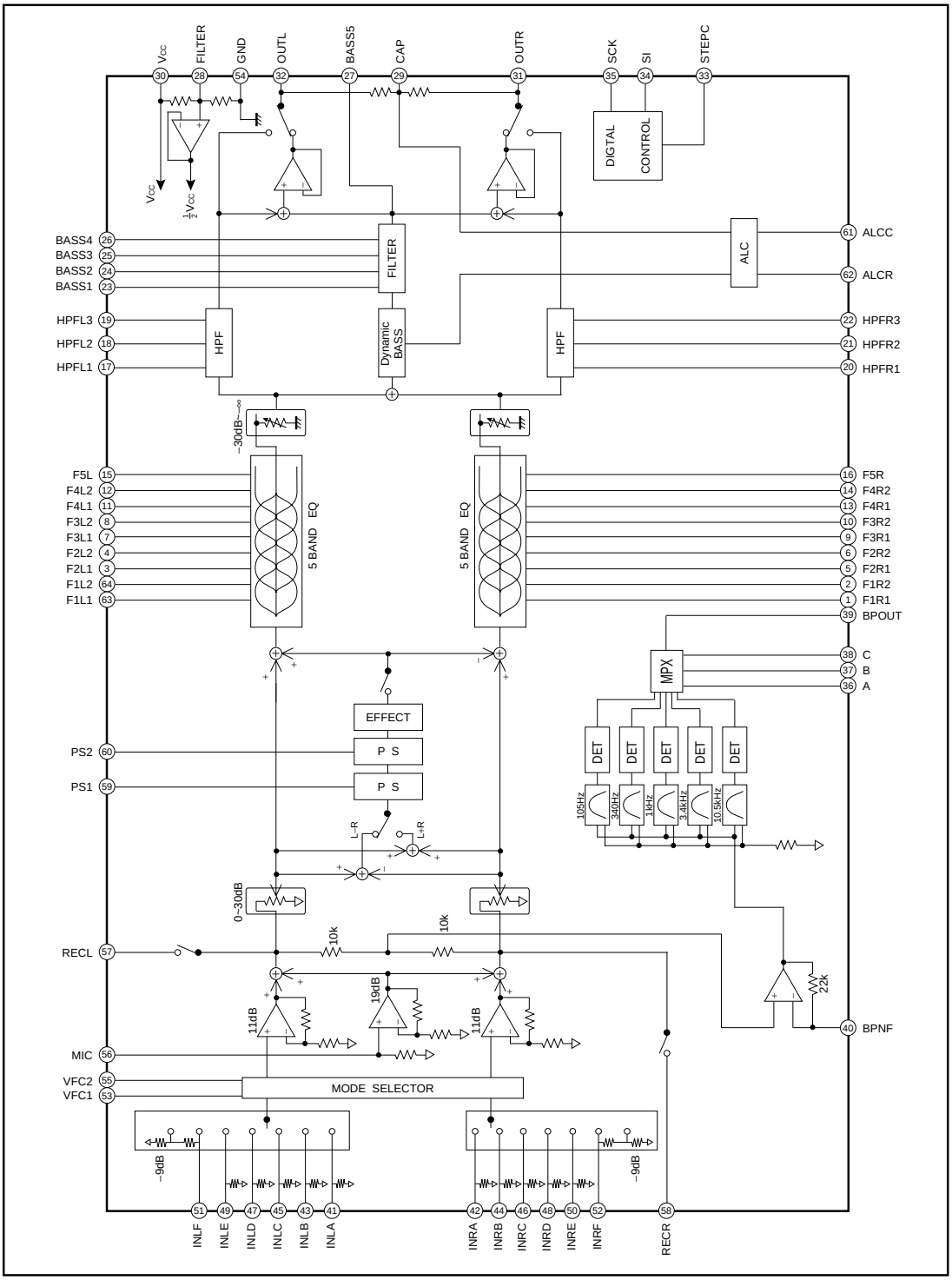
Parameter	Symbol	Limits	Unit
Applied Voltage	V_{CC}	10.0	V
Power Dissipation	Pd	1200*	mW
Operating Temperature	Topr	−20~+70	°C
Storage Temperature	Tstg	−55~+125	°C

*Derating : 12mW/°C for operation above Ta=25°C.
(Mounted on a 70.0mm×70.0mm×1.6mm glass epoxy PCB.)

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply Voltage	V_{CC}	8	9	9.5	V

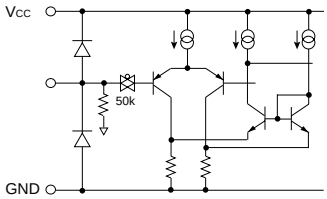
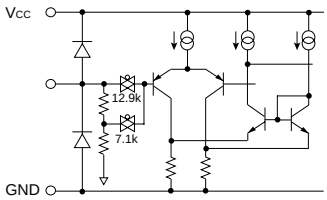
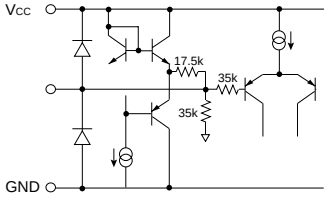
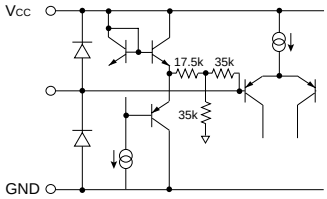
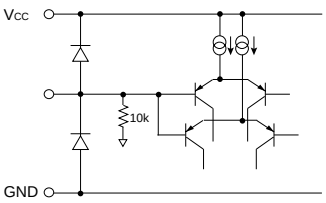
●**Block diagram**

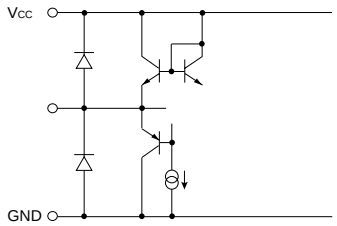
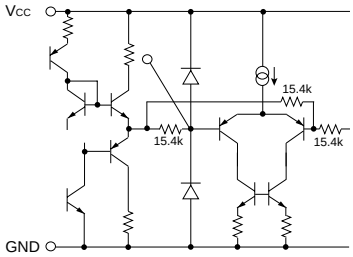
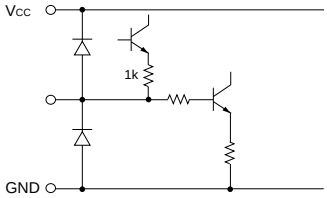
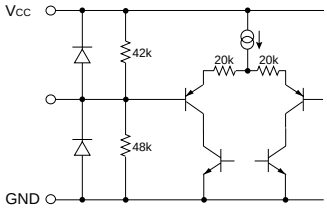
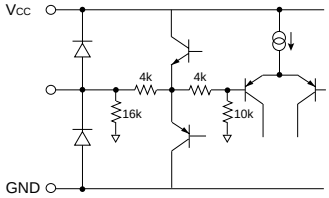
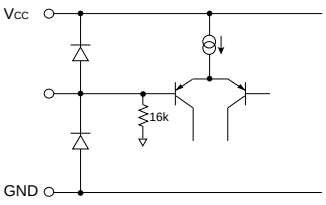


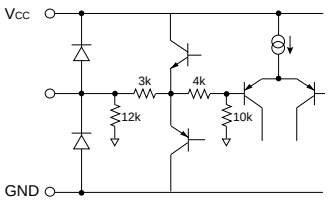
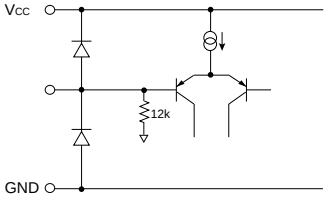
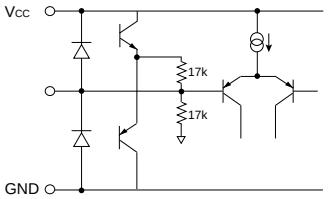
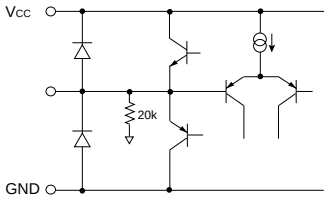
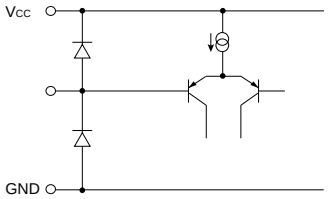
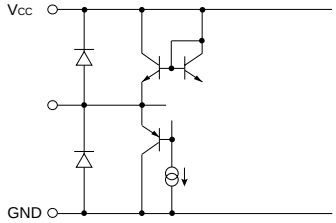
●**Pin descriptions**

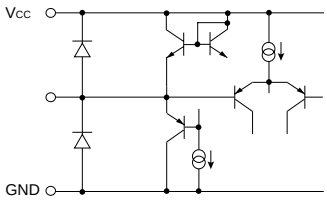
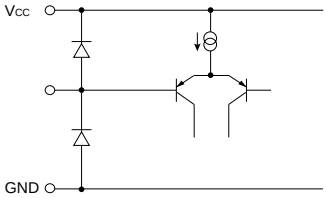
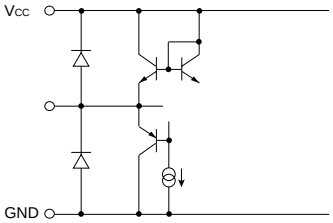
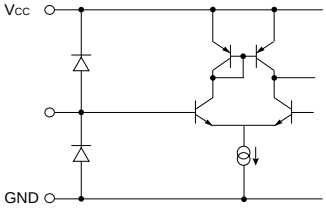
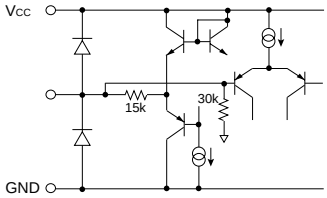
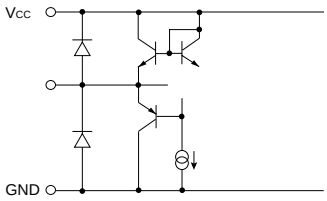
Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	F1R1	Rch GREQ f1 Filter Setting Pin	33	STEPC	Time constant attachment for switching shock protection
2	F1R2	Rch GREQ f1 Filter Setting Pin	34	SI	Serial Data Latch Receiving Pin
3	F2L1	Lch GREQ f2 Filter Setting Pin	35	SCK	Serial Clock Receiving Pin
4	F2L2	Lch GREQ f2 Filter Setting Pin	36	A	Parallel Data Receiving Pin
5	F2R1	Rch GREQ f2 Filter Setting Pin	37	B	Parallel Data Receiving Pin
6	F2R2	Rch GREQ f2 Filter Setting Pin	38	C	Parallel Data Receiving Pin
7	F3L1	Lch GREQ f3 Filter Setting Pin	39	BPOUT	Output Pin For Spectrum analyzer
8	F3L2	Lch GREQ f3 Filter Setting Pin	40	BPNF	Spectrum analyzer Level Setting PIN
9	F3R1	Rch GREQ f3 Filter Setting Pin	41	INLA	Lch Input Pin A
10	F3R2	Rch GREQ f3 Filter Setting Pin	42	INRA	Rch Input Pin A
11	F4L1	Lch GREQ f4 Filter Setting Pin	43	INLB	Lch Input Pin B
12	F4L2	Lch GREQ f4 Filter Setting Pin	44	INRB	Rch Input Pin B
13	F4R1	Rch GREQ f4 Filter Setting Pin	45	INLC	Lch Input Pin C
14	F4R2	Rch GREQ f4 Filter Setting Pin	46	INRC	Rch Input Pin C
15	F5L	Lch GREQ f5 Filter Setting Pin	47	INLD	Lch Input Pin D
16	F5R	Rch GREQ f5 Filter Setting Pin	48	INRD	Rch Input Pin D
17	HPFL1	Lch High-pass Filter Setting Pin	49	INLE	Lch Input Pin E
18	HPFL2	Lch High-pass Filter Setting Pin	50	INRE	Rch Input Pin E
19	HPFL3	Lch High-pass Filter Setting Pin	51	INLE	Lch Input Pin F
20	HPFR1	Rch High-pass Filter Setting Pin	52	INRF	Rch Input Pin F
21	HPFR2	Rch High-pass Filter Setting Pin	53	VFC1	Vocal Fade Filter Setting Pin
22	HPFR3	Rch High-pass Filter Setting Pin	54	GND	Ground Pin
23	BASS1	Dynamic Bass Filter Setting Pin	55	VFC2	Vocal Fade Filter Setting Pin
24	BASS2	Dynamic Bass Filter Setting Pin	56	MIC	Input Pin For Microphone
25	BASS3	Dynamic Bass Filter Setting Pin	57	RECL	Lch RECOUT Output Pin
26	BASS4	Dynamic Bass Filter Setting Pin	58	RECR	Rch RECOUT Output Pin
27	BASS5	Biamp Output Pin	59	PS1	Surround Setting Pin
28	FILTER	$V_{CC}/2$ Pin	60	PS2	Surround Setting Pin
29	CAP	ALC trap frequency setting pin	61	ALCC	Time Constant of ALC Setting Pin
30	V_{CC}	Power Supply Pin	62	ALCR	ALC Level Setting Pin
31	OUTR	Rch Output Pin	63	F1L1	Lch GREQ f1 Filter Setting Pin
32	OUTL	Lch Output Pin	64	F1L2	Lch GREQ f1 Filter Setting Pin

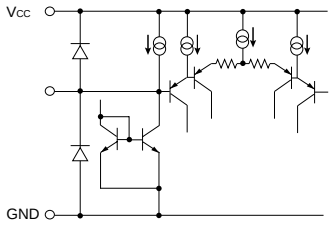
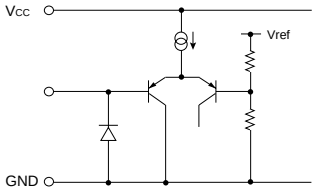
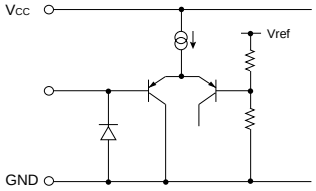
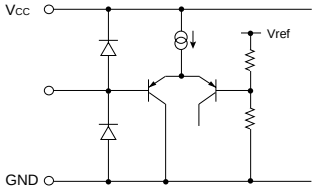
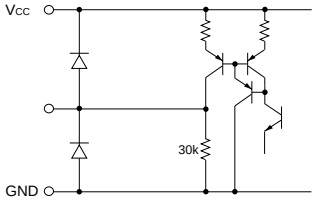
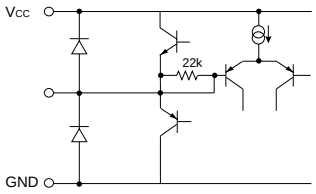
●Input / output circuits

Pin No.	Pin name	Pin voltage	Equivalent circuit	Pin description
41 42 43 44 45 46 47 48 49 50	INLA INRA INLB INRB INLC INRC INLD INRD INLE INRE	Vcc/2		A pin for inputting a sound signal. It is suitable for input of CD, MD, tuner and tape. The input impedance is 50kΩ (upon typical setting).
51 52	INLF INRF	Vcc/2		A pin for inputting a sound signal. The input impedance is 20kΩ (upon typical setting). It is possible to set 0dB or –9dB.
53	VFC1	Vcc/2		A pin for setting Vocal Fade frequency characteristic.
54	GND	–	–	A Ground Pin.
55	VFC2	Vcc/2		A pin for setting Vocal Fade frequency characteristic.
56	MIC	Vcc/2		A pin for inputting a mic signal. The input impedance is 10kΩ (upon typical setting).

Pin No.	Pin name	Pin voltage	Equivalent circuit	Pin description
57 58	RECL RECR	Vcc/2		A pin for outputting a sound signal for recording.
59 60	PS1 PS2	Vcc/2		A pin for setting surrond phase shifter.
61	ALCC	0		A pin for setting attack time and release time of ALC.
62	ALCR	–		A pin for setting threshold to set the ALC.
63 1 7 9	F1L1 F1R1 F3L1 F3R1	Vcc/2		A pin for setting graphic equalizer frequency characteristic.
64 2 8 10	F1L2 F1R2 F3L2 F3R2	Vcc/2		A pin for setting graphic equalizer frequency characteristic.

Pin No.	Pin name	Pin voltage	Equivalent circuit	Pin description
3 5 11 13	F2L1 F2R1 F4L1 F4R1	Vcc/2		A pin for setting graphic equalizer frequency characteristic.
4 6 12 14	F2L2 F2R2 F4L2 F4R2	Vcc/2		A pin for setting graphic equalizer frequency characteristic.
15 16	F5L F5R	Vcc/2		A pin for setting graphic equalizer frequency characteristic.
17 20	HPFL1 HPFR1	Vcc/2		A pin for setting cut-off frequency of HPF.
18 21	HPFL2 HPFR2	Vcc/2		A pin for setting cut-off frequency of HPF.
19 22	HPFL3 HPFR3	Vcc/2		A pin for setting cut-off frequency of HPF.

Pin No.	Pin name	Pin voltage	Equivalent circuit	Pin description
23 25	BASS1 BASS3	Vcc/2		A pin for setting Dynamic Bass (Biamp) frequency characteristic.
24 26	BASS2 BASS4	Vcc/2		A pin for setting Dynamic Bass (Biamp) frequency characteristic.
27	BASS5	Vcc/2		A pin for outputting Biamp.
28	FILTER	Vcc/2		A pin for inputting Vcc/2 from outside of IC.
29	CAP	Vcc/2		A pin for specifying trap frequency of ALC
30	VCC	–	–	Power Supply Pin.
31 32	OUTR OUTL	Vcc/2		A pin for outputting a sound signal.

Pin No.	Pin name	Pin voltage	Equivalent circuit	Pin description
33	STEPC	–		Time constant attachment for switching shock protection.
34	SI	–		A pin for inputting a serial data.
35	SCK	–		A pin for inputting a serial clock.
36 37 38	A B C	–		A pin for inputting a parallel data.
39	BPOUT	–		A pin for outputting a spectrum analyzer B.P.F.
40	BPNF	Vcc/2		A pin for adjusting gain of non-inverting amplifier in sperctrum analyzer.

●Electrical characteristics

(Unless specified particulary noted, Ta=25°C, V_{CC}=9V, f=1kHz, Rg=600Ω, R_L=10kΩ, V_{IN}=300mVrms, INPUT SELECTOR=Ach, MODE SELECTOR=Through, VOLUME=0dB, SURROUND=0dB, GRAPHIC EQUALIZER=0dB, DYNAMIC BASS=0dB, SPECTRUM ANALYZER=RESET)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Input pin	Measurement pin	Data setting (1)	(2)	(3)	(4)	(4)	(5)	(5)	(6)	(7)	(8)	Switch control table SW 1/4	SW 2/5	SW 3/6	SW 7	SW 8
Circuit current	IQ	–	40	60	mA	No signal, after power on.	–	30	–	–	–	–	–	–	–	–	–	–	1	1	1	2	1
Maximum input voltage	VIM	0.4	0.7	–	Vrms	THD=1%	41 42	32 31	00	05	03	04	0C	02	0A	06	81	07	1	1	1	2	1
Maximum output voltage	VOM	2.0	2.5	–	Vrms	THD=1%	41 42	32 31	00	05	03	04	0C	02	0A	06	81	07	1	1	1	2	1
Voltage gain	GV	9	11	13	dB		41 42	32 31	00	05	03	04	0C	02	0A	06	81	07	1	1	1	2	1
Total harmonic distortion rate	VOM	–	0.01	0.05	%	V_O=1Vrms, 400Hz–30kHz BPF	41 42	32 31	00	05	03	04	0C	02	0A	06	81	07	1	1	1	2	1
Output noise voltage *	VNO	–	35	50	μVrms	Biamp=0dB, DIN AUDIO	41 42	32 31	00	15	03	04	0C	02	0A	06	89	07	1	2	–	2	1
Residual output noise voltage *	VMNO	–	5	20	μVrms	Rg=0Ω, Volume=–∞, Biamp=0dB, DIN AUDIO	41 42	32 31	00	15	03	04	0C	02	0A	06	89	07	1	2	–	2	1
Cross talk *	CT	70	80	–	dB	Biamp=0dB, Rg=0Ω, DIN AUDIO	41 42	31 32	00	05	03	04	0C	02	0A	06	81	07	1/1	1/2	1/–	2	1
Channel balance	CB	–1.5	0	1.5	dB	Lch reference	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Selector A-E Input impedance	RIN	35	50	65	kΩ		41,42 43,44 45,46 47,48 49,50	41,42 43,44 45,46 47,48 49,50	–	–	–	–	–	–	–	–	–	–	1 2 3 4 5	1	2	2	1
Selector F Input impedance	RINF	10	20	30	kΩ		51 52	51 52	–	–	–	–	–	–	–	–	–	–	6 6	1	2	2	1
Maximum attenuation *	ATTMAX	86	95	–	dB	DIN AUDIO	41 42	32 31	F8	05	03	04	0C	02	0A	06	81	07	1	1	1	2	1
Vocal fade suppression quantity	GVF	25	30	–	dB		41,42 41,42	32 31	00	25	03	04	0C	02	0A	06	81	07	1	1	1	2	1
Graphic equalizer boost gain set error (Set 2dB,4dB,6dB)	VGQBL	–2	0	2	dB	V_{IN}=100mVrms f_{IN}=100Hz, 300Hz, 1kHz, 3kHz, or 10kHz	41 42	32 31	00	05	03	74 04 04 04 04	0C 7C 0C 0C 0C	02 02 72 02 02	0A 0A 0A 7A 0A	06 06 06 06 76	81	07	1	1	1	2	1
Graphic equalizer boost gain set error (Set 8dB,10dB,12dB)	VGQBH	–3	0	3	dB	V_{IN}=100mVrms f_{IN}=100Hz, 300Hz, 1kHz, 3kHz, or 10kHz																	
Graphic equalizer cut gain set error (Set –2dB,–4dB,–6dB)	VGQCL	–2	0	2	dB	V_{IN}=100mVrms f_{IN}=100Hz, 300Hz, 1kHz, 3kHz, or 10kHz	41 42	32 31	00	05	03	E4 04 04 04 04	0C EC 0C 0C 0C	02 02 E2 02 02	0A 0A 0A EA 0A	06 06 06 06 E6	81	07	1	1	1	2	1
Graphic equalizer cut gain set error (Set–8dB,–10dB,–12dB)	VGQCL	–3	0	3	dB	V_{IN}=100mVrms f_{IN}=100Hz, 300Hz, 1kHz, 3kHz, or 10kHz																	
Graphic equalizer channel balance	GQCB	–1.5	0	1.5	dB	Lch reference	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Dynamic bass boost gain	VBB	15	18	21	dB	V_{IN}=40mVrms, f_{IN}=75Hz 23pin=GND	41,42 41,42	32 31	00	E5	03	04	0C	02	0A	06	81	07	1	1	1	2	2
Dynamic bass boost channel balance	VBCB	–1.5	0	1.5	dB	Lch reference	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Input separation *	CTIN	80	90	–	dB	DIN AUDIO	41 42	57 58	00	05	03	04	0C	02	0A	06	41 C1 21 A1 61	07	1	1	1	2	1
Input mute attenuation *	VINMU	80	90	–	dB	DIN AUDIO	41 42	32 31	00	05	03	04	0C	02	0A	06	01	07	1	1	1	2	1
Microphone voltage gain	GMIC	17	19	21	dB	V_{IN}=100mVrms	56	32 31	00	05	03	04	0C	02	0A	06	81	07	1	2	–	1	1
Microphone mute attenuation *	VMICMU	80	90	–	dB	V_{IN}=100mVrms DIN AUDIO	56	32 31	00	15	03	04	0C	02	0A	06	81	07	1	2	–	1	1
RECOUT voltage gain	GREC	9	11	13	dB		41 42	57 58	00	05	03	04	0C	02	0A	06	81	07	1	1	1	2	1
RECOUT mute attenuation *	VRECMU	80	90	–	dB	DIN AUDIO	41 42	57 58	00	0D	03	04	0C	02	0A	06	81	07	1	1	1	2	1
Selector F attenuation	F2ATT	–7	–9	–11	dB		49 50	32 31	00	05	03	04	0C	02	0A	06	E1	07	6	1	1	2	1
Surround maximum voltage gain	VSUMAX	7	9	11	dB	V_{IN}=100mVrms f_{IN}=10kHz	41 42	32 31	00	05	1B	04	0C	02	0A	06	81	07	1	1	1	2	1

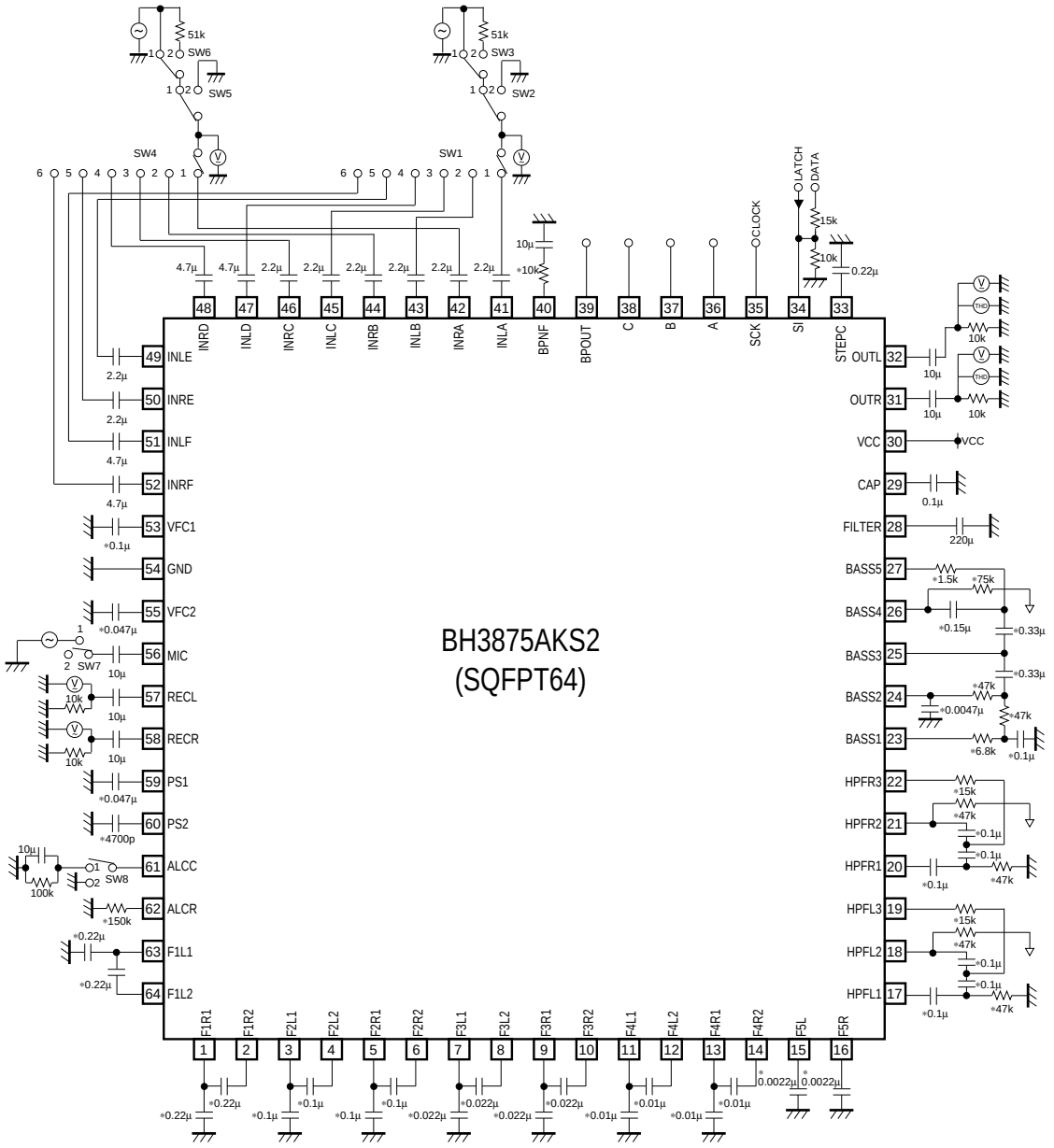
© Design against radiation-proof is not made.
* VP-9690A (Average value detection, effective value display) DIN AUDIO filter by Matsushita Communication is used for * measurement.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Input pin	Measure-ment pin	Data setting										Switch control table				
									(1)	(2)	(3)	(4)	(4)	(5)	(5)	(6)	(7)	(8)	SW 1/4	SW 2/5	SW 3/6	SW 7	SW 8
Simulated stereo maximum voltage gain Lch	VMONL	6.5	8.5	10.5	dB	V_{IN}=100mVrms f_{IN}=680Hz	41,42 41,42	32 31	00	05	1B	04	0C	02	0A	06	91	07	1	1	1	2	1
Simulated stereo maximum voltage gain Rch	VMONR	11.3	13.3	15.3	dB	V_{IN}=100mVrms f_{IN}=680Hz																	
Spectrum analyzer maximum output level	VMAX	4.0	4.8	–	V	V_{IN}=–23dBV	41,42 41,42	39	00	05	03	04	0C	02	0A	06	81	47 C7 27 A7 67	1	1	1	2	1
Spectrum analyzer output offset voltage	VOS	0	30	230	mV	V_{IN}=0Vrms	–	39	00	05	03	04	0C	02	0A	06	81	47 C7 27 A7 67	–	–	–	–	–
Spectrum analyzer standard output level	VST	0.65	1.35	1.7	V	V_{IN}=–41dBV f_{IN}=105Hz, 340Hz, 1kHz, 3.4kHz, or 10.5kHz	41,42 41,42	39	00	05	03	04	0C	02	0A	06	81	47 C7 27 A7 67	1	1	1	2	1
Ripple rejection ∗	RR	40	–	–	dB	VRR=100mVrms f_{RR}=100Hz, DIN AUDIO	30	32 31	00	05	03	04	0C	02	0A	06	81	07	1	2	–	2	1

© Design against radiation-proof is not made.

∗ VP-9690A (Average value detection, effective value display) DIN AUDIO filter by Matsushita communication is used for ∗ measurement.

●**Measurement circuit**



Recommendable External Parts

1. Element marked with ∗
   - · Carbon-film resistor : ±1%
   - · Film capacitor : ±1%
   - · Ceramic capacitor : ±1%
2. Unless specified particularly, use the following external parts
   - · Carbon-film resistor : ±5%
   - · Film capacitor : ±20%
   - · Electrolytic capacitor : ±20%

Notes on wiring

1. GND shall be wired solidly.
2. Wiring pattern of SI and SCK shall be away from that of analog unit and cross talk shall not be acceptable.
3. Lines of SI and SCK shall not be parallel if possible. The lines shall be shielded, if they are adjacent to each other.

●Circuit operations

Timing of Control Signal

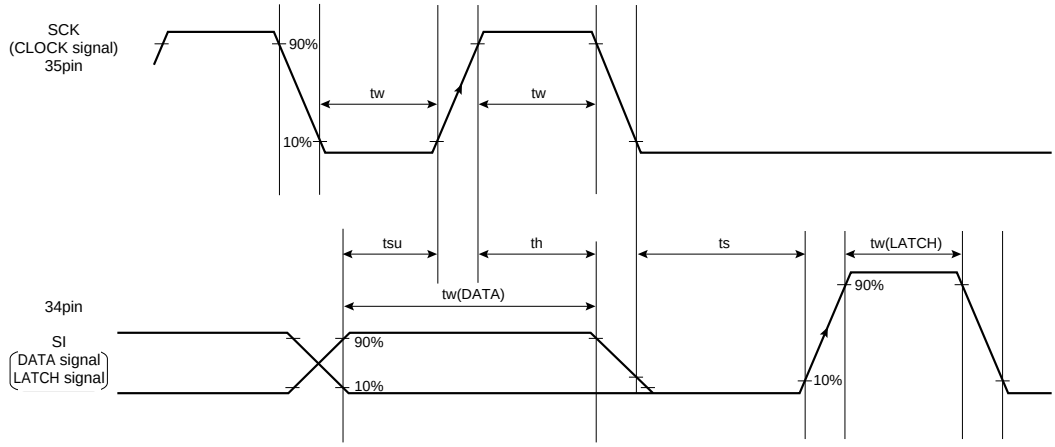


Fig.2

DATA (SI) is read at a rising edge of CLOCK.
DATA is fixed by the rising edge of LATCH.
Be sure to set SCK and SI to Low after latching.
When the CLOCK signal is High, it doesn't accept LATCH signal.

Constant of Timing Chart (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
"High" Input voltage	V_{IH}	3.3	5.0	6.0	V
"Middle" Input voltage	V_{IM}	1.8	2.0	2.4	V
"Low" Input voltage	V_{IL}	–0.3	0	1.2	V
Clock width	tw	2.0	–	–	µs
Data width	tw (DATA)	4.0	–	–	µs
Latch width	tw (LATCH)	2.0	–	–	µs
Setup time (DATA→CLOCK)	tsu	1.0	–	–	µs
Hold time (CLOCK→DATA)	th	1.0	–	–	µs
Setup time (DATA, CLOCK→LATCH)	ts	1.0	–	–	µs

·Serial signal SI is judging DATA and LATCH in the difference of the voltage level.
·In the application schematic, it is changing 0-5V 3line serial data into the 2line serial data at the voltage with the resistance and the diode of the external. We request enough examination, because there is a case where the voltage which is changed by the ability for the microcomputer to drive and the external parts.

When transmitting more than one piece of data at once, we request the following serial control transmission.

(1) Timing of serial data and latch

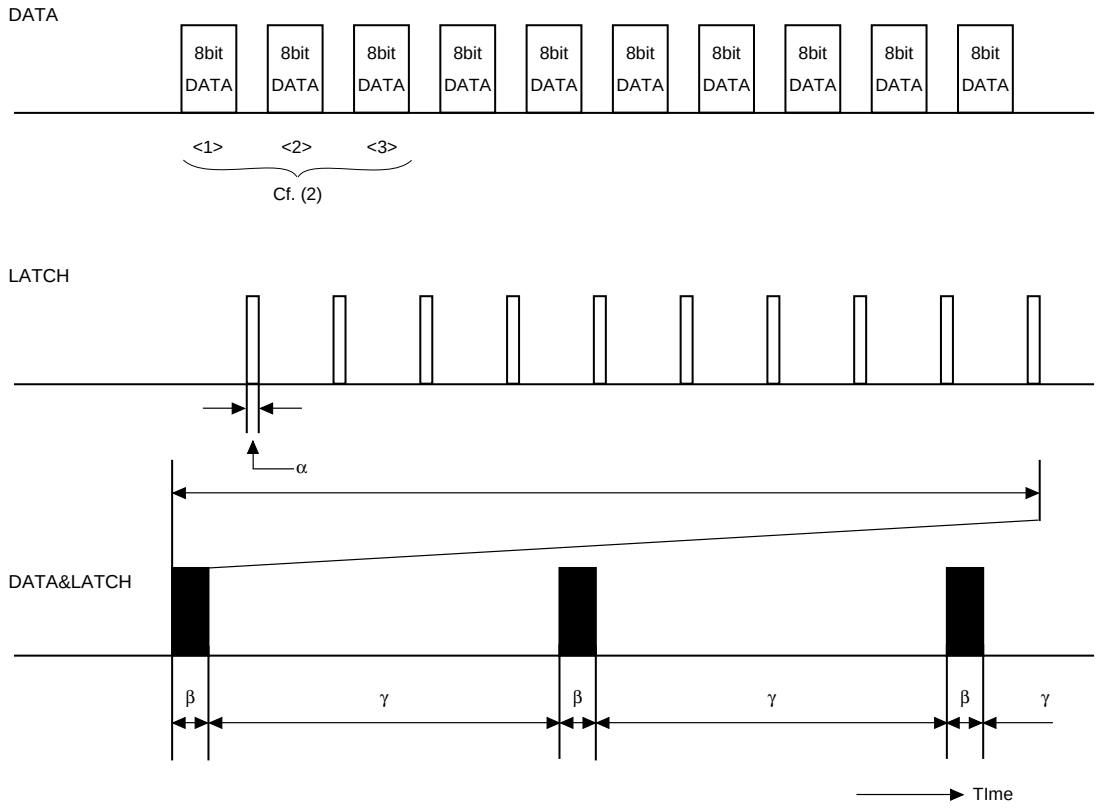


Fig.3

	Parameter	Time
α	LATCH pulse width	More than 2.0μs
β	The time wich transmits more than one piece of data at once.	Less than 2.5ms
γ	The time which sends more than one piece of the following data after sending more than one piece of data (When the capacitor of 33pin is 0.22μF.)	More than 100ms

(2) About the order which transmits more than one piece of DATA at once

When transmitting more than one piece of DATA including <1>, <2> or <3> at once, transmit DATA of <1>, <2> or <3> of the data format first.

In case of transmitting some data from <1> until <8>, transmit only necessary DATA in order from <1>.

(3) About DATA needing the timing of (1)

DATA needing the timing of (1) are DATA <1>, <2> and <3>. Even if one data of DATA <1>, <2> and <3> is transmitted, follow the timing of (1).

In case of transmitting some data from <4> until <8>, the timing of <1> need not be followed. In the case, there are no problems if the constant of timing chart in page 12 is satisfied.

(4) Relation of the serial data and 33pin capacitor

The interval γ of the data and the data can be more shortly set by changing the capacitor of 33pins.
(Ex. When making the changing speed of VOLUME faster)

The relation between the interval γ of the data and the data and the capacitor of 33pin is as follows.

33pin Capacitor	The interval of the data and the next data
0.047μF	More than 25ms
0.1μF	More than 50ms
0.22μF	More than 100ms

NOTE : It is possible to do the interval of the and the next data shortly by changing 33pin capacitor into 0.047μF. However, the switching sound becomes rather bigger than the switching sound of setting 0.1μF about the switching sound of VOLUME, DBASS, SURROUND, MODE SELECTOR.

(5) Others

If there is common impedance in GND of the IC, the switching sound sometimes occurs by changing the mode.
Wiring pattern of SI and SCK shall be away from that of analog unit and cross talk shall not be acceptable.

SERIAL CONTROL DATA FORMAT

<1>	D00	D01	D02	D03	D04	D05	D06	D07
	● VOLUME					0	0	0
<2>	D10	D11	D12	D13	D14	D15	D16	D17
	● MODE SELECTOR			MIC	REC OUT	1	0	1
<3>	D20	D21	D22	D23	D24	D25	D26	D27
	● DYNAMIC BASS / Biamp			● SURROUND EFFECT		0	1	1
<4>	D30	D31	D32	D33	D34	D35	D36	D37
	▲ GRAPHIC EQUALIZER f1 / f2				GREQ 0 : f1 1 : f2	1	0	0
<5>	D40	D41	D42	D43	D44	D45	D46	D47
	▲ GRAPHIC EQUALIZER f3 / f4				GREQ 0 : f3 1 : f4	0	1	0
<6>	D50	D51	D52	D53	D54	D55	D56	D57
	▲ GRAPHIC EQUALIZER f5				*	1	1	0
<7>	D60	D61	D62	D63	D64	D65	D66	D67
	INPUT SELECTOR			SURROUND / STEREO	DYNAMIC BASS / Biamp	0	0	1
<8>	D70	D71	D72	D73	D74	D75	D76	D77
	SPECTRUM ANALYZER			*	*	1	1	1

* Don't Care

As for functions of the ● and ▲ mark, measures to reduce step noise are done. Because the functions of no marks have no measures of step noise, please supply mute.
As for the ● mark, it becomes a soft switch method.

<1> VOLUME ATTENUATION

ATT	D00	D01	D02	D03	D04	D05	D06	D07
0.0dB	0	0	0	0	0	0	0	0
–2.0dB	1	0	0	0	0			
–4.0dB	0	1	0	0	0			
–6.0dB	1	1	0	0	0			
–8.0dB	0	0	1	0	0			
–10.0dB	1	0	1	0	0			
–12.0dB	0	1	1	0	0			
–14.0dB	1	1	1	0	0			
–16.0dB	0	0	0	1	0			
–18.0dB	1	0	0	1	0			
–20.0dB	0	1	0	1	0			
–22.0dB	1	1	0	1	0			
–24.0dB	0	0	1	1	0			
–26.0dB	1	0	1	1	0			
–28.0dB	0	1	1	1	0			
–30.0dB	1	1	1	1	0			
–32.0dB	0	0	0	0	1			
–34.0dB	1	0	0	0	1			
–36.0dB	0	1	0	0	1			
–38.0dB	1	1	0	0	1			
–40.0dB	0	0	1	0	1			
–44.0dB	1	0	1	0	1			
–48.0dB	0	1	1	0	1			
–52.0dB	1	1	1	0	1			
–56.0dB	0	0	0	1	1			
–60.0dB	1	0	0	1	1			
–64.0dB	0	1	0	1	1			
–68.0dB	1	1	0	1	1			
–72.0dB	0	0	1	1	1			
–76.0dB	1	0	1	1	1			
–82.0dB	0	1	1	1	1			
–∞	1	1	1	1	1			

<2> MODE SELECTOR, MIC, REC OUT

MODE	D10	D11	D12	D13	D14	D15	D16	D17
THROUGH	0	0	0	MIC 0 : ON 1 : MUTE	REC OUT 0 : ON 1 : MUTE	1	0	1
THROUGH	1	0	0					
THROUGH	0	1	0					
THROUGH	1	1	0					
VOCAL FADE	0	0	1					
Lch MONAULAL	1	0	1					
Rch MONAULAL	0	1	1					
L+R	1	1	1					

NOTE : About input selector, mode selector is cleared when MUTE of the input selector is chosen.
When MUTE of the input selector is canceled, choose the mode selector, too.
The MUTE command of the input selector has priority over the command of the mode selector.

<3> Dynamic Bass / Biamp Effect, Surround Effect

(a) Dynamic Bass / Biamp Effect

The effect quantity in biamp is different from the value of the below table.

GAIN	D20	D21	D22	D23	D24	D25	D26	D27
0dB	0	0	0	Refer to the Surround Effect		0	1	1
0dB	1	0	0					
3dB	0	1	0					
6dB	1	1	0					
9dB	0	0	1					
12dB	1	0	1					
15dB	0	1	1					
18dB	1	1	1					

(b) Surround Effect

The effect quantity in simulated stereo mode is different from the value of the below table.

GAIN	D20	D21	D22	D23	D24	D25	D26	D27
0dB	Refer to the Dynamic Bass Effect			0	0	0	1	1
3dB				1	0			
6dB				0	1			
9dB				1	1			

NOTE : GAIN is the name given to the transfer data. Depending on the values of the external constant, the specified gain may not be output.

<4> Graphic Equalizer f1 / f2

GAIN	D30	D31	D32	D33	D34	D35	D36	D37
+12dB	1	1	1	1	GREQ SELECT 0 : f1 1 : f2	1	0	0
+12dB	0	1	1	1				
+10dB	1	0	1	1				
+8dB	0	0	1	1				
+6dB	1	1	0	1				
+4dB	0	1	0	1				
+2dB	1	0	0	1				
0dB	0	0	0	1				
0dB	0	0	0	0				
–2dB	1	0	0	0				
–4dB	0	1	0	0				
–6dB	1	1	0	0				
–8dB	0	0	1	0				
–10dB	1	0	1	0				
–12dB	0	1	1	0				
–12dB	1	1	1	0				

NOTE : GAIN is the name given to the transfer data. Depending on the values of the external constant, the specified gain may not be output.

<5> Graphic Equalizer f3 / f4

GAIN	D40	D41	D42	D43	D44	D45	D46	D47
+12dB	1	1	1	1	GREQ SELECT 0 : f3 1 : f4	0	1	0
+12dB	0	1	1	1				
+10dB	1	0	1	1				
+8dB	0	0	1	1				
+6dB	1	1	0	1				
+4dB	0	1	0	1				
+2dB	1	0	0	1				
0dB	0	0	0	1				
0dB	0	0	0	0				
–2dB	1	0	0	0				
–4dB	0	1	0	0				
–6dB	1	1	0	0				
–8dB	0	0	1	0				
–10dB	1	0	1	0				
–12dB	0	1	1	0				
–12dB	1	1	1	0				

NOTE : GAIN is the name given to the transfer data. Depending on the values of the external constant, the specified gain may not be output.

<6> Graphic Equalizer f5, DPL

GAIN	D50	D51	D52	D53	D54	D55	D56	D57
+12dB	1	1	1	1	*	1	1	0
+12dB	0	1	1	1				
+10dB	1	0	1	1				
+8dB	0	0	1	1				
+6dB	1	1	0	1				
+4dB	0	1	0	1				
+2dB	1	0	0	1				
0dB	0	0	0	1				
0dB	0	0	0	0				
–2dB	1	0	0	0				
–4dB	0	1	0	0				
–6dB	1	1	0	0				
–8dB	0	0	1	0				
–10dB	1	0	1	0				
–12dB	0	1	1	0				
–12dB	1	1	1	0				

* Don't Care

NOTE : GAIN is the name given to the transfer data. Depending on the values of the external constant, the specified gain may not be output.

<7> Input Selector, Dynamic Bass / Biamp, Surround / Simulated stereo

INPUT	D60	D61	D62	D63	D64	D65	D66	D67
MUTE	0	0	0	0 : Surround 1 : Simulated stereo	0 : Dynamic Bass 1 : Biamp	0	0	1
INPUT-LA, INPUT-RA	1	0	0					
INPUT-LB, INPUT-RB	0	1	0					
INPUT-LC, INPUT-RC	1	1	0					
INPUT-LD, INPUT-RD	0	0	1					
INPUT-LE, INPUT-RE	1	0	1					
INPUT-LF_1, INPUT-RF_1 (0dB)	0	1	1					
INPUT-LF_2, INPUT-RF_2 (–9dB)	1	1	1					

<8> Spectrum Analyzer

FREQUENCY	D70	D71	D72	D73	D74	D75	D76	D77
RESET	0	0	0	*	*	1	1	1
RESET	1	0	0					
fo=105Hz	0	1	0					
fo=340Hz	1	1	0					
fo=1kHz	0	0	1					
fo=3.4kHz	1	0	1					
fo=10.5kHz	0	1	1					
Priority over parallel data	1	1	1					

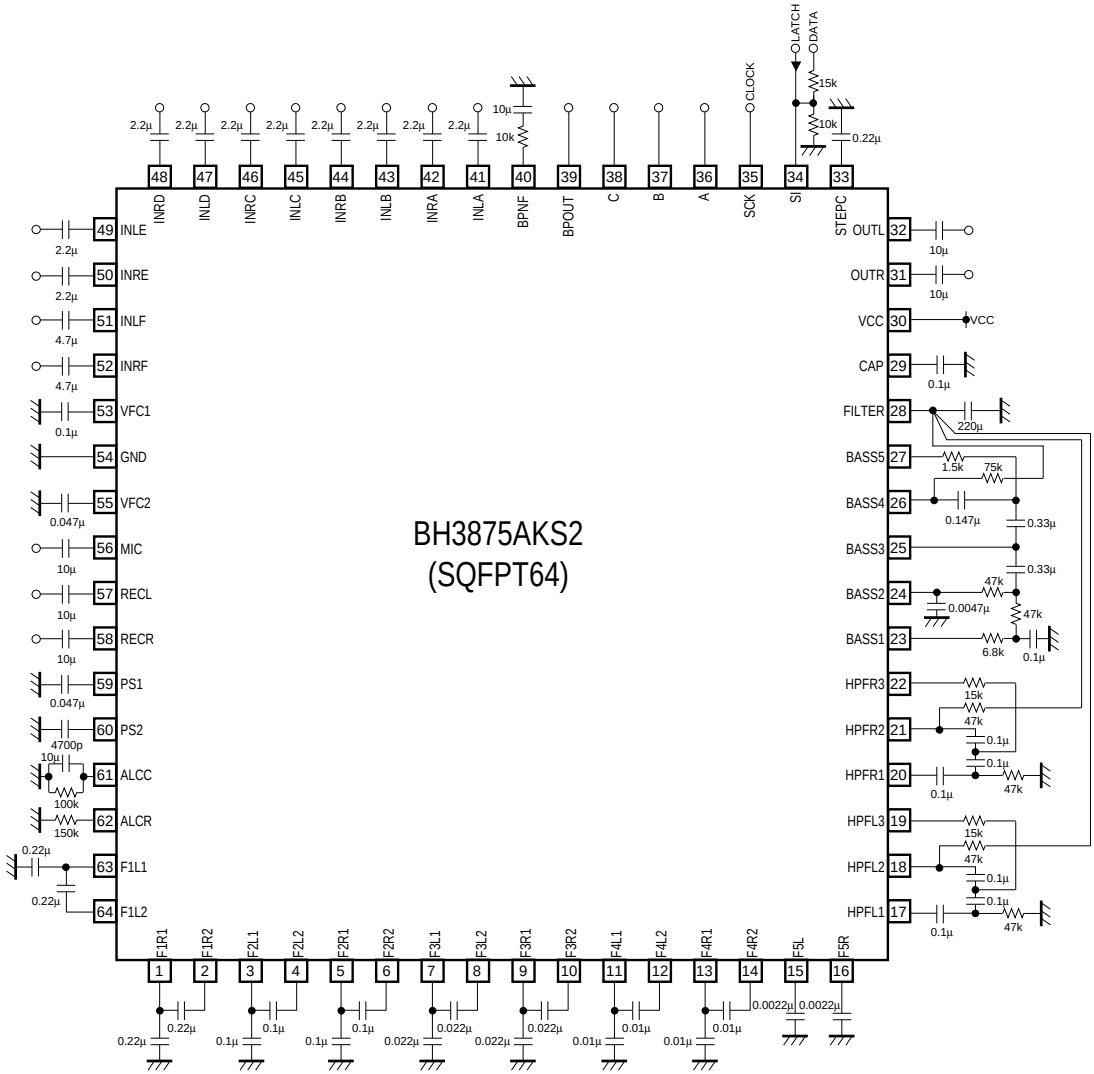
* Don't Care

PARALLEL CONTROL

A	B	C	BPOUT (39pin)
36pin	37pin	38pin	
0	0	0	RESET
0	0	1	105Hz
0	1	0	340Hz
0	1	1	RESET
1	0	0	1kHz
1	0	1	RESET
1	1	0	3.4kHz
1	1	1	10.5kHz

When serial control is done, a parallel control isn't received.
When the serial control is "parallel priority", a parallel control on the left is received.
When changing the frequency of spectrum analyzer, transmit the command of the following frequency after transmitting a reset command.

●**Application example**



●Operation notes

(1) Operation supply voltage range

Within operation supply voltage range, basic circuit function operation is guaranteed within operation ambient temp. But please confirm set up of constant and element, voltage set up and temp set up on use.

(2) Operation temp range

If it within recommended operation voltage range, circuit function operation is guaranteed within operation temp. It corralled to conditions of power dissipation to temp.

Please watch out except condition stipulated by electrical characteristics within the range. It cannot guarantee standard value of electrical characteristics. But it retains original function.

(3) Application circuit

Example of application circuit drawing is convinced as recommendable, But please confirm characteristic including above mentioned noticed.

At use with modification of external constant, please decide with enough margin considering characteristics of this IC, and external parts including quiescence characteristics and excessive characteristics.

Please note that we have not yet confirmed any concerned patent rights completely.

(4) 2-wire serial control

High-frequency digital signal is inputted into the SCK terminal and SI terminal. So wire and print patterns suitably to prevent interference to analog signal system line (especially to input line).

(5) Ground line

Please connect IC's ground to the ground of a set with one point. When the IC has common impedance to the ground line, pop noise may occur in function switching.

(6) Schmidt circuit

This IC has the Schmidt circuit as preventive measures against logic signal input into the DATA (34pin) and CLK (35pin) terminals. Therefore, this IC is not affected so much by noise to a logic signal line.

(7) Power on / off

At ON of OFF of power supply, pop noise occurs. Therefore, please supply mute.

(8) Setting of spectrum analyzer at minimum light level

Output offset voltage may shift due to the surrounding conditions (temperature, stresses, etc.).

Therefore when setting the spectrum analyzer at minimum light level, leave a margin (more than 30% to spectrum analyzer output offset voltage VOS).

●Electrical characteristic curves

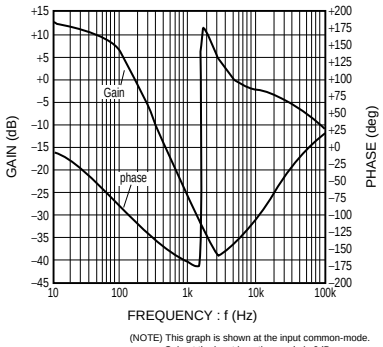


Fig.4 Vocal fade characteristics

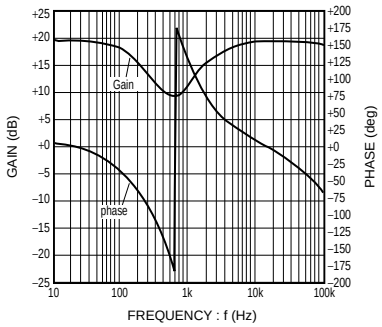


Fig.5 Surround characteristics

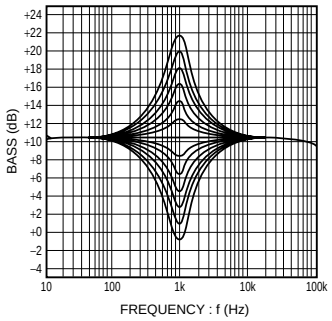


Fig.7 Graphic equalizer characteristics

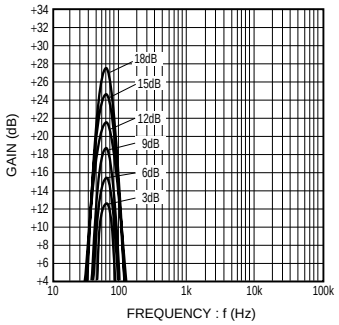


Fig.7 Biamp characteristics
(Input common-mode)

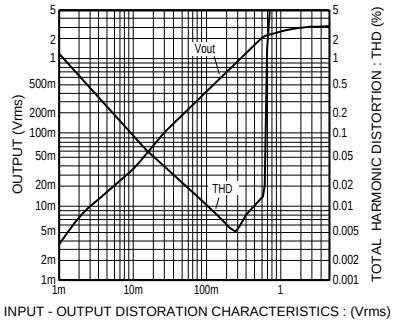
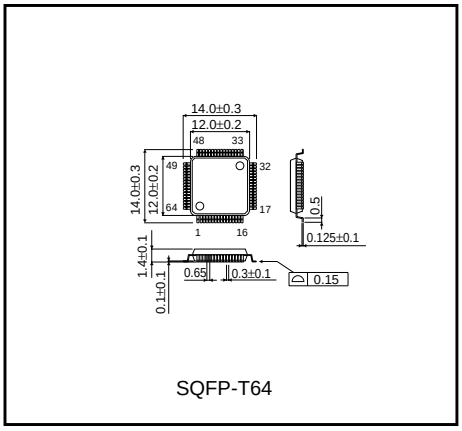


Fig.8 Input-Output distortion
characteristics

●**External dimensions** (Units : mm)



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