Triscend A7 Configurable System-on-Chip Platform

July, 2001 (Version 1.00) **Product Description**

Industry's first complete 32-bit Configurable System-on-Chip (CSoC)

- High-performance, low-power consumption, 32-bit RISC processor (ARM7TDMI™)
- 8K-byte mixed instruction/data cache
- 16K-byte internal scratchpad RAM
- Next-generation embedded programmable logic architecture (up to 40,000 gates)
- High-performance dedicated internal bus (up to 455M-bytes per second at 60 MHz)
- External memory interface supporting Flash, EEPROM, SRAM, and SDRAM
- Advanced real-time, in-system debugging capability
- Stand-alone operation from a single external memory (code + initialization)
- 2.5-volt core with 3.3- or 2.5-volt I/Os
- Four independent high-performance DMA channels

High-performance, 32-bit ARM7TDMI RISC Processor

- Best-selling 32-bit RISC processor
- Binary and source code compatible with other ARM7/ARM7TDMI variants
- Widespread C/C++ compiler, source-level debugger, and RTOS support
- Superior code density using the Thumb® instruction set
- 54 MIPS (Dhrystone 2.1) at 60 MHz
- Low latency, real-time interrupt response
- Fast hardware multiplier
- 32-bit register bank and ALU
- 32-bit addressing — 4G-byte linear address
- 32-bit barrel shifter
- EmbeddedICE™ on-chip debugger

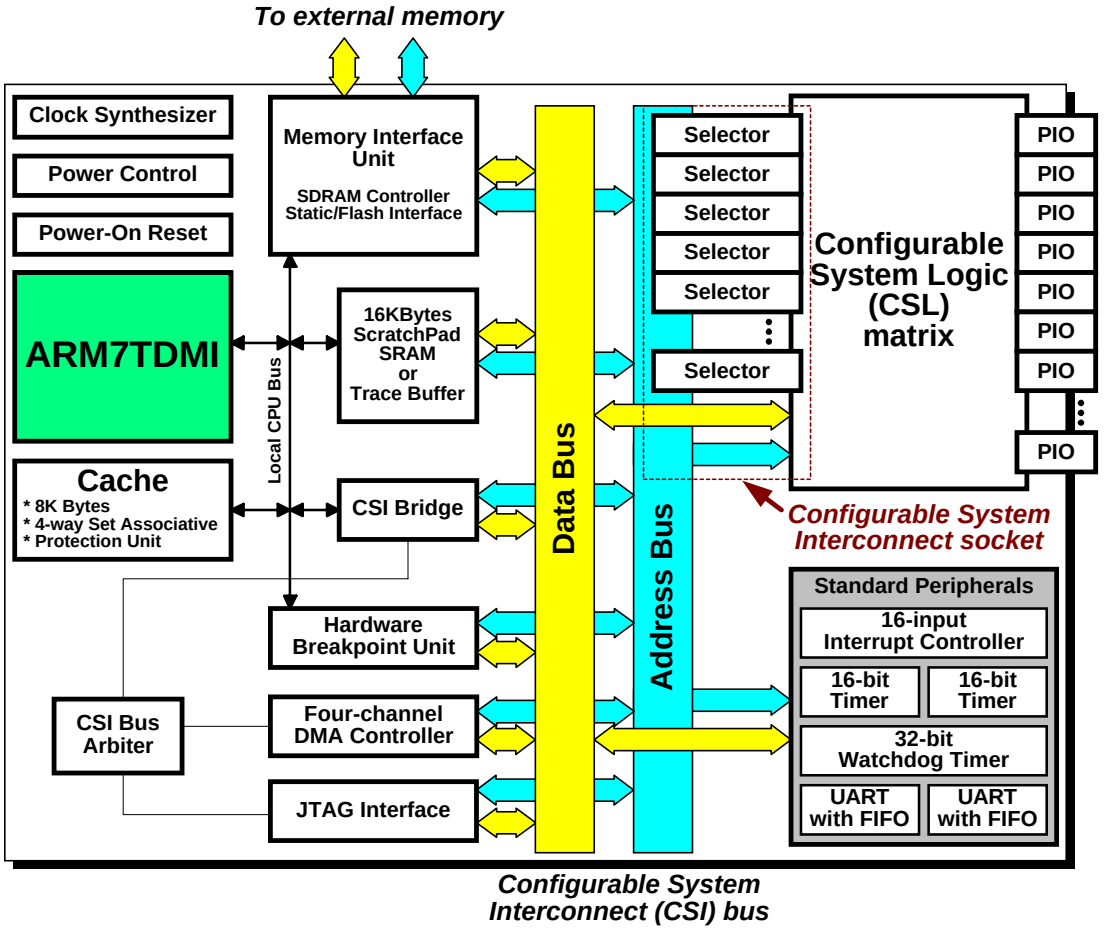


Figure 1. Block diagram of the Triscend A7 Configurable System-on-Chip (CSoC).

Table 1. Triscend A7 Configurable System-on-Chip Family

Device	Embedded Processor Core	Dedicated Resources	System RAM	Configurable System Logic (CSL) Cells	CSI Address Selectors	PIO* Pins (Max)
TA7S05	**ARM7TDMI** 32-bit RISC CPU 8K unified cache Barrel shifter Hardware multiplier Thumb extensions Debug extensions	Flash memory interface SDRAM memory interface 4-channel DMA controller Two 16C550-style UARTs Two 16-bit timers 32-bit watchdog timer 16-input interrupt controller Power management Power-on reset Hardware breakpoint unit JTAG debugger	4Kx32	512	32	124
TA7S12				1,152	72	188
TA7S20				2,048	128	252
TA7S32				3,200	200	316

* Maximum PIO on each base device, actual PIO count depends on package style and initialization mode. See Table 62.
Shaded entries are fabricated on 0.18µ CMOS.

Rich set of embedded support peripherals

- 4-channel high-performance DMA controller
  - fly-by performance
  - memory-to-memory transfers
  - linked-list DMA
  - frame transfer support
- Memory Subsystem Interface Unit (MSSIU) for flexible, glueless interface to external memories (ROM, EEPROM, Flash, SRAM, and SDRAM)
- Two 16C550-style serial ports (UART) with modem interface
- Two 16-bit timers/counters
- 32-bit Watchdog timer
- 16-input interrupt controller with fast interrupt response
- IEEE 1149.1 enhanced JTAG interface
- In-system debug/breakpoint unit
- Power-on reset
- Power-down and power-management modes

Full-Featured Memory Interface Unit

- Simultaneous support for independent external Flash and SDRAM memory sub-systems using x8 or x16 memory devices
- Expandable external data bus: 8-bit, 16-bit and 32-bit support
- Up to two external SDRAM banks
- Automatic support for self-refresh, auto-refresh and initialization of SDRAM
- Programmable SDRAM parameters for optimal memory bandwidth

Embedded SRAM-based Configurable System Logic (CSL) matrix

- Next-generation embedded programmable logic architecture, optimized with processor and bus interface
- Over 3,800 flip-flops and 300 programmable inputs and outputs (PIOs)
- Abundant, flexible interconnect structure with easy access to and from system bus
- Dedicated circuitry for fast adders, counters, and multipliers
- CSL cells optionally used as distributed memory, including true dual-port operation
- Six independent low-skew clock or global signal distribution buffers plus bus clock
- Supported by standard logic design tools
  - VHDL and Verilog logic synthesis
  - Schematic entry
  - VHDL and Verilog simulation

High performance dedicated system bus

- Configurable System Interconnect (CSI) bus integrates CSL matrix, CSoC system
- 455M-bytes per second peak transfer rate
- 32-bit address bus and 32-bit data bus
- Programmable wait-state support
- Openly-defined CSI Socket bus interface to CSL matrix
  - CSL peripheral addresses independent of placement in CSL matrix
  - CSL peripherals compatible with past and future CSoC families
- Ten bus masters and built-in arbitration
  - ARM7TDMI™ CPU
  - Four-channel DMA controller
  - JTAG interface

System Overview

The Triscend A7 Configurable System-on-Chip (CSoC) device is a complete, high-performance user-programmable system. The A7 contains

- an embedded 32-bit ARM7TDMI RISC processor
- a next generation embedded programmable logic architecture, optimized for processor and bus interface
- a high-performance 32-bit internal bus supporting up to 455M-bytes per second peak transfer rates
- 16K-bytes of internal scratchpad SRAM memory and a separate 8K-byte cache.

The ARM7TDMI is a general-purpose 32-bit RISC microprocessor that supports the complete ARM 32-bit instruction set and the reduced 16-bit instruction set, referred to as Thumb. The ARM7TDMI processor offers the following advantages:

- High-performance for very low power consumption and price
- Excellent code density using the Thumb instruction set
- Low-latency interrupt response

ARM7TDMI Processor System with Cache, Scratchpad RAM

The processor is paired with an 8K-byte unified code/data cache and a 16K-byte (4Kx32) scratchpad RAM for storing timing critical code or data. The scratchpad is accessible over the Configurable System Interconnect (CSI) bus by other CSI bus masters, primarily for DMA transfers. The ARM processor is integrated with other system components and the Configurable System Logic (CSL) matrix to provide a complete configurable system, as illustrated in Figure 1.

Next-Generation Embedded Programmable Logic Architecture

The embedded SRAM-based Configurable System Logic (CSL) matrix provides full, easy-to-use system customization. The high-performance programmable logic architecture consists of a highly interconnected matrix of CSL cells. Resources within the matrix provide seamless access to and from the internal CSI bus. Each CSL cell performs various potential functions, including combinatorial and sequential logic. The combinatorial portion performs Boolean logic operations, arithmetic functions, and memory. The sequential element performs independently or in tandem with the combinatorial function. The abundant programmable input/output blocks (PIOs) provide a highly flexible interface between external functions and the internal system bus or configurable system logic. Each PIO offers advanced I/O capabilities including selectable output drive current, optional input hysteresis, and programmable low-power functionality during power-down mode.

Internal, High-Performance Bus

A high-performance internal system bus—called the Configurable System Interconnect (CSI) bus— interconnects the embedded processor, its peripherals, and the CSL matrix at a maximum speed of 60MHz. The bus simultaneously provides 32 bits of read data, 32 bits of write data, and a 32-bit address. Multiple bus masters arbitrate for bus access. Potential bus masters include the ARM7TDMI processor, the read and write channels of all four DMA channels, and the JTAG interface. CSL-based devices become CSI bus masters using DMA services. The CSI bus and the local CPU bus following the little endian format.

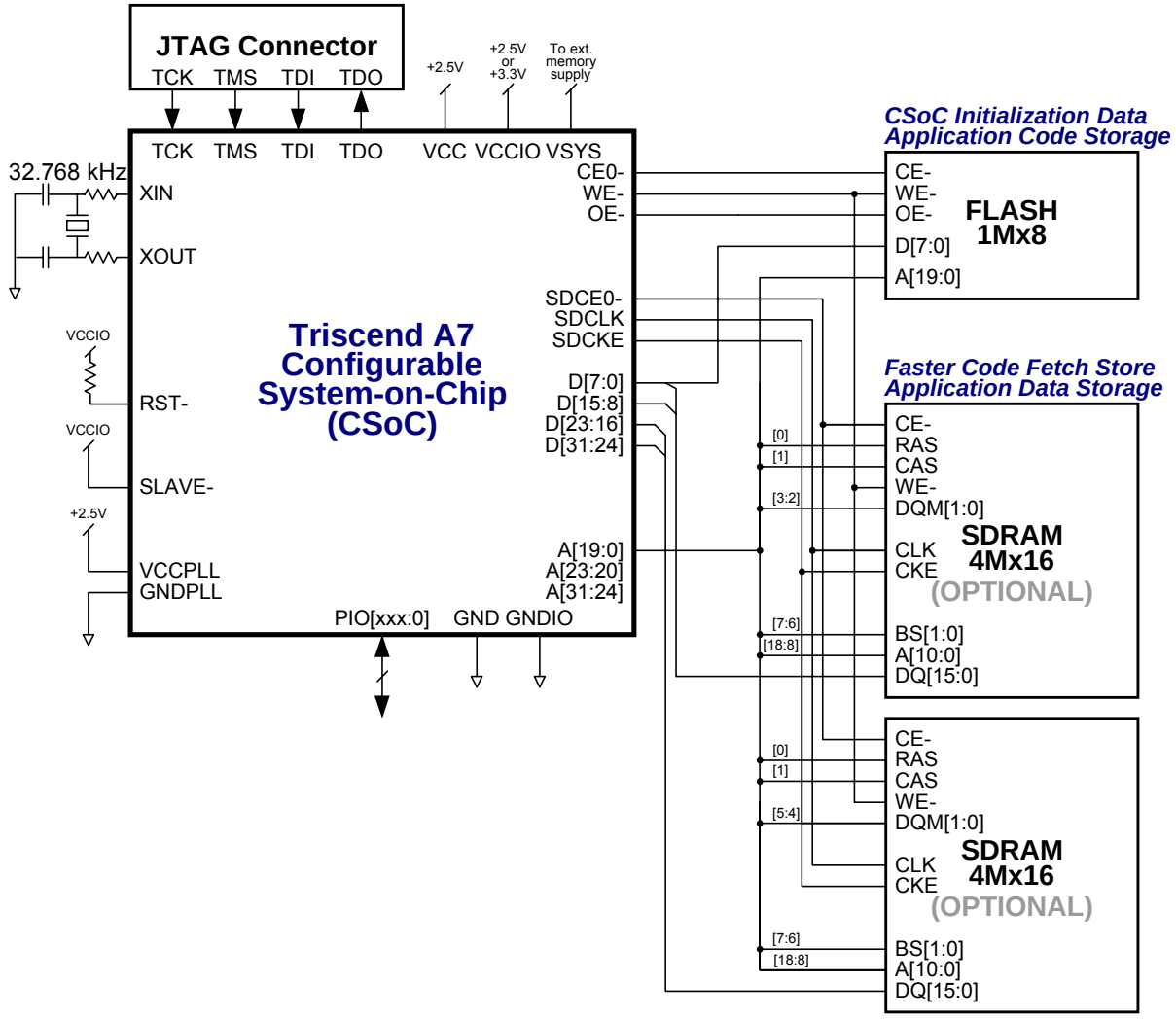


Figure 2. A typical A7-based system.

External Interface to Flash, SDRAM

A static memory interface unit seamlessly connects the A7 device to external static memories such as Flash or SRAM, as shown in Figure 2. An external Flash memory device contains the A7's initialization boot program plus the system application code. The external memory interface has programmable read/write control and chip-select signals that provide flexible set-up, strobe, and hold timing. The CPU connects directly to external memory, eliminating any potential latency incurred by using the CSI bus. For low frequency or minimal applications, the ARM7TDMI processor directly fetches its instructions from external Flash.

The A7 optionally supports external SDRAM, offering additional affordable and high-density memory to the system. The SDRAM interface connects an A7-based system to a variety of SDRAM types and configurations, including 100-pin DIMMs. The SDRAM interface operates at up to 60 MHz and provides options to optimize the interface timing for slower system clocks. SDRAM memory is ideal for DMA buffers. Similarly, the application program can be stored in slow, cheap, byte-wide Flash and copied into SDRAM at power-up. Then, the CPU starts executing code from the wider and faster SDRAM memory. The Flash and SDRAM interfaces share device pins, as shown in Figure 2.

Four-Channel DMA

The four-channel DMA controller provides high-bandwidth communication between CSL-based I/O devices, at up to 228M bytes per second, per direction. The easy-to-use DMA handshake simplifies interface and control logic within the CSL. The DMA controller provides advanced capabilities such as linked-list and frame-transfer support.

Dedicated Peripherals

The A7 also offers a set of common dedicated peripherals including

- two 16-bit timers with pre-scalers,
- two 16C450/550-like serial controllers (UART), with an optional modem interface
- a 32-bit watchdog timer, and
- an interrupt controller.

Complete Single-Chip System

The majority of the system, including the CPU, operates from a single clock signal. The clock source is typically driven directly via an external pin or connected to the on-chip PLL clock synthesizer. The clock synthesizer operates from an external 32.768 kHz watch crystal. Additionally, an internal ring oscillator is provided. Six other global buffers provide high-fanout signals to CSL functions. The bus clock and the global buffers are optionally stopped upon a breakpoint event and shut off during power-down mode.

Power management controls provide selectable power-down options over internal functions. Furthermore, each PIO provides pin-by-pin power-down settings.

An internal initialization boot ROM controls device initialization after power-on or after the reset pin is released. The initialization boot ROM locates user's initialization data and code stored in external Flash or other non-volatile memory. The Triscend FastChip development system programs external Flash via the A7's JTAG port.

Additionally, the JTAG interface provides real-time, in-system debugging capabilities, eliminating the need for an external emulator. The JTAG interface has full access and control over the CPU, peripherals, and CSL functions during debugging.

When debugging application software, the A7 employs the rich set of standard ARM7TDMI debugging tools. The A7 fully supports the standard ARM internal breakpoint and watchpoint capabilities. In addition, the A7's breakpoint unit monitors both the CPU local bus or the CSI bus. Upon a predefined set of conditions, the breakpoint unit halts or interrupts the execution of the application program. The breakpoint unit also supports real-time tracing of local CPU bus or the CSI bus transactions.

All together, the Triscend A7 Configurable System-on-Chip (CSoC) platform offers unparalleled time-to-market and performance advantages for embedded system designs.

A7 Development Support

The Triscend A7 Configurable System-on-Chip (CSoC) platform is supported by a variety of third-party development tools including compilers, debuggers, real-time operating systems (RTOS), and in-system debuggers/emulators as shown in Table 2. Most compilers that support the ARM7 architecture also support the Triscend A7 CSoC device. To accelerate development, there are multiple development boards available, shown in Table 3. Additionally, Triscend provides a free Software Development Kit (SDK) that includes board support packages (BSPs) for leading RTOS environments and a source-level driver library.

The A7's Configurable System Logic (CSL) matrix is well supported by a variety of logic design entry solutions, including both VHDL or Verilog logic synthesis and schematic entry as shown in Table 2. Likewise, there are VHDL and Verilog simulation models available for popular logic verification tools.

Table 2. Supported Development Tools for A7 CSoC.

ARM7TDMI Software Development

Triscend Software Development Kit (SDK)

- Source-level device driver library
- Board Support Packages (BSPs)

Compilers

- Wind River Diab C/C++™ Compiler
- ARM® Developer Suite (ADS) C/C++ Compiler
- GNU C Compiler (GCC)

Source-Level Debuggers

- Wind River visionCLICK, in-system support using Wind River visionPROBE II
- ARM eXtended Debugger (AXD)
- GNU gdb Debugger

Real-Time Operating System (RTOS) Support

- Wind River Tornado/VxWorks®
- Red Hat eCos™
- Red Hat µClinux

JTAG-Based Hardware Emulators/Debuggers

- Wind River visionPROBE II (ARM and CSoC debugging)
- ARM Mutli-ICE™ (ARM only debugging)
- EPI JEENI and MAJIC™ (ARM only debugging)

CSoC/Logic Design Development

Triscend FastChip CSoC Development System

- Graphical development/integration environment, Windows-based
- Drag-and-drop Soft Module library
- Create initialization images for Triscend CSoC devices
- Download directly or program external Flash via JTAG
- Seamless integration with third-party microprocessor and logic design tools
- Powerful real-time, in-system debugging

VHDL/Verilog Logic Synthesis

- Synplicity® Synplify®
- Synopsys® FPGA Compiler II

Schematic Entry

- Cadence/OrCAD Capture
- SpinCircuit eCapture
- Innoveda ViewDraw

VHDL Logic Simulation

- Model Technology™ ModelSim
- Innoveda Fusion/Speedwave
- VITAL/SDF support

Verilog Logic Simulation

- Model Technology™ ModelSim
- Cadence® Verilog XL®
- Synopsys® VCS
- Triscend CSI Bus Functional Model

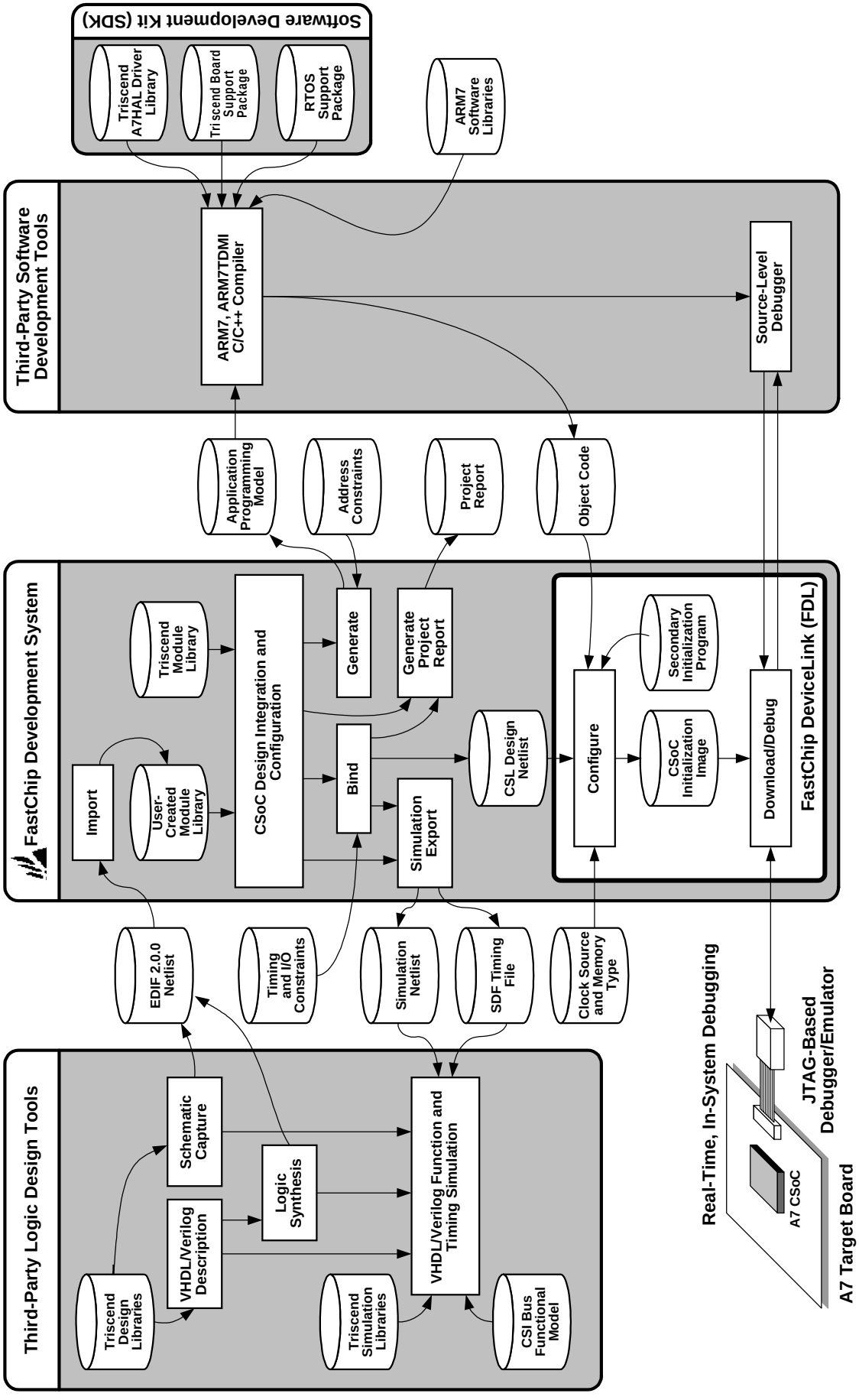


Figure 3. Detailed Triscend A7 Development Flow.

Table 3. A7 Development Boards.

Supplier	Part Number
Triscend Corporation	THW-KIT-720
Embedded Performance Inc. (EPI)	Dev-A7

PC-Based Development Platform

Figure 3 presents a detailed view of the entire Triscend A7 development flow. FastChip is a Windows-based application and operates on most PC-compatible computers with the recommended minimum 192M-bytes of RAM memory. The Triscend FastChip development system provides design integration and configuration capabilities, working in conjunction with third-party logic design and software development tools.

Powerful FastChip CSoC Development System

FastChip includes a powerful Soft Module library of commonly used embedded systems functions like additional UARTs, timers, various bus interfaces, etc. Likewise, FastChip includes libraries that allow designers to create custom functions using third-part logic design and simulation tools. Designs imported into FastChip via an EDIF 2.0.0 netlist become FastChip modules.

FastChip also exports a CSoC designs for either VHDL or Verilog logic simulation purposes. A Triscend-provided bus functional model simulates traffic on the A7's internal CSI bus.

Seamless Integration with ARM7TDMI Compiler

After defining the A7's logic, FastChip's Bind utility creates the physical hardware implementation for the CSoC device. Similarly, FastChip's Generate utility allocates addresses for any functions attached to the Configurable System Interconnect (CSI) bus and creates an application programming model for a third-party ARM compiler. This model includes register definitions for both standard ARM7TDMI functions and any custom hardware.

FastChip combines the output from the Bind utility and the object code from the ARM7TDMI compiler to create a CSoC initialization image. Using this image, FastChip either directly downloads to an A7 device or programs external Flash memory attached to the A7. Optionally, the initialization image can be saved as an Intel Hex file four use with an external device programmer.

Real-time, In-system, Full-Speed Debugging

Furthermore, FastChip provides a real-time, in-system debugging environment using the actual A7 production silicon with the actual system hardware and application software. FastChip drives a supported JTAG-based debugger/emulator and provides interfaces to third-party source-level debuggers. Via a source-level debugger, software developers have register-level access to the A7 device, complete with breakpoints and trace. FastChip's Debug utility also provides logic debugging capabilities, including the ability to probe flip-flop values and the outputs of CSL cells.

FastChip's Configure and Download/Debug utilities are packaged as a separate, standalone application called FastChip Device Link (FDL), providing software developers with necessary software development capabilities without the complexity of the entire FastChip CSoC development system.

Comprehensive Technical Support

The Triscend A7 Configurable System-on-Chip family and the FastChip development system are supported by a world-wide network of factory-trained field applications engineers. Additionally, the Triscend SupportCenter provides online support via the world-wide web at http://support.triscend.com or via E-mail at SupportCenter@Triscend.com.

Resources

Web Sites

ARM7TDMI Information

www.arm.com

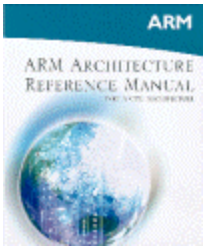
ARM Development Guide

www.embedded.com/directories/embedded/arm2000/index.html

ARM Resources Links

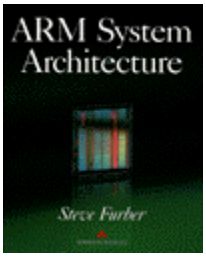
www.bluewaternz.com/links.htm

Books



ARM Architecture Reference Manual
D. Jaggar, David Seal
Prentice Hall:
ISBN 0201737191

ARM System-on-Chip Architecture (Second Edition)
S. Furber
Addison-Wesley:
ISBN 0201675196



ARM System Architecture
S. Furber
Addison-Wesley:
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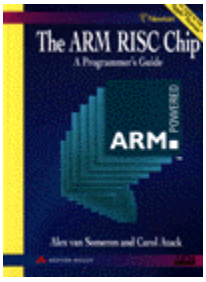
ISBN 4789833518



The ARM RISC Chip, A Programmer's Guide
A. van Someron and C. Atack
Addison-Wesley:
ISBN 0201624109

Pin Description

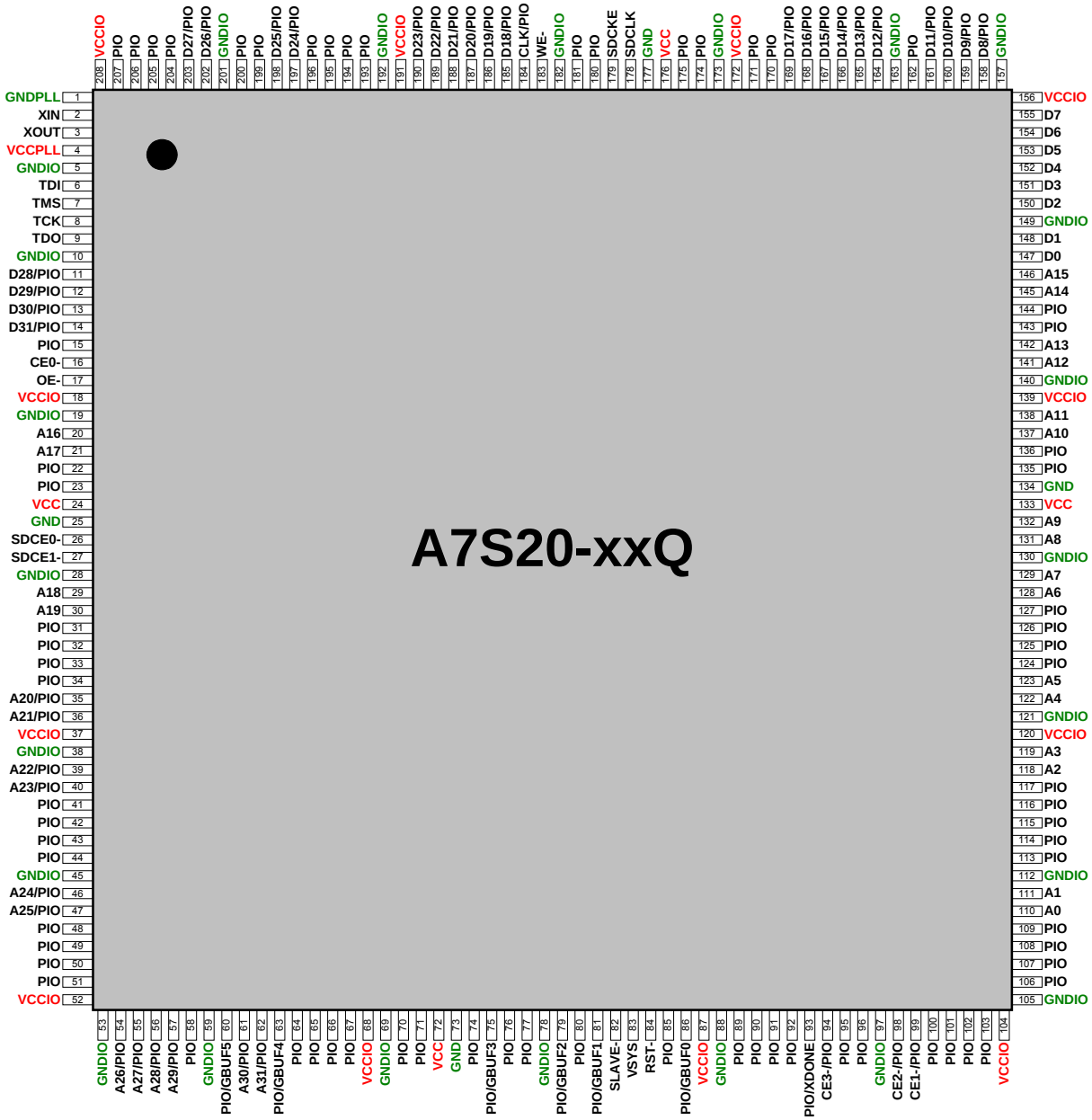
Table 60 describes the pins available on an A7 configurable system-on-chip (CSoC) device. The directionality of each pin is described during parallel mode initialization. After initialization, all PIO pins and the indicated system pins are available as user-defined I/O signals.

Table 60. Pins available on an A7 configurable system-on-chip and their function.

Pin Name	Pin Description	Parallel
A[19:0]	Address bus bits. These pins cannot be reclaimed as user-defined PIO pins.	O
CE0-	Active-Low chip-enable output to external memory. Enables all bytes in an 8-bit subsystem, or the first byte of a 16-bit or 32-bit subsystem, or the first half-word of a 32-bit subsystem using 16-bit wide memories. This pin cannot be reclaimed as a user-defined PIO pin.	O
CE[3:1]-/PIO	Optional active-Low byte-lane chip-enable signals. Used to enable external memory during byte or half-word addressing in 16-bit or 32-bit Flash memory subsystems. If not used as chip-enables, these pins may be reclaimed as user-defined PIO pins.	O
CLK/PIO	External clock source input. Can be reclaimed as a PIO pin if not used as the system clock source.	I
D[7:0]	Data bus bits. These pins cannot be reclaimed as user-defined PIO pins.	I
DQ[31:8]	Optional upper 24 bits of the Data bus. These pins may be reclaimed as user-defined PIO pins. Until initialization is complete, these pins have an internal high-impedance pull-up resistor.	I
GND	Ground connection for internal (non-PIO) logic. All must be connected.	I
GNDIO	Ground connection for PIO functions. All must be connected.	I
GNDPLL	Ground connection for the phase-locked loop (PLL). Must be connected.	I
N.C.	No connect. There is no function on this pin.	N.C.
OE-	Active-Low output-enable signal to read from external memory.	O
PIO	General-purpose input, output, or bi-directional signal pin after initialization is complete. Before initialization is complete, these pins have internal high-impedance pull-up resistors that pull the signal pin to a High logic level.	I (pull-up)
PIO/A[23:20]	Typically, a general-purpose input, output, or bi-directional signal pin after initialization is complete. Before initialization is complete, these pins have an internal high-impedance pull-up resistor that pulls the signal pin to a High logic level. These pins optionally extend the Flash subsystem address up to the maximum 16M-bytes allowed after initialization. Any unused address lines may be used as user-defined PIO pins.	I (pull-up)
PIO/A[31:24]	Typically, a general-purpose input, output, or bi-directional signal pin after initialization is complete. Before initialization is complete, these pins have an internal high-impedance pull-up resistor that pulls the signal pin to a High logic level. These pins are optionally used as the upper 8-bit of the 32-bit CSI bus address during testing.	I (pull-up)
PIO/GBUF5 PIO/GBUF4 PIO/GBUF3 PIO/GBUF2 PIO/GBUF1 PIO/GBUF0	Global buffer input. Typically, a general-purpose input, output, or bi-directional signal pin after initialization is complete. Before initialization is complete, this pin has an internal high-impedance pull-up resistor that pulls the signal pin to a High logic level.	I (pull-up)

Pin Name	Pin Description	Parallel
PIO/XDONE	General-purpose input, output, or bi-directional signal pin after initialization is complete. Before initialization is complete, this pin has an internal high-impedance pull-up resistor that pulls the signal pin to a High logic level. This pin is optionally used during testing.	I (pull-up)
RST-	Active-Low device reset input. Connect to VCCIO with a pull-up resistor. Do not allow it to float.	I
SDCE[1:0]-	Active-Low SDRAM chip-enable signals. If not used, leave unconnected.	O
SDCKE	SDRAM clock enable signal. Disables SDRAM during power-down conditions. If not used, leave unconnected.	O
SDCLK	SDRAM clock source. All SDRAM operations are synchronized to the rising edge of this signal. If not used, leave unconnected.	O
SLAVE-	Test slave mode. Connect to VCCIO. Do not allow it to float.	I
TCK	JTAG Test Clock input. Tie High if unused.	I
TDI	JTAG Test Data Input. Tie High if unused.	I
TDO	JTAG Test Data Output.	O
TMS	JTAG Test Mode Select input. Tie High if unused.	I
VCC	Supply voltage for internal logic functions, separate from I/O. Connect to a +2.5-volt supply. DO NOT CONNECT TO +3.3-VOLT SUPPLY. All must be connected and each must be decoupled with a 0.01 to 0.1 µF capacitor to ground.	I
VCCIO	Supply voltage for I/O functions, separate from internal logic. Connect all to a +2.5-volt or +3.3-volt supply, depending on external interface requirements. All must be connected and each must be decoupled with a 0.01 to 0.1 µF capacitor to ground.	I
VCCPLL	Supply voltage for phase-locked loop circuitry. Connect to a +2.5-volt supply. Must be connected and decoupled with a 0.01 to 0.1 µF capacitor to ground.	I
VSYS	External 'system voltage-good' indicator input. Indicates when external devices, such as the external Flash, have sufficient operating voltage. In most applications, connect VSYS to VCCIO supply source. If VSYS is High during initialization and no valid configuration is found, the CSoC device automatically powers down to conserve power. If VSYS is tied Low, the CSoC device attempts to initialize itself until it finds valid initialization data. This pin must be connected. Do not allow it to float.	I
WE-	Active-Low write-enable signal to write to external memory. Used to program external Flash-based devices.	O
XIN	The input from an external 32.768 kHz watch crystal into the internal crystal oscillator amplifier. Connect to one side of the external crystal as shown in Figure 47. Connect to GNDIO if not using an external crystal.	I
XOUT	Output from the 32.768 kHz internal crystal oscillator amplifier. Connect to one side of the external Hz watch crystal. Leave unconnected if not using an external crystal.	I/O

208-pin PQFP Package Footprint Diagram



(Top View)

324-ball BGA Package Footprint Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	GND PLL	PIO	PIO	D22/ PIO	D21/ PIO	D20/ PIO	D19/ PIO	WE-	SD CKE	SD CLK	D17/ PIO	D15/ PIO	D13/ PIO	D11/ PIO	D10/ PIO	D9/ PIO	D8/ PIO	D5
B	XIN	D25/ PIO	PIO	D27/ PIO	D26/ PIO	D24/ PIO	D23/ PIO	D18/ PIO	CLK/ PIO	PIO	D16/ PIO	D14/ PIO	D12/ PIO	PIO	PIO	PIO	D7	D3
C	XOUT	TDI	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	D6	D2
D	VCC PLL	TMS	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	D4	D1
E	GNDIO	TCK	PIO	PIO	VCCIO	VCCIO	VCCIO	PIO	PIO	PIO	PIO	VCCIO	VCCIO	VCCIO	PIO	PIO	D0	A14
F	D28/ PIO	TDO	PIO	PIO	VCCIO	VCCIO	GNDIO	GNDIO	VCC	GND	GNDIO	GNDIO	VCCIO	VCCIO	PIO	PIO	A15	PIO
G	D30/ PIO	D29/ PIO	PIO	PIO	VCCIO	GNDIO	GNDIO	GNDIO	VCC	GND	GNDIO	GNDIO	GNDIO	VCCIO	PIO	PIO	PIO	PIO
H	CE0-	D31/ PIO	PIO	PIO	PIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	PIO	PIO	PIO	PIO	A12
J	A16	OE-	PIO	PIO	PIO	VCC	VCC	GNDIO	GNDIO	GNDIO	GNDIO	GND	GND	PIO	PIO	PIO	A8	A10
K	A17	PIO	PIO	PIO	PIO	GND	GND	GNDIO	GNDIO	GNDIO	GNDIO	VCC	VCC	PIO	PIO	PIO	A6	A13
L	SD CE0-	PIO	PIO	PIO	PIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	GNDIO	PIO	PIO	PIO	PIO	A11
M	SD CE1-	PIO	PIO	PIO	VCCIO	GNDIO	GNDIO	GNDIO	VCC	GND	GNDIO	GNDIO	GNDIO	VCCIO	PIO	PIO	PIO	A9
N	A18	A20/ PIO	PIO	PIO	VCCIO	VCCIO	GNDIO	GNDIO	VCC	GND	GNDIO	GNDIO	VCCIO	VCCIO	PIO	PIO	A4	A7
P	PIO	A19	PIO	PIO	VCCIO	VCCIO	VCCIO	PIO	PIO	PIO	PIO	VCCIO	VCCIO	VCCIO	PIO	PIO	PIO	A5
R	A22/ PIO	A21/ PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	A3
T	A23/ PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	A2
U	A24/ PIO	A26/ PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO	PIO/ XDONE	CE2-/ PIO	A1
V	A25/ PIO	A27/ PIO	A28/ PIO	A29/ PIO	PIO/ GBUF5	A30/ PIO	A31/ PIO	PIO/ GBUF4	PIO/ GBUF3	PIO/ GBUF2	PIO/ GBUF1	SLAVE-	VSYS	RST-	PIO/ GBUF0	CE3-/ PIO	CE1-/ PIO	A0

(Top view, through top of package to solder balls underneath)

Electrical and Timing Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{CC}	Core logic supply voltage relative to GND	-0.5	3.0	V
V_{CCIO}	PIO supply voltage relative to GND	-0.5	4.0	V
V_{IN}	Input voltage relative to GND [1]	-0.5	4.0	V
V_{TS}	Voltage applied to three-state output [1]	-0.5	4.0	V
T_{STG}	Storage temperature (ambient)	-60	+150	° C
T_{SOL}	Maximum soldering temperature (10 sec at 1/16 in. = 1.5 mm)		+260	° C
T_J	Junction temperature, plastic packages		+125	° C

Recommended Operating Conditions/DC Characteristics

Symbol	Parameter	Min	Max	Units
V_{CC}	Core logic supply voltage relative to GND	2.3	2.7	V
V_{CCIO}	PIO supply voltage relative to GND	2.3	3.6	V
T_J	Operating junction temperature, commercial [3]	0	+85	° C
	Operating junction temperature, industrial [3]	-40	+100	° C
V_{CCR}	Longest supply voltage rise time from 1V to 3V [4]		200	ms
V_{IL}	Input Low voltage	0	30% V_{CC}	V
V_{IH}	Input High voltage	50% V_{CC}	V_{CC}+0.5	V
V_S	Schmitt Hysteresis, hysteresis mode	5% VCC	20% VCC	V
V_{ESD}	Electro-static discharge protection, human body model	2 000		V
T_{IN}	Input signal transition time		250	ns
V_{OL}	Output Low voltage, I_{OL} = -16 mA, V_{CC} min (TTL) [5]		0.4	V
	Output Low voltage, I_{OL} = -1.5 mA, V_{CC} min (LVCMOS)		10% VCC	V
V_{OH}	Output High voltage, I_{OH} = 8 mA, V_{CC} min (TTL) [5]	2.4		V
	Output High voltage, I_{OH} = 0.5 mA, V_{CC} min (LVCMOS)	90% VCC		V
V_{DR}	Data retention supply voltage of internal core logic (below which initialization data may be lost)	2.5		V
V_{DRIO}	Data retention supply voltage of PIO (below which initialization data may be lost)	2.1		V
I_{OL}	Output Low current, output in highest drive strength mode (TTL), V_{OL} max, V_{CC} min		-16.0	mA
	Output Low current, output in lowest current drive mode (TTL), V_{OL} max, V_{CC} min		-4.0	mA
	Output Low current (LVCMOS), V_{OL} max, V_{CC} min		-1.5	mA
I_{OH}	Output High current, output in highest drive strength mode (TTL), V_{OH} min, V_{CC} min		+8.0	mA
	Output High current, output in lowest drive strength mode (TTL), V_{OH} min, V_{CC} min		+2.0	mA
	Output High current (LVCMOS), V_{OH} min, V_{CC} min		+0.5	mA
I_{IL}	Input leakage current	-10	+10	µA
C_{IO}	Pin capacitance [7]		10	pF
L_{IO}	Pin inductance [7]		20	nH

Note 1: Maximum DC overshoot above VCC or undershoot below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, device pins may undershoot to -2.0 V or overshoot to +5.0 V, provided this condition lasts less than 20 ns and with less than 100 mA forcing current.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent device damage. The values listed are stress ratings only. Functional operation of the device at these or any conditions exceeding those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

Note 3: Typical ambient operating conditions are between 0 to +70° C for commercial devices and -40 to +85° C for industrial devices, depending on the application's power consumption, package style, and airflow.

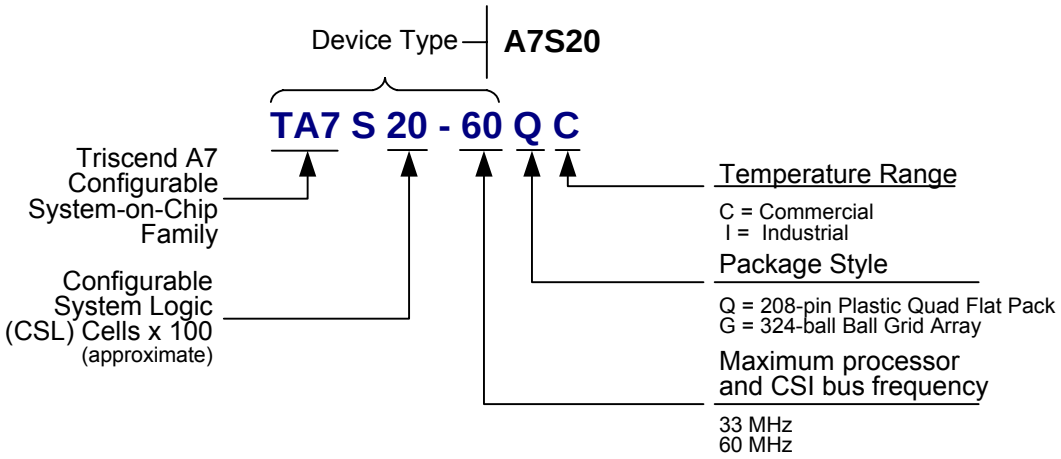
Note 4: Ramp rate can be extended by asserting RST- until V_{CC} reaches the minimum specified value.

Note 5: Output in highest drive strength mode.

Note 6: Continuous static loads must fall within the I_{OH}, I_{OL} limits in this section.

Note 7: Capacitance and inductance is sample-tested only.

Ordering Information



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