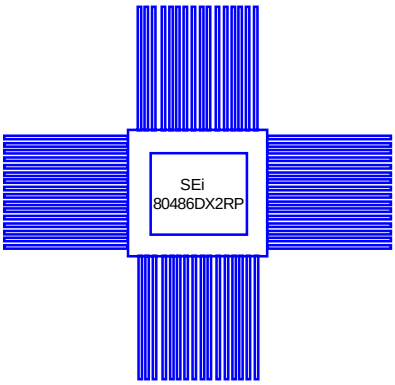
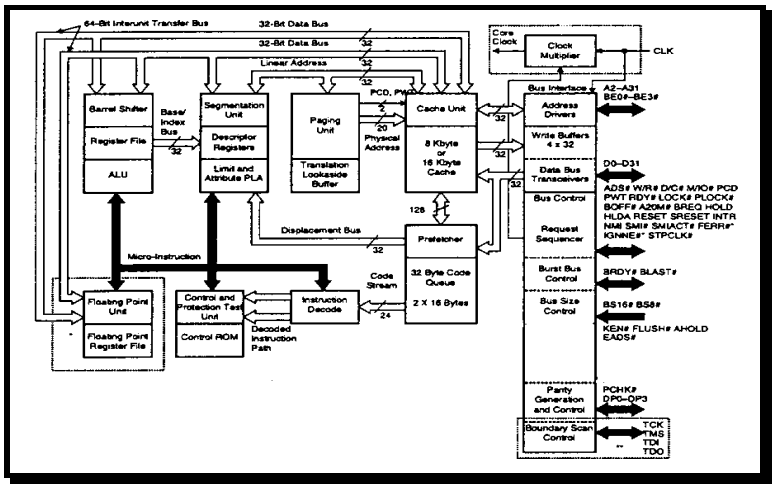
80486DX2RP

RADIATION HARDENED 32-BIT MICROPROCESSOR





FEATURES:

- 32-Bit Microprocessor
- Total Dose Hardness: typical 100 Krad (Si); dependent upon orbit
- Single Event Effect
  - $SEL_{TH} = 59.6$ MeV/mg/cm^2
  - $SEU_{TH} = 5$ MeV/mg/cm^2
- Package:
  - 208 Pin RAD-PAK® Quad Flat Pack
- 8-Kilobyte On-Chip Cache with Consistency Support
- External Cache Controller
- Integrated Floating-Point Unit
- Single Cycle Execution
- 32-Bit RISC Integer Core
- Instruction Pipelining
- On-Chip Management Unit
- Write Buffers
- Bus Backoff
- Instruction Restart
- On Chip Floating Point Unit

DESCRIPTION:

Space Electronics' 80486DX2RP (RP for RAD-PAK®) high-performance 32-bit microprocessor features a typical 100krad (Si) total dose tolerance. The 80486DX2RP processor integrates an 8K unified cache and floating-point (FPU) hardware-on-chip. The on-chip memory management unit is completely compatible with the 80386 processor. The on-chip cache memory allows frequently used data and code to be stored on-chip, reducing accesses to the external bus. Its speed-multiplying technology, allowing the processor to operate at frequencies higher than the external memory bus. The clock multiplier on the 80486DX2RP improves execution performance without increasing board design complexity. It enhances all operations operating out of the cache and/or not blocked by external bus accesses. The burst bus feature enables fast cache fills. The patented radiation-hardened RAD-Pak® technology incorporates radiation shielding in the microcircuit package. It provides a 100 Krad or better (Si) total dose survivability, based on a GEO-type orbit. Actual TID tolerance is dependent upon orbit and mission duration. Capable of surviving in-space environment, the 80486DX2RP is ideal for satellite, spacecraft, and space probe missions. It is available in Class S packaging and screening.

80486DX2RP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage Respect to Ground	V_{CC}	-0.5	+6.5	V
DC Voltage on Other Pins with Respect to Ground		-0.5	V_{CC} + 0.5	V
Operating Temperature Range	T_{OPR}	-55	+125	^{O}C
Storage Temperature Range	T_{STG}	-65	+150	^{O}C

80486DX2RP OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Digital Supply Voltage	V_{CC}	4.5	5.5	V
Temperature Range	T_A	-55	+125	^{O}C

80486DX2RP DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC}=5V $\pm$ 10%, T_A = -55 to +125°C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNIT
Input Leakage Current	Inputs without Pull-ups or pull-downs $0V < V_{IN} < V_{CC}$	I_{LI}	-15	+15	μA
Output Leakage Current		I_{LO}	-15	+15	μA
UP# Active Supply Current	3/	I_{CCU}		50	mA
Input Leakage Current	1/ 5/	I_{IH}		200 300	μA
Input Leakage Current	2/	I_{IL}		-400	μA
Input Low Voltage		V_{IL}	-0.3	0.8	V
Input High Voltage		V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage	Address, Data, BEn 4.0mA Definition, Control 5.0mA	V_{OL}		0.45	V
Output High Voltage	Address, Data, BEn -1.0mA Definition, Control -0.9mA	V_{OH}	2.4		V
I_{CC} Active (Power Supply) 6/	f_{OP} = 50MHz f_{OP} = 66MHz			950 1200	mA
I_{CC} Active (Thermal Supply) 4/ 7/ 8/	f_{OP} = 50MHz f_{OP} = 66MHz			906 1145	mA
I_{CC} Stop Grant 9/	f_{OP} = 50MHz f_{OP} = 66MHz			70 90	mA
I_{CC} Stop Clock 10/	f_{OP} = 0MHz			2	mA
CLK2 Capacitance	@ 1MHz 4/	C_{CLK}		6	pF
Input Capacitance	@ 1MHz 4/	C_{IN}		10	pF
Output or I/O Capacitance	@ 1MHz 4/	C_{OUT}		10	pF

Note:

1/ This parameter is for inputs with pull-downs and V_{IH} = 2.4V.
2/ This parameter is for inputs with pull-ups and V_{IL} = 0.45V.
3/ When the processor is in Stop Grant state, the I_{CCU} of the host processor is less than 2 mA.
4/ Not 100% tested.
5/ This parameter is for inputs with pull-downs and V_{IH} = 2.4V. (SRESET pin only).

6/ This parameter is for proper power supply selection. It is measured using the worst case instruction mix at V_{CC} = 5.25V.
7/ The maximum current column is for thermal design power dissipation. It is measured using the worst case instruction mix at V_{CC} = 5V.
8/ The typical current column is the typical operating current in a system. This value is measured in a system using a typical device at V_{CC} = 5V, running Microsoft Windows 3.1 at an idle condition. This typical value is dependent upon the specific system configuration.
9/ The I_{CC} Stop Grant specification refers to the I_{CC} value once the processor enters the Stop Grant or Auto HALT Power Down state.
10/ The I_{CC} Stop Clock specification refers to the I_{CC} value once the processor enters the Stop Clock state. The V_{IH} and V_{IL} levels must be equal to V_{CC} and 0V, respectively, in order to meet the I_{CC} Stop Clock specifications.

80486DX2RP AC ELECTRICAL CHARACTERISTICS
(V_{CC}=5V ± 10%, T_A = -55 to +125°C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNIT
Operating Frequency 80486DX2RP-50 80486DX2RP-66	1/			 50 66	MHz
CLK Frequency 80486DX2RP-50 80486DX2RP-66			 8 8	 25 33	MHz
CLK Period 80486DX2RP-50 80486DX2RP-66		t_1	 40 30	 125 125	ns
CLK Period Stability 80486DX2RP-50 80486DX2RP-66		t_{1a}		 ±250 ±250	ps
CLK High Time 80486DX2RP-50 80486DX2RP-66	at 2V	t_2	 14 11		ns
CLK2 Low Time 80486DX2RP-50 80486DX2RP-66	at 0.8V	t_3	 14 11		ns
CLK Fall Time 80486DX2RP-50 80486DX2RP-66	2V to 0.8V	t_4		 4 3	ns
CLK2 Rise Time 80486DX2RP-50 80486DX2RP-66	0.8V to 2V	t_5		 4 3	ns
A2 - A31, PWT, PCD, BE0-3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, BREQ, HLDA, SMIACT#, FERR# Valid Delay 80486DX2RP-50 80486DX2RP-66		t_6	 3 3	 19 14	
A2 - A31, PWT, PCD, BE0-3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, BREQ, HLDA, Float Delay 2/ 80486DX2RP-50 80486DX2RP-66		t_7		 28 20	ns

80486DX2RP AC ELECTRICAL CHARACTERISTICS (continue)

(V_{CC}=5V ± 10%, V_{PP} = V_{SS}, T_A = -55 to +125°C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNIT
PCHK# Valid Delay		t_8			
80486DX2RP-50			3	24	ns
80486DX2RP-66			3	14	
BLAST#, PLOCK# Valid Delay		t_{8a}			
80486DX2RP-50			3	24	
80486DX2RP-66			3	14	ns
BLAST#, PLOCK# Float Delay 2/		t_9			
80486DX2RP-50				28	ns
80486DX2RP-66				20	
D0-D31, DP0-DP3 Write Data Valid Delay		t_{10}			
80486DX2RP-50			3	20	ns
80486DX2RP-66			3	14	
D0-D31, DP0-DP31 Write Data Float Delay 2/		t_{11}			ns
80486DX2RP-50				28	
80486DX2RP-66				20	
EADS# Setup Time		t_{12}			
80486DX2RP-50			8		ns
80486DX2RP-66			5		
EADS# Hold Time		t_{13}			
80486DX2RP-50			3		ns
80486DX2RP-66			3		
KEN#, BS16#, BS#, Setup Time		t_{14}			ns
80486DX2RP-50			8		
80486DX2RP-66			5		
KEN#, BS16#, BS# Hold Time		t_{15}			
80486DX2RP-50					ns
80486DX2RP-66			3		
			3		
RDY#, BRDY# Setup Time		t_{16}			
80486DX2RP-50			8		ns
80486DX2RP-66			5		
RDY#, BRDY# Hold Time		t_{17}			
80486DX2RP-50			3		ns
80486DX2RP-66			3		
HOLD, AHOLD Setup Time		t_{18}			
80486DX2RP-50			8		ns
80486DX2RP-66			6		
BOFF# Setup Time		t_{18a}			
80486DX2RP-50			8		ns
80486DX2RP-66			7		

80486DX2RP AC ELECTRICAL CHARACTERISTICS (continue)

(V_{CC}=5V ± 10%, V_{PP} = V_{SS}, T_A = -55 to +125◦C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNIT
HOLD, AHOLD, BOFF# Hold Time		t_{19}			ns
80486DX2RP-50			3		
80486DX2RP-66			3		
FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET, IGNNE# Setup Time		t_{20}			ns
80486DX2RP-50			8		
80486DX2RP-66			5		
FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET, IGNNE# Hold Time		t_{21}			ns
80486DX2RP-50			3		
80486DX2RP-66			3		
D0-D31, DP0-DP3, A4-A31 Read Setup Time		t_{22}			ns
80486DX2RP-50			5		
80486DX2RP-66			5		
D0-D31, DP0-DP3, A4-A31 Read Hold Time		t_{23}			
80486DX2RP-50			3		ns
80486DX2RP-66			3		

Note:
1/ 0-MHz operation is guaranteed when the STPCLK# and Stop Grant bus cycle protocol is used.
2/ Not 100% tested, guaranteed by design characterization.

80486DX2RP AC SPECIFICATIONS FOR THE TEST ACCESS PORT

(V_{CC}=5V ± 10%, V_{PP} = V_{SS}, T_A = -55 to +125◦C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNIT
TCK Frequency 1/		t_{24}		8	MHz
TCK Period		t_{25}	125		ns
TCK High Time	at 2.0V	t_{26}	40		ns
TCK Low Time	at 0.8V	t_{27}	40		ns
TCK Rise Time 2/		t_{28}		8	ns
TCK Fall Time 2/		t_{29}		8	ns
TDI, TMS Setup Time 3/		t_{30}	8		ns
TDI, TMS Hold Time 3/		t_{31}	10		ns
TDO Valid Delay 3/		t_{32}	3	30	ns
TDO Float Delay 3/		t_{33}		36	ns
All Outputs (Non-Test) Valid Delay 3/		t_{34}	3	30	ns
All Outputs (Non-Test) Float Delay 3/		t_{35}		36	ns
All Inputs (Non-Test) Setup Time 3/		t_{36}	8		ns
All Inputs (Non-Test) Hold Setup 3/		t_{37}	10		ns

Note:
1/ TCK period < CLK period.
2/ Rise/Fall times are measured between 0.8V and 2.0V. Rise/Fall times can be relaxed by 1 ns per 10-ns increase in TCK period.
3/ Parameters t_{30} - t_{36} are measured from TCK.

80486DX2RP PINOUT DESCRIPTION

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	36	Vss	71	NC	106	Vcc	141	D3	176	Vcc
2	Vcc	37	M/IO#	72	IGNNE#	107	Vss	142	D2	177	A14
3	Vcc	38	Vcc	73	STPCLK#	108	D16	143	D1	178	A13
4	PCHK#	39	D/C#	74	D31	109	DP2	144	D0	179	Vcc
5	BRDY#	40	PWT	75	D30	110	Vss	145	DP0	180	A12
6	BOFF#	41	PCD	76	Vss	111	Vcc	146	Vss	181	Vss
7	BS16#	42	Vcc	77	Vcc	112	D15	147	A31	182	A11
8	BS8#	43	Vss	78	D29	113	D14	148	A30	183	Vcc
9	Vcc	44	Vcc	79	D28	114	Vcc	149	A29	184	Vss
10	Vss	45	Vcc	80	Vcc	115	Vss	150	Vcc	185	Vcc
11	NC	46	EADS#	81	Vss	116	D13	151	A28	186	A10
12	RDY#	47	A20M#	82	Vcc	117	D12	152	A27	187	A9
13	KEN#	48	RESET	83	D27	118	D11	153	A26	188	Vcc
14	Vcc	49	FLUSH#	84	D26	119	D10	154	A25	189	Vss
15	Vss	50	INTR	85	D25	120	Vss	155	Vcc	190	A8
16	HOLD	51	NMI	86	Vcc	121	Vcc	156	Vss	191	Vcc
17	AHOLD	52	Vss	87	D24	122	Vss	157	Vss	192	A7
18	TCK	53	Vss	88	Vss	123	D9	158	A24	193	A6
19	Vcc	54	Vcc	89	Vcc	124	D8	159	A23	194	UP#
20	Vcc	55	Vss	90	DP3	125	DP1	160	A22	195	A5
21	Vss	56	Vcc	91	D23	126	D7	161	A21	196	A4
22	Vcc	57	Vss	92	D22	127	NC	162	Vcc	197	A3
23	Vcc	58	SRESET	93	D21	128	Vcc	163	Vcc	198	Vcc
24	CLK	59	SMIACT#	94	Vss	129	D6	164	A20	199	Vss
25	Vcc	60	Vcc	95	Vcc	130	D5	165	A19	200	Vcc
26	HLDA	61	Vss	96	NC	131	Vcc	166	A18	201	Vss
27	W/R#	62	Vcc	97	Vss	132	Vss	167	TMS	202	A2
28	Vss	63	NC	98	Vcc	133	Vcc	168	TDI	203	ADS#
29	Vcc	64	NC	99	D20	134	Vcc	169	Vcc	204	BLAST#
30	BREQ	65	SMI#	100	D19	135	Vss	170	Vss	205	Vcc
31	BE0#	66	FERR#	101	D18	136	Vcc	171	A17	206	PLOCK#
32	BE1#	67	NC	102	Vcc	137	Vcc	172	Vcc	207	LOCK#
33	BE2#	68	TDO	103	D17	138	Vss	173	A16	208	Vss
34	BE3#	69	Vcc	104	Vss	139	Vcc	174	A15		
35	Vcc	70	NC	105	Vss	140	D4	175	Vss		

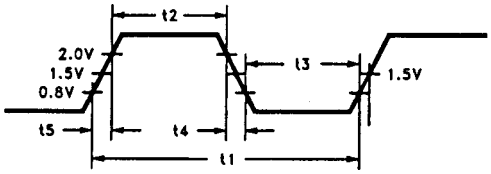


Figure 1. 80486DX2RP CLK Waveforms

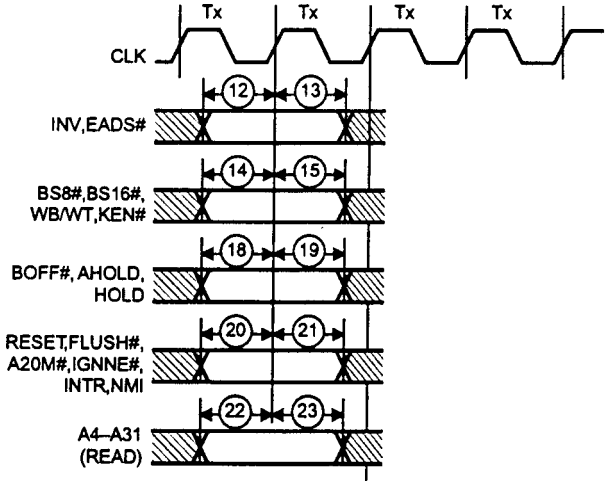


Figure 2. 80486DX2RP Input Setup and Hold Timing

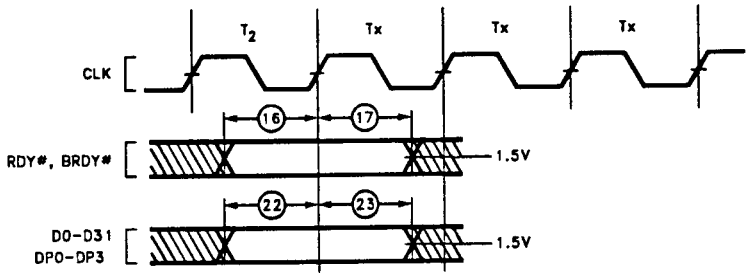


Figure 3. 80486DX2RP Input Setup and Hold Timing

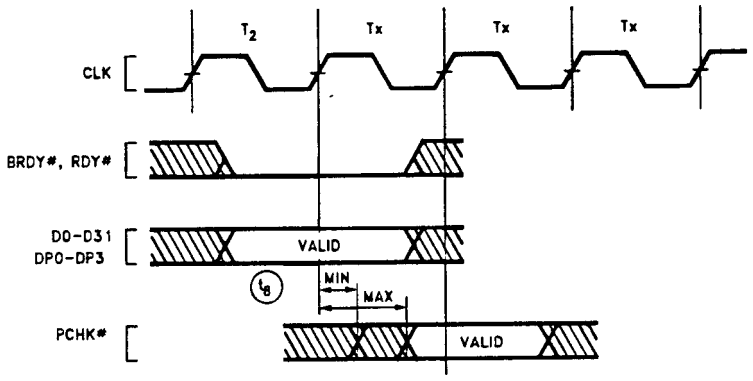


Figure 4. 80486DX2RP PCHK# Valid Delay Timing

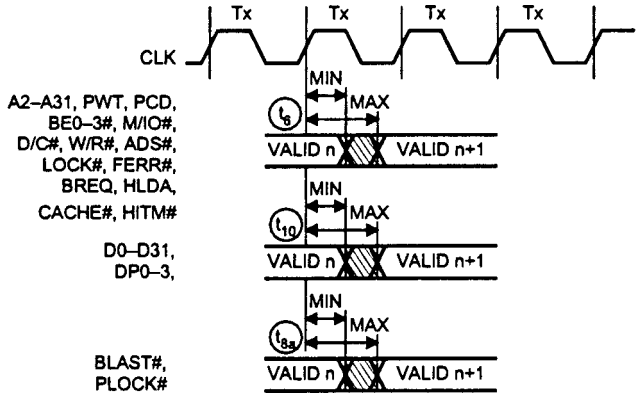


Figure 5. 80486DX2RP Output Valid Delay Timing

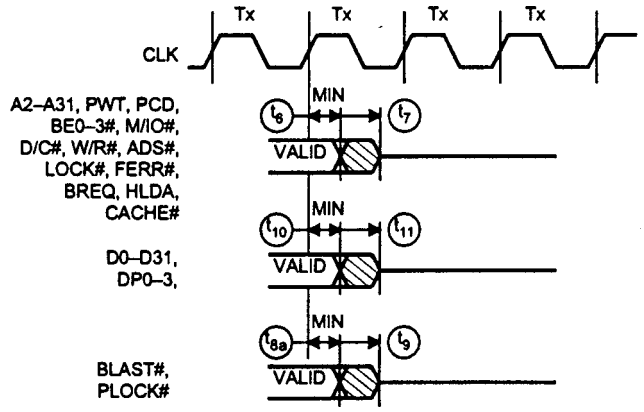


Figure 6. 80486DX2RP Maximum Float Delay Timing

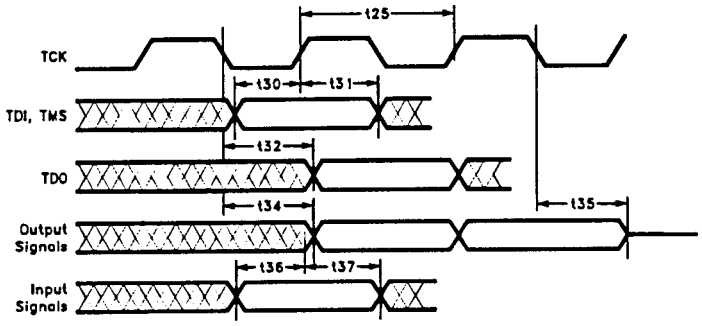
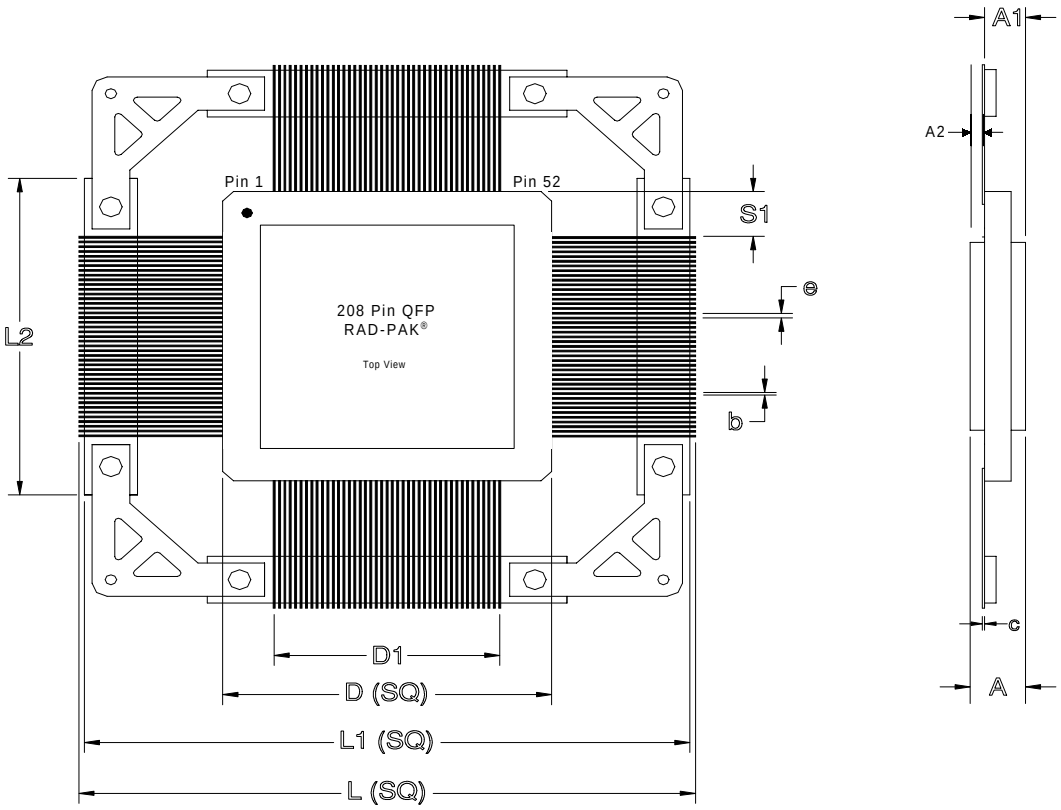


Figure 7. 80486DX2RP Test Signal Timing



Symbol	Dimension (inches)	
	Minimum	Maximum
A	.110	.150
A1	.026	-
b	.007	.013
c	.004	.009
D	1.133	1.515
D1	1.275 BSC	
S1	.013	-
e	.025 BSC	
L	2.500	2.540
L1	2.485	2.505
A1	.075	.125
N	208	

Note: This package has to be mounted cavity down to match the pinout.