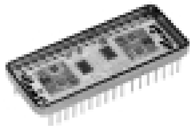
DRC-11522



TWO-CHANNEL DIGITAL-TO-RESOLVER CONVERTER

DESCRIPTION

The DRC-11522 is a dual 16-bit digital-to-resolver (D/R) converter. Each channel is independent from the other with the exception of the 16 digital lines. The DRC-11522 allows the user to program the gain of the resolver output.

Packaged in a 36-pin double DIP, the DRC-11522 is two digital-to-resolver converters in one hybrid module. Using an AC reference input, the DRC-11522 is a digital-to-resolver converter. When using a DC reference input, the unit can be used as a hybrid digital-to-sin/cos DC converter. With the reference input proportional to the radius vector, the DRC-11522 converts polar to rectangular coordinates.

The circuit design in the DRC-11522 allows for higher accuracy and reduces the output scale factor variation so that the output can drive displays directly. The output line-to-line voltage can be scaled by pin programming. Other features include buffered reference input, and a wide operating temperature range.

APPLICATIONS

Because of its high reliability, small size and low power consumption, the DRC-11522 is ideal for the most stringent and severe industrial and military ground or avionics applications. All units are available with MIL-PRF-38534 processing.

Among the many possible applications are computer-based systems in which digital information is processed, such as simulators, flight trainers, flight instrumentation, fire control systems, radar and navigation systems.

FEATURES

- *16-Bit Resolution*
- *Pin Programmable Gain Control*
- *Two Channels in One 36-Pin DDIP*
- *Accuracy: to ±2 Min.*
- *0.1% Scale Factor Variation with Angle*
- *DC-Coupled Reference*
- *High Reliability CMOS D/R Chip*
- *8-Bit/2-Byte Double-Buffered Transparent Latches*

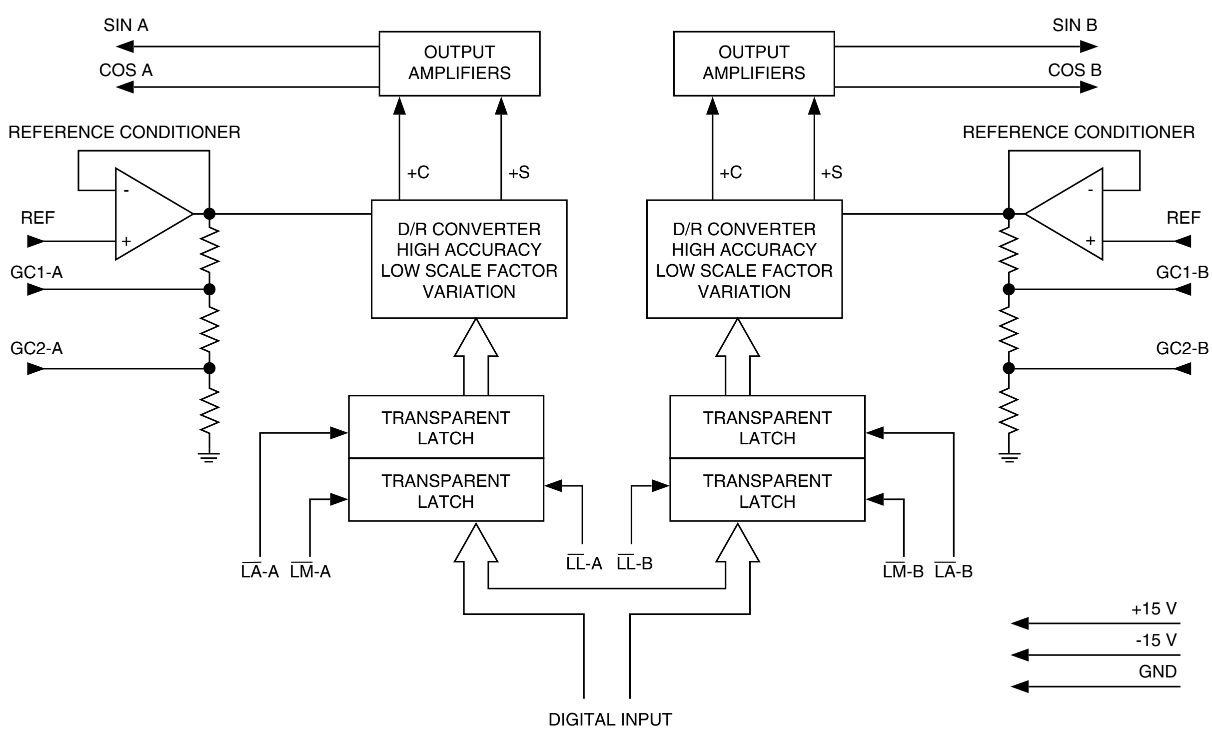


FIGURE 1. DRC-11522 BLOCK DIAGRAM

TABLE 1. SPECIFICATIONS (for each channel)

Apply over temperature range, power supply ranges, reference voltage, and frequency range, and 10% harmonic distortion in the reference.

PARAMETER	VALUE	DESCRIPTION/REMARKS
RESOLUTION	16 bits (0.33 arc minutes)	MSB = 180° LSB = 0.0055°
ACCURACY		
Output Accuracy	±8 minutes to ±1 minute (see ordering info)	Accuracy applies over operating temp. range
Differential Linearity	±1 LSB max	
Radius accuracy	±0.03%	Simultaneous amplitude variation in both outputs as a function of digital angle
DYNAMICS		
Output Settling Time	Less than 20 µsec for any digital step change.	For any analog or digital step change
DIGITAL INPUT		
Logic Type		Natural binary angle parallel positive logic CMOS and TTL compatible. Inputs are CMOS transient protected. Each input has a 20 µA max pull down to GND.
Logic “0”	-0.3 V-dc to 1.25 V-dc	External logic voltage not needed. TTL compatible.
Logic “1”	+2.0 V-dc to +5.5 V-dc	
Load Current	20 µA max to GND	Bits 1-16
	20 µA to V_L	$\overline{LL}$, $\overline{LM}$, $\overline{LA}$ (See timing Diagram, FIGURE 2)
REFERENCE INPUT		
Type		Programmable (See TABLE 2.)
Frequency Range	DC to 1000 Hz	DC to 10 kHz with reduced accuracy.
Voltage	3.5 V ±10%	0 to ±10 peak AC or DC
Input Impedance	10 M Ohm min	Operational Amplifier Buffer
ANALOG OUTPUT		
Type		Resolver
Output Current	2 mA rms max	
Max Output Voltage (Tracks Reference Input Voltage)	$K * V_{in} * \text{Sin}\ \theta$ also $K * V_{in} * \text{Cos}\ \theta$	±10 V peak AC or DC
Converter Gain (K)	0.5, 1.0, or 2.0 ±1%	See TABLE 2.
Transformation Ratio Tol.	±0.2% max	
Scale Factor Variation	±0.1% max	
DC Offset	±10 mV typical, ±25 mV max	Each Line to GND
POWER SUPPLIES		
Voltage	±15 VDC ±10%	For ±10 V peak output
Max Voltage Without Damage	±18 VDC	
Current or Impedance	±40 mA max	
TEMPERATURE RANGES (CASE)		
Operating		
-1 Option	-55°C to +125°C	
-3 Option	0°C to +70°C	
Storage	-60°C to +135°C	
PHYSICAL CHARACTERISTICS		
Type	36-pin double DIP	
Size	0.78 x 1.9 x 0.21 inch (2.0 x 4.8 x 0.53 cm)	
Weight	0.6 oz (17g) max	

TECHNICAL INFORMATION

DIGITAL INPUTS

For each channel, the 16-bit digital angle is double buffered with transparent latches (See FIGURE 1). The latch controls have internal pull-up current sources to +5 V, this puts the latches in the transparent mode when they are not connected.

Angle is determined by adding the logic bits. The enable inputs are $\overline{LL}$ (1st Latch LSBs), $\overline{LM}$ (1st Latch MSBs), and $\overline{LA}$ (2nd Latch All); see FIGURE 2 for timing.

OUTPUT SCALING AND REFERENCE LEVEL ADJUSTMENT

The DRC-11522 operates like a multiplying D/A converter in that the voltage of each output line is directly proportional to the reference voltage. The maximum line-to-line levels are determined by the output amplifiers and are programmable for a gain of 0.5, 1.0, or 2.0 (See TABLE 2.).

TABLE 2. PROGRAMMABLE GAIN

GC1-A (PIN 7)	**GC2-A** (PIN 8)	**GAIN** (K)
GND	OPEN	0.5
OPEN	GND	1.0
OPEN	OPEN	2.0
GC1-B (PIN 4)	**GC2-B** (PIN 5)	**GAIN** (K)

OUTPUT PHASING AND OUTPUT SCALE FACTOR

The analog output signals have the following phasing:

$$\sin = (REF * K)\ A_O\ [1 + A(\theta)]\ \sin\theta$$
$$\cos = (REF * K)\ A_O\ [1 + A(\theta)]\ \cos\theta$$

The output amplifiers simultaneously track reference voltage fluctuations because they are proportional to (REF * K). The transformation ratio A_O is determined by the programmable gain inputs (0.5, 1.0, or 2.0). The maximum variation in A_O from all causes is 0.1%. The term $A(\theta)$ represents the variation of the amplitude with the digital signal input angle. $A(\theta)$, which is called the scale factor variation, is a smooth function of (θ) without discontinuities and is less than ±0.1% for all values of (θ) The total maximum variation in $A_O[1 + A(\theta)]$ is therefore ±0.2%.

Because the amplitude factor (REF * K) A_O $[1 + A(\theta)]$ varies simultaneously on all output lines, it is not a source of error when the DRC-11522 is driving a ratiometric system. However, if the outputs are used independently, as in x-y plotters, the amplitude variations must be taken into account.

TABLE 3. PINOUTS

PIN	FUNCTION	PIN	FUNCTION
1	$\overline{LL}$-B	19	Bit 16 (LSB)
2	COS A	20	Bit 15
3	SIN A	21	Bit 14
4	GC1-B	22	Bit 13
5	GC2-B	23	Bit 12
6	Ref B	24	Bit 11
7	GC1-A	25	Bit 10
8	GC2-A	26	Bit 9
9	Ref A	27	Bit 8
10	COS B	28	Bit 7
11	SIN B	29	Bit 6
12	NC	30	Bit 5
13	+15 V	31	Bit 4
14	-15 V	32	Bit 3
15	$\overline{LA}$-B	33	Bit 2
16	$\overline{LA}$-A	34	Bit 1 (MSB)
17	$\overline{LL}$-A	35	$\overline{LM}$-A
18	GND	36	$\overline{LM}$-B
NOTE: Functions $\overline{LL}$, $\overline{LM}$, $\overline{LA}$ both A and B may be left unconnected when not used.			

TABLE 4. PIN DEFINITIONS

PIN	DEFINITION
GND	Power Supply Ground Digital Ground Analog Signal Ground
B1-B16	Digital Input bits B1, = MSB = 180 degrees
$\overline{LM}$-A	High Byte Enable (B1-B8) for MSB's 8-bit Input register of channel A. Logic high enables, low holds.
$\overline{LM}$-B	High Byte Enable (B1-B8) for MSB's 8-bit Input register channel B Logic high enables, low holds.
$\overline{LL}$-A	Low Byte Enable (B9-B16) for LSB's 8-bit Input register of channel A. Logic high enables, low holds
$\overline{LL}$-B	Low Byte Enable (B9-B16) for LSB's 8-bit Input register of channel B. Logic high enables, low holds.
$\overline{LA}$-A	Channel A Load Converter. Logic high transfers Channel A input registers data into 16-bit holding register. When low, Channel A is in hold mode.
$\overline{LA}$-B	Channel B Load Converter. Logic high transfers Channel B input registers data into 16-bit holding register. When low, Channel B is in hold mode.
+15 V	Power Supply Voltage.
-15 V	Power Supply Voltage. **CAUTION:** **REVERSAL OF POWER SUPPLIES WILL DAMAGE THE CONVERTER.**
Ref-A	Channel A reference voltage Input
Ref-B	Channel B reference voltage input
GC1-A	Channel A gain programming pin
GC2-A	Channel A gain programming pin
GC1-B	Channel B gain programming pin
GC2-B	Channel B gain programming pin
Sin A	Analog output of Channel A
Cos A	Analog output of Channel A
Sin B	Analog output of Channel B
Cos B	Analog output of Channel B

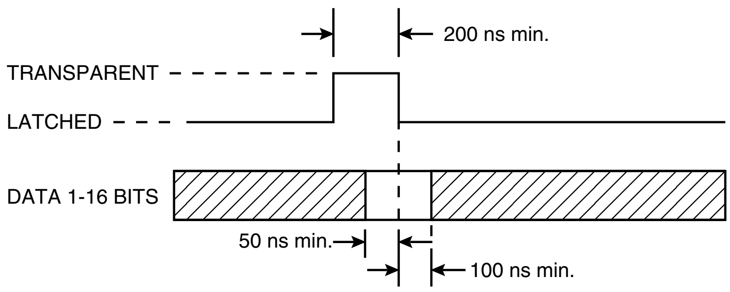
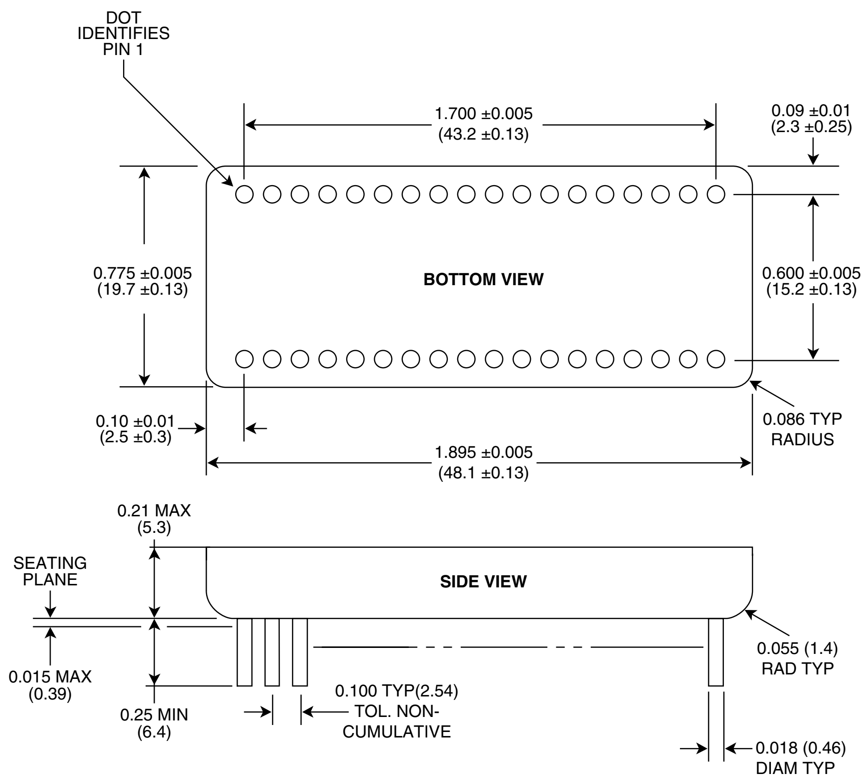


FIGURE 2. $\overline{LL}$, $\overline{LM}$, AND $\overline{LA}$ TIMING DIAGRAM



Notes:
1. Dimensions shown are in inches (millimeters)
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.010 (±2.54) of outline dimensions.
   Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Package is Kovar with electroless nickel plating.
6. Case is electrically floating.

FIGURE 3. DRC-11522 MECHANICAL OUTLINE (36-PIN DOUBLE DIP)

ORDERING INFORMATION

DRC-11522-X X X X

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- K = One Lot Date Code
- W = One Lot Date Code and PreCap Source
- Y = One Lot Date Code and 100% Pull Test
- Z = One Lot Date Code, PreCap Source and 100% Pull Test
- Blank = None of the Above

Accuracy:
- 3 = ±4 minutes
- 4 = ±2 minutes

Process Requirements:
- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

*Standard DDC Processing with burn-in and full temperature test — see table below.

STANDARD DDC PROCESSING		
TEST	MIL-STD-883	
	METHOD(S)	CONDITION(S)
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	A
BURN-IN	1015, Table 1	—

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