# MPC860 ON-CHIP ACCESS GUIDE

## 16.4 CORE CONTROL REGISTERS

The following registers are CPU and a subsection of SIU control registers implemented within the MPC860. Access to these special registers occurs via the instructions **mtspr** and **mfspr.** Special purpose registers must access memory indirectly via the general purpose registers. General purpose registers may be written as ‘rN’ or simply as ‘N.’ An assembler directive for accessing these registers is as follows:

mtspr 8, r0 /* MOVE TO THE LINK REGISTER */

mfspr 3, 638 /* MOVES FROM THE IMMR REGISTER TO REGISTER 3 */

**NOTE**

The IMMR register (special purpose register #638) setting determines the base address for all on-chip 860 modules which are not dedicated to core (CPU) operation. During HRESET, the internal base address is initially set to one of four addresses determined by the ISB field in the HARD RESET CONFIGURATION WORD. If during HRESET the RSTCONF pin is not driven low and the HARD RESET CONFIGURATION WORD is not placed on the data bus, the initial base address is $00000000. After the reset process is finished, the internal base address may be moved to any value by writing to the IMMR register. I

**Table 16-3. Standard Special Purpose Registers (Sheet 1 of 2)**

| SPR | | | NAME | DESCRIPTION | CROSS REF. |
|---|---|---|---|---|---|
| DECIMAL | spr 5:9 | spr 0:4 | | | UM SECTION |
| 1 | 00000 | 00001 | XER | Fixd Pt Exception Cause | 2.4.2.2 |
| 8 | 00000 | 01000 | LR | Link Register | 2 |
| 9 | 00000 | 01001 | CTR | Count Register | 2 |
| 18 | 00000 | 10010 | DSISR | Data Storage Int. Status | 2 |
| 19 | 00000 | 10011 | DAR | Data Address Register | 2.6.15, 8 |
| 22 | 00000 | 10110 | DEC | Decrementer | 9 |
| 26 | 00000 | 11010 | SRR0 | Machine Status Save/Rest | 2, 3.3.8 |
| 27 | 00000 | 11011 | SRR1 | Machine Status Save/Rest | 2, 3.3.8 |
| 272 | 01000 | 10000 | SPRG0 | Address of except. handler | |

## Table 16-3. Standard Special Purpose Registers (Sheet 2 of 2)

| SPR | | | NAME | DESCRIPTION | CROSS REF. |
|---|---|---|---|---|---|
| DECIMAL | spr 5:9 | spr 0:4 | | | UM SECTION |
| 273 | 01000 | 10001 | SPRG1 | Exception Handler Scratch | |
| 274 | 01000 | 10010 | SPRG2 | Scratch Register 2 | |
| 275 | 01000 | 10011 | SPRG3 | Scratch Register 3 | |
| 287 | 01000 | 11111 | PVR | Processor Version | 3.3.2 |

## Table 16-4. Standard Time Base Register mapping* (See Note *)

| SPR | | | NAME | DESCRIPTION | CROSS REF |
|---|---|---|---|---|---|
| DECIMAL | spr 5:9 | spr 0:4 | | | UM SECTION |
| 268 | 01000 | 01100 | TB read (See Note 2.) | Read Lower Time Base | 9.13 |
| 269 | 01000 | 01101 | TBU read (See Note 2.) | Read Upper Time Base | 9.13 |
| 284 | 01000 | 11100 | TB write (See Note 3.) | Write Lower Time Base | 9.13 |
| 285 | 01000 | 11101 | TBU write (See Note 3.) | Write Upper Time Base | 9.13 |

* 1. Extended opcode for **mftb**, 371 rather then 339

2. Any write (**mtspr**) to this address, results in an Implementation Dependent Software Emulation interrupt

3. Any read (**mftb**) to this address, results in an Implementation Dependent Software Emulation interrupt

## Table 16-5. Added Special Purpose Registers (Sheet 1 of 4)

| SPR | | | NAME | DESCRIPTION | CROSS REF |
|---|---|---|---|---|---|
| DECIMAL | spr 5:9 | spr 0:4 | | | UM SECTION |
| 80 | 00010 | 10000 | EIE * (See Note 1.) | External Interrupt Enable | 2.3 |
| 81 | 00010 | 10001 | EID | External Interrupt Disable | 2.3 |
| 82 | 00010 | 10010 | NRI | Non Recoverable Int. | 2.3 |
| 144 | 00100 | 10000 | CMPA (See Note 2.) | Compare A Value (See Note 3.) | 5 |
| 145 | 00100 | 10001 | CMPB | Compare B Value | 5 |
| 146 | 00100 | 10010 | CMPC | Compare C Value | 5 |
| 147 | 00100 | 10011 | CMPD | Compare D Value | 5 |
| 148 | 00100 | 10100 | ICR | Interrupt Cause | 5 |
| 149 | 00100 | 10101 | DER | Debug Enable | 5 |

## Table 16-5. Added Special Purpose Registers (Sheet 2 of 4)

| SPR | | | NAME | DESCRIPTION | CROSS REF |
|---|---|---|---|---|---|
| DECIMAL | spr 5:9 | spr 0:4 | | | UM SECTION |
| 150 | 00100 | 10110 | COUNTA | Instr/Load Watchpt Count | 5 |
| 151 | 00100 | 10111 | COUNTB | Instr/Load Watchpt Count | 5 |
| 152 | 00100 | 11000 | CMPE | Compare E Value | 5 |
| 153 | 00100 | 11001 | CMPF | Compare F Value | 5 |
| 154 | 00100 | 11010 | CMPG | Compare G Value | 5 |
| 155 | 00100 | 11011 | CMPH | Compare H Value | 5 |
| 156 | 00100 | 11100 | LCTRL1 | Load/Store Compare Cntl | 5 |
| 157 | 00100 | 11101 | LCTRL2 | Load/Store AND-OR | 5 |
| 158 | 00100 | 11110 | ICTRL | Instr. Support Cntl | 5 |
| 159 | 00100 | 11111 | BAR | Breakpt Address | 2.6.15, 5 |
| 630 | 10011 | 10110 | DPDR | Develop. Port Data | 5 |
| 631 | 10011 | 10111 | DPIR (See Note 4.) | Develop. Port Instr. | 5 |
| 638 | 10011 | 11110 | IMMR | Internal Memory Map | 9, 16 |

## Table 16-5. Added Special Purpose Registers (Sheet 3 of 4)

| SPR | | | NAME | DESCRIPTION | CROSS REF |
|---|---|---|---|---|---|
| DECIMAL | spr 5:9 | spr 0:4 | | | UM SECTION |
| 560 | 10001 | 10000 | IC_CST | Instr. Cache Cntl/Stat | 6 |
| 561 | 10001 | 10001 | IC_ADR | Instr. Cache Address | 6 |
| 562 | 10001 | 10010 | IC_DAT | Instr. Cache Data | 6 |
| 568 | 10001 | 11000 | DC_CST | Data Cache Cntl/Stat | 7 |
| 569 | 10001 | 11001 | DC_ADR | Data Cache Address | 7 |
| 570 | 10001 | 11010 | DC_DAT | Data Cache Data | 7 |
| 784 | 11000 | 10000 | MI_CTR | Instruction MMU Cntl | 8 |
| 786 | 11000 | 10010 | MI_AP | Instr. MMU Access Perm. | 8 |
| 787 | 11000 | 10011 | MI_EPN | Instr. MMU Effect. Pg Num | 8 |
| 789 | 11000 | 10101 | MI_TWC (MI_L1DL2P) | Instr. MMU Tblewalk Cntl | 8 |
| 790 | 11000 | 10110 | MI_RPN | Instr. MMU Real Pg Num | 8 |

**Table 16-5. Added Special Purpose Registers (Sheet 4 of 4)**

| SPR | | | NAME | DESCRIPTION | CROSS REF |
|---|---|---|---|---|---|
| DECIMAL | spr 5:9 | spr 0:4 | | | UM SECTION |
| 816 | 11001 | 10000 | MI_DBCAM | Data MMU CAM Read | 8 |
| 817 | 11001 | 10001 | MI_DBRAM0 | Data MMU CAM Read 0 | 8 |
| 818 | 11001 | 10010 | MI_DBRAM1 | Data MMU CAM Read 1 | 8 |
| 792 | 11000 | 11000 | MD_CTR | Data MMU Cntl | 8 |
| 793 | 11000 | 11001 | M_CASID | CASID | 8 |
| 794 | 11000 | 11010 | MD_AP | Data MMU Access Priv | 8 |
| 795 | 11000 | 11011 | MD_EPN | Data MMU Eff. Page Num | 8 |
| 796 | 11000 | 11100 | M_TWB (MD_L1P) | MMU TableWalk Base | 8 |
| 797 | 11000 | 11101 | MD_TWC (MD_L1DL2P) | Data MMU TbleWalk Cntl | 8 |
| 798 | 11000 | 11110 | MD_RPN | Data MMU Real Pg Num | 8 |
| 799 | 11000 | 11111 | M_TW (M_SAVE) | MMU TableWalk Special | 8 |
| 824 | 11001 | 11000 | MD_DBCAM | Data MMU CAM Read | 8 |
| 825 | 11001 | 11001 | MD_DBRAM0 | Data MMU CAM Read0 | 8 |
| 826 | 11001 | 11010 | MD_DBRAM1 | Data MMU CAM Read1 | 8 |

*

1. Refer to 2.3.5.1 “Restartability after an interrupt” on page 20.

2. Refer to 5.5.1 “Development support registers list” on page 119.

3. Protection of Registers designated with “debug” privilege is described in 5.5.2 “Development support registers protection” on page 120.

4. This register is a *fetch only register*, using **mtspr** is ignored using mfspr gives undefined value. Refer to 5.3 “Development system interface” on page 95.

**Table 16-6. Other control Registers**

| DESCRIPTION | NAME | CROSS REF |
|---|---|---|
| Machine State register | MSR | 2.4.2.2 |
| Condition Register | CR | 2.4.2.2 |

## 16.5 INTERNALLY MAPPED REGISTERS

The MPC860 internal memory resources are mapped within a contiguous block of storage. The size of the internal space in the MPC860 is 16Kbytes. The location of this block within

the global 4 Giga-byte real storage space can be mapped on a 64Kbytes resolution through an implementation specific special register, the Internal Memory Map Register (IMMR). The following table defines the internal memory map of the MPC860.

To address the registers below, the number in the column labeled “Internal Address” is added as an offset to the IMMR register (special purpose register number 638).

For example, if the most significant bits of special purpose register 638 (the IMMR) are set to $FF00, then to initialize the SDMA Configuration Register (SDCR) one would write to location $FF000030. To access the dual port RAM, one would address locations $FF002000 through $FF004000.



**Table 16-7. MPC860 internal memory map (Sheet 1 of 13)**

| Internal Address | Mnemonic | Name | Size |
|---|---|---|---|
| GENERAL SIU - SEE SECTION 9 | | | |
| 000 | SIUMCR | SIU Module configuration | 32 |
| 004 | SYPCR | System Protection Control | 32 |
| 008 | SWT | SW watch dog timer Current Value | 32 |
| 00E | SWSR | Software service | 16 |
| 010 | SIPEND | Interrupt Pend Register | 32 |
| 014 | SIMASK | Interrupt Mask | 32 |
| 018 | SIEL | Interrupt Edge Level mask | 32 |
| 01C | SIVEC | Interrupt Vector | 32 |
| 020 | TESR | Transfer Error status | 32 |
| 024 TO 02F | Reserved | | |
| 030 | SDCR | SDMA Configuration Register | 32 |
| 034 TO 07F | Reserved | | |
| PCMCIA - SEE SECTION 12 | | | |
| 080 | PBR0 | PCMCIA Base | 32 |
| 084 | POR0 | PCMCIA Option | 32 |

**Table 16-7. MPC860 internal memory map (Sheet 2 of 13)**

| Internal Address | Mnemonic | Name | Size |
|---|---|---|---|
| 088 | PBR1 | PCMCIA Base | 32 |
| 08C | POR1 | PCMCIA Option | 32 |
| 090 | PBR2 | PCMCIA Base | 32 |
| 094 | POR2 | PCMCIA Option | 32 |
| 098 | PBR3 | PCMCIA Base | 32 |
| 09C | POR3 | PCMCIA Option | 32 |
| 0A0 | PBR4 | PCMCIA Base | 32 |
| 0A4 | POR4 | PCMCIA Option | 32 |
| 0A8 | PBR5 | PCMCIA Base | 32 |
| 0AC | POR5 | PCMCIA Option | 32 |
| 0B0 | PBR6 | PCMCIA Base | 32 |
| 0B4 | POR6 | PCMCIA Option | 32 |
| 0B8 | PBR7 | PCMCIA Base | 32 |
| 0BC | POR7 | PCMCIA Option | 32 |
| 0C0 TO 0DF | Reserved | | |
| 0E0 | PGCRA | PCMCIA slot A control | 32 |
| 0E4 | PGCRB | PCMCIA slot B control | 32 |
| 0E8 | PSCR | PCMCIA Status | 32 |
| 0EC TO 0EF | Reserved | | |
| 0F0 | PIPR | PCMCIA pins value | 32 |
| 0F4 TO 0F7 | Reserved | | |
| 0F8 | PER | PCMCIA Enable | 32 |

## Table 16-7. MPC860 internal memory map (Sheet 3 of 13)

| Internal Address | Mnemonic | Name | Size |
|---|---|---|---|
| 0FC TO 0FF | Reserved | | |
| MEMC - SEE SECTION 12 | | | |
| 100 | BR0 | Base Regster | 32 |
| 104 | OR0 | Option Register | 32 |
| 108 | BR1 | Base Regster | 32 |
| 10C | OR1 | Option Register | 32 |
| 110 | BR2 | Base Regster | 32 |
| 114 | OR2 | Option Register | 32 |
| 118 | BR3 | Base Regster | 32 |
| 11C | OR3 | Option Register | 32 |
| 120 | BR4 | Base Regster | 32 |
| 124 | OR4 | Option Register | 32 |
| 128 | BR5 | Base Regster | 32 |
| 12C | OR5 | Option Register | 32 |
| 130 | BR6 | Base Regster | 32 |
| 134 | OR6 | Option Register | 32 |
| 138 | BR7 | Base Regster | 32 |
| 13C | OR7 | Option Register | 32 |
| 140 TO 163 | Reserved | | |
| 164 | MAR | Memory Address | 32 |
| 168 | MCR | Memory Command | 32 |
| 16C TO 16F | Reserved | | 32 |
| 170 | MAMR | Machine A Mode | 32 |

**Table 16-7. MPC860 internal memory map (Sheet 4 of 13)**

| Internal Address | Mnemonic | Name | Size |
|---|---|---|---|
| 174 | MBMR | Machine B Mode | 32 |
| 178 | MSTAT | Memory Status | 16 |
| 17A | MPTPR | Memory Periodic Timer Prescaler | 16 |
| 17C | MDR | Memory Data | 32 |
| 180 TO 1FF | Reserved | | |
| SYSTEM INTEGRATION TIMERS - SEE SECTION 9 | | | |
| 200 | TBSCR | Time base Status and Control | 16 |
| 204 | TBREFF0 | Time Base Reference 0 | 32 |
| 208 | TBREFF1 | Time Base Reference 1 | 32 |
| 20C TO 21F | Reserved | | |
| 220 | RTCSC | Real Time Clock Status and Control | 16 |
| 224 | RTC | Real Time Clock | 32 |
| 228 | RTSEC | Real Time AlarmSeconds | 32 |
| 22C | RTCAL | Real Time Alarm | 32 |
| 230 TO 23F | Reserved | | 8x32 |
| 240 | PISCR | PIT Status and Control | 16 |
| 244 | PITC | PIT Count | 32 |
| 248 | PITR | PIT | 32 |
| 24C TO 27F | Reserved | | |
| CLOCKS AND RESET - SEE SECTION 16 | | | |
| 280 | SCCR | System Clock Control | 32 |
| 284 | PLPRCR | PLL, Low power and Reset Control Register | 32 |

**Table 16-7. MPC860 internal memory map (Sheet 5 of 13)**

| Internal Address | Mnemonic | Name | Size |
|---|---|---|---|
| 288 | RSR | Reset Status Register | 32 |
| 28C TO 2FF | Reserved | | |
| SYSTEM INTEGRATION TIMERS KEYS - SEE SECTION 9 | | | |
| 300 | TBSCRK | Time base Status and Control Key | 32 |
| 304 | TBREFF0K | Time Base Reference 0 Key | 32 |
| 308 | TBREFF1K | Time Base Reference 1 Key | 32 |
| 30C | TBK | Time Base and Decrementer Key | 32 |
| 310 TO 31F | Reserved | | |
| 320 | RTCSCK | Real Time Clock Status and Control Key | 32 |
| 324 | RTCK | Real Time Clock Key | 32 |
| 328 | RTSECK | Real Time AlarmSeconds Key | 32 |
| 32C | RTCALK | Real Time Alarm Key | 32 |
| 330 TO 33F | Reserved | | 8x32 |
| 340 | PISCRK | PIT Status and Control Key | 32 |
| 344 | PITCK | PIT Count Key | 32 |
| 348 TO 37F | Reserved | | |
| CLOCKS AND RESET KEYS - SEE SECTION 16 | | | |
| 380 | SCCRK | System Clock Control Key | 32 |
| 384 | PLPRCRK | PLL, Low power and Reset Control Register Key | 32 |
| 388 | RSRK | Reset Status Register Key | 32 |
| 38C TO 3FF | Reserved | | |

**Table 16-7. MPC860 internal memory map (Sheet 6 of 13)**

| Internal Address | Mnemonic | Name | Size |
|---|---|---|---|
| 400 TO 7FF | Reserved | | |
| 800 TO 85F | Reserved | | |
| I2C - SEE SECTION 13.17 | | | |
| 860 | I2MOD | I2C Mode Register | 8 |
| 864 | I2ADD | I2C Address Register | 8 |
| 868 | I2BRG | I2C BRG Register | 8 |
| 86C | I2COM | I2C Command Register | 8 |
| 870 | I2CER | I2C Event Register | 8 |
| 874 | I2CMR | I2C Mask Register | 8 |
| DMA SEE SECTION 13.10 | | | |
| 900 -903 | Reserved | | |
| 904 | SDAR | SDMA Address Register | 32 |
| 908 | SDSR | SDMA Status Register | 8 |
| 909-90B | Reserved | | 3 x 8 |
| 90C | SDMR | SDMA Mask Register | 8 |
| 90D-90F | Reserved | | 3 x 8 |
| 910 | IDSR1 | IDMA1 Status Register | 8 |
| 911-913 | Reserved | | 3 x 8 |
| 914 | IDMR1 | IDMA1 Mask Register | 8 |
| 915-917 | Reserved | | 3 x 8 |
| 918 | IDSR2 | IDMA2 Status Register | 8 |
| 919-91B | Reserved | | 3 x 8 |
| 91C | IDMR2 | IDMA2 Mask Register | 8 |
| 91D-92F | Reserved | | |
| CPM INTERRUPT CONTROL - SEE SECTION 13.20 | | | |

**Table 16-7. MPC860 internal memory map (Sheet 7 of 13)**

| Internal Address | Mnemonic | Name | Size |
|---|---|---|---|
| 930 | CIVR | CP Interrupt vector register | 16 |
| 932 TO 93F | Reserved | | |
| 940 | CICR | CP Interrupt Configuration Register | 32 |
| 944 | CIPR | CP Interrupt Pending Register | 32 |
| 948 | CIMR | CP Interrupt Mask Register | 32 |
| 94C | CISR | CP In-Service Register | 32 |
| INPUT/OUTPUT PORT - SEE SECTION 13.19 | | | |
| 950 | PADIR | Port A Data Direction Register | 16 |
| 952 | PAPAR | Port A Pin Assignment Register | 16 |
| 954 | PAODR | Port A Open Drain Register | 16 |
| 956 | PADAT | Port A Data Register | 16 |
| 958 TO 95F | Reserved | | |
| 960 | PCDIR | Port C Data Direction Register | 16 |
| 962 | PCPAR | Port C Pin Assignment Register | 16 |
| 964 | PCSO | Port C Special Options | 16 |
| 966 | PCDAT | Port C Data Register | 16 |
| 968 | PCINT | Port C Interrupt Control Register | 16 |
| 96A TO 96F | Reserved | | |
| 970 | PDDIR | Port D Data Direction Register | 16 |
| 972 | PDPAR | Port D Pin Assignment Register | 16 |
| 974 | Reserved | Reserved | 16 |
| 976 | PDDAT | Port D Data Register | 16 |

**Table 16-7. MPC860 internal memory map (Sheet 8 of 13)**

| Internal Address | Mnemonic | Name | Size |
|---|---|---|---|
| 978 TO 97F | Reserved | | |
| CPM TIMERS - SEE SECTION 13.7 | | | |
| 980 | TGCR | Timer Global Configuration Register | 16 |
| 982 TO 98F | Reserved | | |
| 990 | TMR1 | Timer1 Mode Register | 16 |
| 992 | TMR2 | Timer2 Mode Register | 16 |
| 994 | TRR1 | Timer1 Reference Register | 16 |
| 996 | TRR2 | Timer2 Reference Register | 16 |
| 998 | TCR1 | Timer1 Capture Register | 16 |
| 99A | TCR2 | Timer2 Capture Register | 16 |
| 99C | TCN1 | Timer1 Counter | 16 |
| 99E | TCN2 | Timer2 Counter | 16 |
| 9A0 | TMR3 | Timer3 Mode Register | 16 |
| 9A2 | TMR4 | Timer4 Mode Register | 16 |
| 9A4 | TRR3 | Timer3 Reference Register | 16 |
| 9A6 | TRR4 | Timer4 Reference Register | 16 |
| 9A8 | TCR3 | Timer3 Capture Register | 16 |
| 9AA | TCR4 | Timer4 Capture Register | 16 |
| 9AC | TCN3 | Timer3 Counter | 16 |
| 9AE | TCN4 | Timer4 Counter | 16 |
| 9B0 | TER1 | Timer1 Event Register | 16 |
| 9B2 | TER2 | Timer2 Event Register | 16 |
| 9B4 | TER3 | Timer3 Event Register | 16 |
| 9B6 | TER4 | Timer4 Event Register | 16 |

**Table 16-7. MPC860 internal memory map (Sheet 9 of 13)**

| Internal Address | Mnemonic | Name | Size |
|---|---|---|---|
| 9B8 TO 9BF | Reserved | | |
| COMMUNICATION PROCESSOR - SEE SECTION 13.4-13.5 | | | |
| 9CO | CPCR | Communication Processor Command Register | 16 |
| 9C4 | RCCR | RISC Configuration Register | 16 |
| 9C6 | RES | Reserved | 8 |
| 9C7 | RES | Reserved | 8 |
| 9C8 | RES | Reserved | 32 |
| 9CC | CPMCR1 | Comm. Processor Module Control Register1 | 16 |
| 9CE | CPMCR2 | Comm. Processor Module Control Register 2 | 16 |
| 9D0 | CPMCR3 | Comm. Processor Module Control Registerr 3 | 16 |
| 9D2 | CPMCR4 | Comm. Processor Module Control Register 4 | 16 |
| 9D6 | RTER | RISC Timers Event Register | 16 |
| 9DA | RTMR | RISC Timers Mask Register | 16 |
| 9DC TO 9EF | Reserved | | |
| BRGS - SEE SECTION 13.13 | | | |
| 9F0 | BRGC1 | BRG1 Configuration Register | 32 |
| 9F4 | BRGC2 | BRG2 Configuration Register | 32 |
| 9F8 | BRGC3 | BRG3 Configuration Register | 32 |
| 9FC | BRGC4 | BRG4 Configuration Register | 32 |
| SCC1 - SEE SECTION 13.14 | | | |
| A00 | GSMR_L1 | SCC1 General mode register | 32 |
| A04 | GSMR_H1 | SCC1 General mode register | 32 |
| A08 | PSMR1 | SCC1 Protocol Specific Mode Register | 16 |
| A0C | TODR1 | SCC1 Transmit on demand | 16 |
| A0E | DSR1 | SCC1 Data Sync. Register | 16 |

**Table 16-7. MPC860 internal memory map (Sheet 10 of 13)**

| Internal Address | Mnemonic | Name | Size |
|---|---|---|---|
| A10 | SCCE1 | SCC1 Event Register | 16 |
| A14 | SCCM1 | SCC1 Mask Register | 16 |
| A17 | SCCS1 | SCC1 Status Register | 8 |
| A18 TO A1F | Reserved | | |
| SCC2 - SEE SECTION 13.14 | | | |
| A20 | GSMR_L2 | SCC2 General mode register | 32 |
| A24 | GSMR_H2 | SCC2 General mode register | 32 |
| A28 | PSMR2 | SCC2 Protocol Specific Mode Register | 16 |
| A2C | TODR2 | SCC2 Transmit on Demand | 16 |
| A2E | DSR2 | SCC2 Data Sync. Register | 16 |
| A30 | SCCE2 | SCC2 Event Register | 16 |
| A34 | SCCM2 | SCC2 Mask Register | 16 |
| A37 | SCCS2 | SCC2 Status Register | 8 |
| A38 TO A3F | Reserved | | |
| SCC3 - SEE SECTION 13.14 | | | |
| A40 | GSMR_L3 | SCC3 General mode register | 32 |
| A44 | GSMR_H3 | SCC3 General mode register | 32 |
| A48 | PSMR3 | SCC3 Protocol Specific Mode Register | 16 |
| A4C | TODR3 | SCC3 Transmit on Demand | 16 |
| A4E | DSR3 | SCC3 Data Sync. Register | 16 |
| A50 | SCCE3 | SCC3 Event Register | 16 |
| A54 | SCCM3 | SCC3 Mask Register | 16 |
| A57 | SCCS3 | SCC3 Status Register | 8 |

**Table 16-7. MPC860 internal memory map (Sheet 11 of 13)**

| Internal Address | Mnemonic | Name | Size |
|---|---|---|---|
| A58 TO A5F | Reserved | | |
| SCC4 - SEE SECTION 13.14 | | | |
| A60 | GSMR_L4 | SCC4 General mode register | 32 |
| A64 | GSMR_H4 | SCC4 General mode register | 32 |
| A68 | PSMR4 | SCC4 Protocol Specific Mode Register | 16 |
| A6C | TODR4 | SCC4 Transmit on Demand | 16 |
| A6E | DSR4 | SCC4 Data Sync. Register | 16 |
| A70 | SCCE4 | SCC4 Event Register | 16 |
| A74 | SCCM4 | SCC4 Mask Register | 16 |
| A77 | SCCS4 | SCC4 Status Register | 8 |
| A78 TO A81 | Reserved | | |
| SMC1- SEE SECTION 13.15 | | | |
| A82 | SMCMR1 | SMC1 Mode Register | 16 |
| A86 | SMCE1 | SMC1 Event Register | 8 |
| A8A | SMCM1 | SMC1 Mask Register | 8 |
| A8C | Reserved | | |
| SMC2 - SEE SECTION 13.15 | | | |
| A92 | SMCMR2 | SMC2 Mode Register | 16 |
| A96 | SMCE2 | SMC2 or PIP Event Register | 8 |
| A9A | SMCM2 | SMC2 Mask Register | 8 |
| A9C | Reserved | | |
| SPI - SEE SECTION 13.16 | | | |
| AA0 | SPMODE | SPI Mode Register | 16 |
| AA6 | SPIE | SPI Event Register | 8 |
| AAA | SPIM | SPI Mask Register | 8 |

**Table 16-7. MPC860 internal memory map (Sheet 12 of 13)**

| Internal Address | Mnemonic | Name | Size |
|---|---|---|---|
| AAD | SPCOM | SPI Command Register | 8 |
| PIP - SEE SECTION 13.18 | | | |
| AB2 | PIPC | PIP Configuration Register | 16 |
| AB6 | PTPR | PIP Timing Parameters Register | 16 |
| AB8 | PBDIR | Port B Data Direction Register | 32 |
| ABC | PBPAR | Port B Pin Assignment Register | 32 |
| AC2 | PBODR | Port B Open Drain Register | 16 |
| AC4 | PBDAT | Port B Data Register | 32 |
| AC8 TO ADF | Reserved | | |
| SI - SEE SECTION 13.12 | | | |
| AE0 | SIMODE | SI Mode Register | 32 |
| AE4 | SIGMR | SI Global Mode Register | 8 |
| AE6 | SISTR | SI Status register | 8 |
| AE7 | SICMR | SI Command Register | 8 |
| AE8 | RES | Reserved | 32 |
| AEC | SICR | SI Clock Route | 32 |
| AF0 | SIRP | SI RAM Pointers | 32 |
| AF4 TO BFF | Reserved | | |
| C00 TO DFF | SIRAM | SI Routing RAM | 512 bytes |
| E00 TO FFF | RESERVED | | |
| 1000 TO 2000 | Reserved | | |

**Table 16-7. MPC860 internal memory map (Sheet 13 of 13)**

| Internal Address | Mnemonic | Name | Size |
|---|---|---|---|
| 2000 TO 4000 | DPRAM | | |

## 16.6 PARAMETER RAM ADDRESSING

To address protocol specific areas within the Parameter RAM, the offset listed in table 16-8 below would be added to the base location of the Dual Port RAM. Assume that the 15 most significant bits of the IMMR register areset to $FF00. The Dual port RAM base address is therefore located at $FF002000. The base address of SCC1's protocol specific registers would begin at $FF003C00. Likewise, SCC2 protocol specific registers would begin at $FF003D00. To initialize the UART parameter MAX_IDL (maximum number of idle characters) for SCC1, one would write to location $FF003C38 *(refer to the UART MEMORY MAP in Section 13.14)*

**Table 16-8. Parameter RAM Locations**

| Page | Addreses | Peripheral |
|---|---|---|
| 1 | DPRAM_Base+ $1c00 | SCC1 |
| | DPRAM_Base+ $1c7f | |
| | DPRAM_Base+ $1c80 | $I^2C$ |
| | DPRAM_Base+ $1caf | |
| | DPRAM_Base+ $1cb0 | MISC |
| | DPRAM_Base+ $1cbf | |
| | DPRAM_Base+ $1cc0 | IDMA1 |
| | DPRAM_Base+ $1cff | |
| 2 | DPRAM_Base+ $1d00 | SCC2 |
| | DPRAM_Base+ $1d7f | |
| | DPRAM_Base+ $1d80 | SPI |
| | DPRAM_Base+ $1daf | |
| | DPRAM_Base+ $1db0 | Timers |
| | DPRAM_Base+ $1dbf | |
| | DPRAM_Base+ $1dc0 | IDMA2 |
| | DPRAM_Base+ $1dff | |
| 3 | DPRAM_Base+ $1e00 | SCC3 |
| | DPRAM_Base+ $1e7f | |
| | DPRAM_Base+ $1e80 | SMC1 |
| | DPRAM_Base+ $1ebf | |
| | DPRAM_Base+ $1ec0 | DSP1 |
| | DPRAM_Base+ $1eff | |
| 4 | DPRAM_Base+ $1f00 | SCC4 |
| | DPRAM_Base+ $1f7f | |
| | DPRAM_Base+ $1f80 | SMC2 |
| | DPRAM_Base+ $1fbf | |
| | DPRAM_Base+ $1fc0 | DSP2 |
| | DPRAM_Base+ $1fff | |

## 16.6.1 UPM RAM Locations

To access the UPM RAM entries, first write the MDR register with a UPM word. This UPM word is the pattern that controls a single clock cycle of an external memory access. The MDR is at address IMMR+$17C. For a burst read cycle, a valid UPM pattern is $0x0fffcc24. An example of a write to this location is (assuming r3 = $0FFFCC24)

mtspr (638)$17C, r3

| BITS | MNEMONIC | DESCRIPTION | FUNCTION |
|---|---|---|---|
| 0-31 | MD(0:31) | **MEMORY DATA**.This is the Data to be written into the RAM array when a WRITE command is supplied to the MCR. This is the Data read from the array when a READ command is supplied to the MCR. | |

Next, the MAR register should be written with the cycle-type offset within the UPM RAM.

For example, if setting up the first cycle of a burst read, the user should write to location IMMR+$168 (MCR) being sure that bits 0:1 are equal to $00, and that bits 26-31 are equal to $08.

MCR Register

| | | | |
|---|---|---|---|
| 0-1 | OP(0:1) | **COMMAND OPCODE**. This field determines which command will be executed by the machine specified in the UM field. | 00 = WRITE. Write the contents of the MDR into the RAM location pointed by MAD in the UPM specified in UM.<br>01 = READ. Read the contents of the RAM location pointed by MAD in the UPM specified in UM into the MDR.<br>10 = RUN. Run the pattern written in the RAM array of the UPM specified in UM servicing the memory bank specified in MB. The pattern run will start at the location pointed by MAD and will continue until the LAST bit in the RAM is set.<br>11 = Reserved |

BITS 2:25 not relevant in this reference discussion

| | | | |
|---|---|---|---|
| 26-31 | MAD(0:5) | **MACHINE ADDRESS.** This field is the RAM address pointer of the command executed. | |