SME5410MCZ-270

July 1998

UltraSPARC™-II*i* CPU Module

DATA SHEET — 270 MHz CPU, 256 Kbyte E-cache, UPA, 66 MHz PCI

DESCRIPTION

The UltraSPARC™-II*i* CPU module (SME5410MCZ-270) is a high performance, SPARC™ V9-compliant, small form-factor CPU module. It interfaces to the UltraSPARC Port Architecture 64S (UPA64S) interconnect bus, main memory, and the primary PCI bus.

The module consists of one UltraSPARC™-II*i* microprocessor, one 32K x 36 tag SRAM, two 32K x 36 data SRAMs, and circuitry for generating the processor, UPA64S clocks. PCI clocks are generated externally.

Components on the module operate at nominal voltages of 3.3V and 2.6V. All signal levels to and from the module are 3.3V LVTTL compatible, with the exception of the following: both the differential UPA clock outputs, which operate at 3.3V, PECL; and the PCI interface signals, which are 3.3V PCI compatible.

The module runs at 270 MHz internal processor frequency. Clock synthesizer and division circuitry on the module set the UPA frequency to one third of the internal processor frequency. The module interface is implemented using two high-speed, controlled-impedance connectors, see the "Module Block Diagram" on page 2.

Features

- High performance UltraSPARC™-II*i* CPU module
- Programmable bus speed
- SPARC™ V9 compliant
- Implements VIS Instruction Set (VIS™)
- 64-bit wide data bus
- 0.5 Mbyte E-cache clocked at 150 MHz
- Operates at 3.3V and 2.6V LVTTL
- 66 MHz PCI bus to rev. 2.1 PCI specification
- 130 mm x 100 mm form factor
- JTAG (IEEE 1149) boundary-scan interface
- System interface through two impedance-controlled connectors

Benefits

- 8.5 SPECint95 (est.), 10.1 SPECfp95 (est.) at 270 MHz
- Provides the flexibility for using the CPU at different bus speeds
- Run applications that conform to the SPARC™ V9 ABI
- Comprehensive hardware support for 3D graphics, H-261 compression/decompression, and MPEG2 decompression
- Peak bandwidth of up to 1.2 Gbyte
- UltraSPARC™-II*i* CPU module pipelined E-cache interface delivers high performance
- Very high bus speeds and power savings, thus reducing the heat generated
- Integrated interface simplifies PCI system design
- Small footprint, modular manufacturing
- Board-level testability
- High performance impedance controlled connectors provide reliable signal integrity.

Component Overview

The UltraSPARC™-II*i* CPU module (SME5410MCZ-270) consists of the following components:

- UltraSPARC™-II*i* Processor in a ceramic LGA package
- 256 kilobyte E-cache, made up of two (32K X 36) SRAM integrated circuits (ICs
- 32 k X 36Tag SRAM
- Clock generator, divider and buffer ICs[1]
- External Interface Connector (J0901): PCI / JTAG / temperature sense signals
- External Interface Connector (J0801): Memory / UPA64S signals

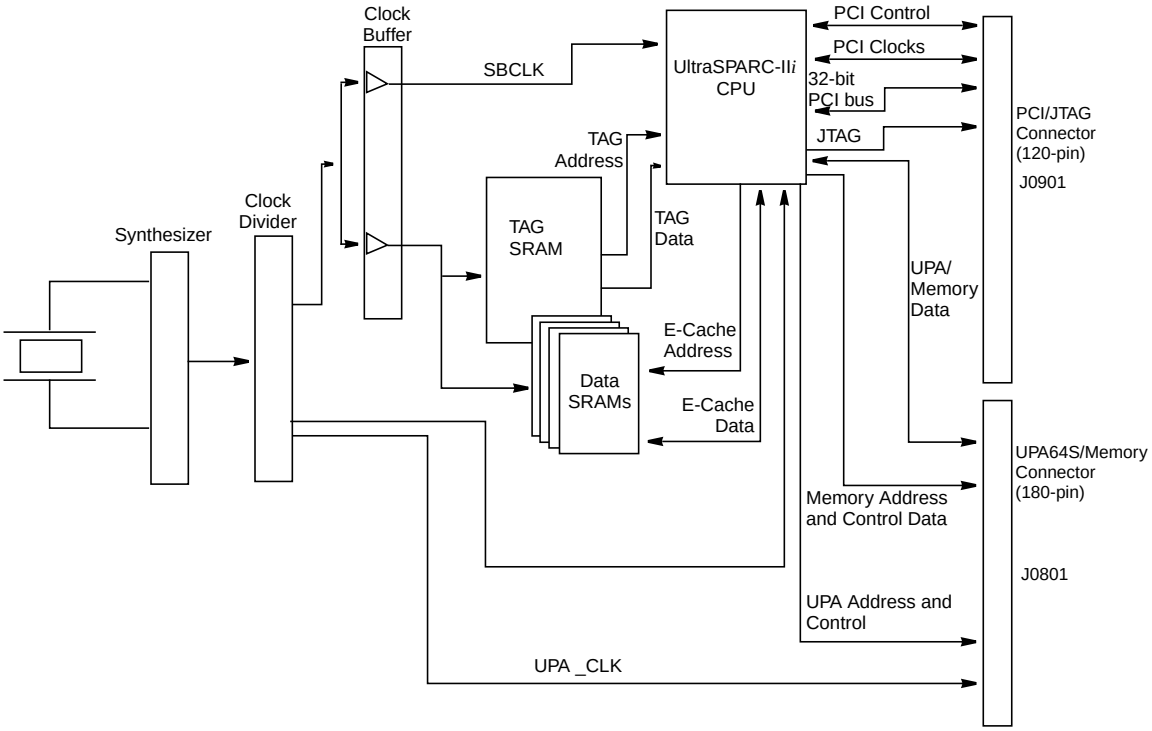


Figure 1. Module Block Diagram

1. Clock Generator: MC12430; Frequency Divider: MC100LVE39; Clock Buffer: MC10LVE210

UltraSPARC™-IIi CPU

The UltraSPARC™-II*i* processor is a high-performance, highly integrated, superscalar processor implementing the SPARC V9 64-bit RISC architecture. It is capable of sustaining the execution of up to four instructions per cycle even in the presence of conditional branches and cache misses. It supports a 44-bit virtual address space and a 41-bit physical address space. The instruction set also includes the Visual Instruction Set (VIS™) that accommodates the following functions:

- the most common operations related to two-dimensional image processing
- three-dimensional graphics
- video compression and decompression algorithms and other pixel-based algorithms
- support for high-bandwidth bcopy through block load and block store instructions

The UltraSPARC™-II*i* CPU is packaged in a ceramic 587-pin 1.27 mm Land Grid Array (LGA) package. The package dimension is 37.5 mm by 37.5 mm.

The PCI interface supports the PCI 2.1 specification with a 66 MHz clock rate or 33 MHz across a PCI bridge, for example the Advanced PCI Bridge (APB). PCI DMA transfers are cache coherent.

External Cache

The 0.5Mbyte external cache is connected to the E-cache data bus and is implemented in five synchronous register-latch SRAM ICs:

- four 64K x 18 data SRAMs configured as 64K x 64-bit data + 8-bit byte parity
- one 64K x 18 tag SRAM

The CPU-SRAM interface runs at half of the CPU pipeline frequency. SRAM signals operate at 2.6V LVCMOS levels. The SRAM clock is a differential low-voltage PECL input.

The external cache SRAMs operate in “2–2” (Register-Latched) mode which means that it takes two processor clocks to send the address and two clocks to access and return the E-cache data. 2–2 mode has a four cycle pin-to-pin latency, which provides lower E-cache latency. In addition, no dead cycles are necessary when alternating between reads and writes because of tighter control over turn on and turn off times in these SRAMs.

The cache SRAMs are plastic 119-pin, 50-mil BGA packages measuring 22 mm by 14 mm.

System Functions

System clock division is arranged to clock the on-board subsystems at the following frequencies (relative to internal CPU clock):

- UPA system interface: 64-bit, operating at 1/3 CPU frequency
- PCI bus: 32-bit, runs at 66 MHz (maximum)
- On-module E-cache SRAM: 64 bit, runs at 1/2 CPU frequency
- DRAM interface: configured for external multiplexing to 128 bits + 16 ECC bits at the DRAM

External Interface Connector Pin Assignments

Two supply voltages are required to power this module: V_{DD} at 3.3V, and V_{DD_CORE}, nominally 2.6V:

- V_{DD} powers the CPU I/O and the SRAM core
- V_{DD_CORE} supplies the core of the processor chip and SRAM I/O on the module.

Note: *Both supply voltages are driven by external system supplies.*

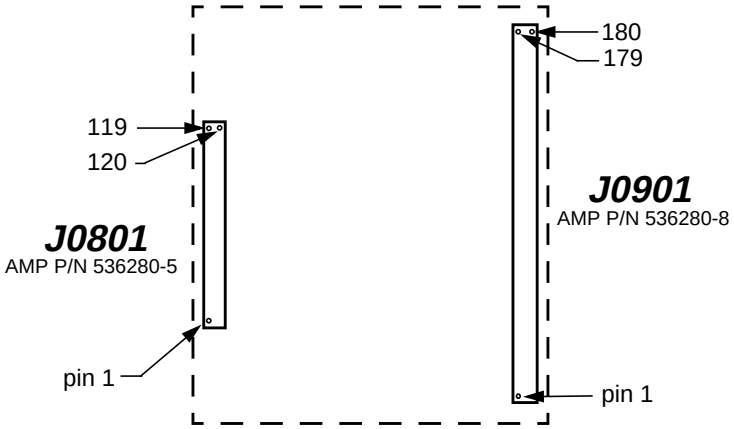


Figure 2. Connector Positions for the Module on the Motherboard (Top View)

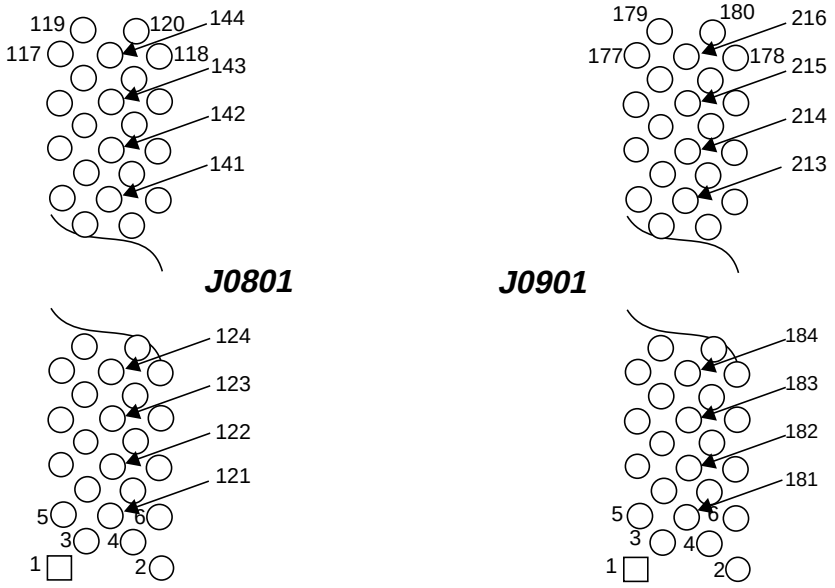


Figure 3. Module Connectors, Pin Numbering (Top View)

TECHNICAL CAPABILITIES

All performance specifications are for a 270 MHz processor, with 256 Kbyte 2-2-2 mode E-cache.

SPEC 95 Performance

System Performance	
SPECint95	8.5 (estimated)
SPECfp95	10.1 (estimated)

One of the features of UltraSPARC™-II*i* is the superior performance of its integrated I/O, DRAM and UPA64S interfaces:

Memory Performance

270 MHz with 2-2-2 mode SRAM	
Maximum E-cache read bandwidth	1.08 Gbyte/s
Maximum E-cache write bandwidth	1.08 Gbyte/s
Maximum DRAM random read bandwidth	315 Mbyte/s
Maximum DRAM random write bandwidth	315 Mbyte/s
Maximum same page read bandwidth	360 Mbyte/s
Memcopy, from DRAM to DRAM	273 Mbyte/s
Memcopy, from DRAM to UPA64S	495 Mbyte/s

FP Vector

Sustained Performance (to DRAM)	
STREAM Copy (compiled)	179 Mbyte/s
STREAM Scale (compiled)	179 Mbyte/s
STREAM Add (compiled)	190 Mbyte/s
STREAM Triad (compiled)	181 Mbyte/s

Note: *DRAM bandwidth is one-third to one-quarter greater than these numbers, since there is an initial DRAM read of the data locations that are used for store operations.*

PCI Bandwidth

PCI Sustained Bandwidth			
To DRAM from Processor PCI Bus (DMA)	66 MHz, 32-bit	Random 64-byte reads	132 Mbyte/s
		Random 64-byte writes	151 Mbyte/s
To E-cache from Processor PCI Bus (DMA)	66 MHz, 32-bit	Random 64-byte reads	163 Mbyte/s
		Random 64-byte writes	186 Mbyte/s
From Processor to Processor PCI bus (PIO)	66 MHz, 32-bit	64-byte writes	200 Mbyte/s

All sustained DMA numbers are for a single device. Multiple devices on separate secondary buses can cause higher sustained bandwidths. In no case is the combined bandwidth from two secondary buses less than the peak bandwidth available from one bus. This is because of efficient internal arbitration between multiple events in the bus bridge.

UPA64S Bandwidth

UPA PIO Bandwidth			
From Processor, to UPA64S (PIO)	90 MHz, 64-bit	Random 64-byte writes	540 Mbyte/s
		Compressed 8-byte writes	720 Mbyte/s

PCI Bandwidth with APB (33MHz Secondary Bus)

PCI Secondary Sustained Bandwidth			
From Processor, to Secondary PCI Bus (PIO)	33 MHz, 32-bit	64-byte Writes	124 Mbyte/s
To DRAM from Secondary PCI Bus (DMA)	33 MHz, 32-bit	Random 64-byte reads	78 Mbyte/s
		Random 64-byte writes	124 Mbyte/s

SIGNAL DESCRIPTIONS

Quick Signal Reference - Clock Interface

Symbol	Type [1]	Name and Function
UPA_CLK_POS, UPA_CLK_NEG	O PECL	Differential 3.3V PECL clock supplied to the UPA64S interface
PCI_REF_CLK	I	PCI reference clock; Should be 66 MHz. But this can be a 33 MHz PCI, if a 33 MHz PCI interface is required
PCI_REF_CLK	I	PCI clock; always 66 MHz; doubled to 133 MHz for use in an internal PCI logic

1. KEY: O – output; I – input; I/O – input or output; PECL – Positive Emitter-coupled Logic

Quick Signal Reference - JTAG/ Test /Temperature Interface (J0901)

Symbol	Type	Name and Function
TDO	O	IEEE 1149 test data output; tri-state signal driven only when the TAP controller is in the shift-DR state
TDI	I	IEEE 1149 test data input; pin is internally pulled to logic one when not driven.
TCK	I	IEEE 1149 test clock input; pin must always be driven to logical 1 or logical 0 if not tied to a clock source
TMS	I	IEEE 1149 test mode select input; internally pulled to logic 1 when not driven
TRST_L	I	IEEE 1149 test reset input (active low); internally pulled to logical 1 when not driven
TEMP_SENSE[1:0]	O	Temperature sensing thermistor terminals on the module
MFG_L	I	For manufacturing test use, no connect

Quick Signal Reference - Initialization Interface

Symbol	Type	Name and Function
PO_RST_L	I	For non power-on resets; for debug; asynchronous assertion and de-assertion; active low
S_DATA	I	Serial frequency-setting data for MC12430 module clock synthesizer
S_CLK	I	Data clock for module clock synthesizer
S_LOAD	I	Serial load mode pin for clock synthesizer
X_RESET_L	I	Driven to signal XIR traps; for debug; behaves as a non-maskable interrupt; asynchronous assertion and de-assertion; active low
SYS_RESET_L	I	Driven for POR (power-on) resets; asynchronous assertion and de-assertion; active low
PCI_RESET_L	O	Resets PCI subsystem; asynchronous assertion and monotonic deassertion; also used for UPA64S reset
PCI_CLKSEL[1:0]	O	Selects PCI clock frequency generated on the system board
VID[4:0]	O	V_{dd_CORE} voltage digital programming

Quick Signal Reference - PCI interface

Symbol	Type	Name and Function
PPCI_AD[31:0]	I/O	Address and data bits are multiplexed on these PCI pins
PPCI_CBE_L[3:0]	I/O	Bus command and byte enables are multiplexed on these PCI pins
PPCI_PAR	I/O	Parity; even parity generated across AD[31:0] and CBE_L[3:0]
PPCI_DEVSEL_L	STS [1]	Device Select; indicates the driving device has decoded its address as the target of the current access; as input, indicates whether any device has been selected
PPCI_FRAME_L	STS	Cycle Frame; driven by current master to indicate beginning and end of an access
PPCI_REQ_L[3:0]	I	Request; indicates to arbiter that an external device requires use of the bus
PPCI_GNT_L[3:0]	T/S [2]	Grant; indicates to device that access to the bus has been granted
PPCI_IRDY_L	STS	Initiator Ready; indicates the bus master's ability to complete the current data phase
PPCI_TRDY_L	STS	Target Ready; indicates the selected device's ability to complete the current data phase.
PPCI_PERR_L	O/D [3]	Parity error; reports data parity errors
PPCI_SERR_L	O/D	System Error; reports address parity errors, data parity errors on special cycles, or any other catastrophic PCI errors
PPCI_STOP_L	STS	Stop; indicates that current target is requesting that the master stop the current transaction

1. Sustained tri-state, bidirectional; only one driver at a time; must drive high for one cycle before letting the line float. External pullups maintain the high level between drives, and are needed on the motherboard.

2. Tri-state output.

3. Open drain; as STS, but allows multiple devices to be wire-ORed. A pullup is required to sustain the inactive state, and should be implemented on the motherboard.

Quick Signal Reference - Interrupt Interface

Symbol	Type	Name and Function
SB_DRAIN	O	Store Buffer Drain; asserted after Interrupts or by software to cause outstanding DMA writes to be flushed from downstream buffers on the PCI
SB_EMPTY[1:0]	I	Store Buffer Empty; assert when the APB PCI bus bridge chip has guaranteed that all DMA writes queued before the assertion of SB_DRAIN have left the bus bridge
INT_NUM[5:0]	I	Interrupt Number; sampled at 66 MHz PCI clock rate; encoded Interrupt request from the RIC chip.

Quick Signal Reference - Memory and XCVR Interface

Symbol	Type	Name and Function
MEM_WE_L	O	Memory Write Enable; active low
MEM_CAS_L[1:0]	O	Memory Column Address Strobe; active low
MEM_RAST_L[3:0]	O	Memory Row Address Strobe, Top; active low
MEM_RASB_L[3:0]	O	Memory Row Address Strobe, Bottom, active low
SYS _DAT[63:0]	I/O	Memory / UPA64S data bus
MEM_ECC[7:0]	I/O	Memory ECC bits
MEM_ADR[12:0]	O	Memory Address bus, (row and column)
XCVR_OEA_L	O	Transceiver Output Enable A; active low
XCVR_OEB_L	O	Transceiver Output Enable B; active low
XCVR_SEL_L	O	Transceiver Select; Active low; picks high or low half of read data
XCVR_WR_CNTL[1:0]	O	Transceiver Write Control; controls clock enables on internal registers
XCVR_RD_CNTL[1:0]	O	Transceiver Read Control; controls clock enables on internal registers
XCVR_CLK[2:0]	O	Transceiver Clock; all data and control signals are registered by these clocks; multiple outputs to minimize loading effects of six transceivers; should be parallel terminated to GND on the motherboard

Quick Signal Reference - UPA64S Interface

Symbol	Type	Name and Function
UPA_S_REPLY[2:0]	O	UPA_S_REPLY; encoded command that indicates arrival of write data on MEM_DATA[63:0], or command to drive MEM_DATA[63:0] with read data
UPA_P_REPLY[1:0]	I	UPA_P_REPLY; Encoded command that indicates consumption of prior write, or ability to provide read data
UPA_ADR[28:0]	O	UPA_ADR; sends 2 cycle address packet to UPA64S slave, or provides internal state debug information
UPA_ADR_VLD	O	UPA_ADR_VLD; asserted during first cycle of two cycle address packet
SYS-DAT[63:0]	I/O	Memory/UPA64S Data bus

CLOCK DISTRIBUTION

A raw clock signal is generated within the module using a Motorola high frequency PLL clock generator (MC12430) with a 16MHz series resonant crystal. The MC12430 provides a serial and parallel interface for configuring the frequency synthesis. The parallel interface pins are hardwired on the module but the serial interface signals S_LOAD, S_DATA, and S_CLOCK are brought out to the Memory / UPA64S external connector to allow clock configuration from the motherboard.

The raw clock from this clock generator is divided down in a clock divider (MC100LVEL39) to produce the processor SRAM and UPA64S clock signals. Only the differential Low Voltage Positive ECL (LVPECL) UPA64S clock signal (at 1 / 3 of the CPU clock frequency) is output to the 180-pin Memory / UPA64S external connector.

An clock buffer (MCLVE210) distributes the CPU and SRAM clocks.

The JTAG TCK signal enters the module via the 120-pin PCI / JTAG connector (J0901) and connects to the SRAMs and the UltraSPARC™-II*i* processor.

The incoming motherboard PCI_CLK and the PCI_REF_CLK signals also arrive at the PCI / JTAG / Temperature sense interface connector and travel to the UltraSPARC™-II*i*.

The UltraSPARC™-II*i* CPU module can select motherboard PCI clock generator frequency values to be in either the 66 MHz / 33 MHz or the 60 MHz / 30 MHz sets. The PCI / JTAG connector (J0901) signals (PCI_CLKSEL0 and PCI_CLKSEL1) provide frequency-encoding bits that conform to IC Works' CPU / PCI System Clock Generator (Part Number W48C60-422) specification. The table "PCI Frequency Selection." shows this encoding.

.

TABLE 1: PCI Frequency Selection

PCI_CLKSEL0	PCI_CLKSEL1	PCI Clock Rate
0	1	30/60 MHz
1	0	33/66 MHz

Figure 4 shows a schematic diagram of the module clock distribution.

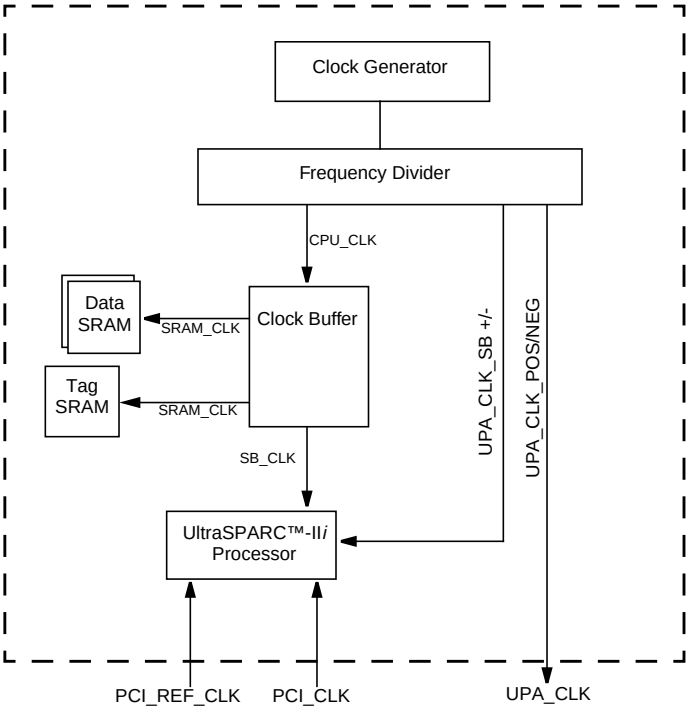


Figure 4. Module Clock Distribution

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings[1] [2]

Symbol	Parameter	Rating	Units
V_{DD}	Supply voltage range for I/O	0 to 3.8 V	V
V_{DD_CORE}	Supply voltage range for CPU core	0 to 2.7 [3]	V
V_I	Input voltage range	V_{ss} - 0.5 < V_I < V_{DD} + 0.5	V
V_O	Output voltage range	V_{ss} - 0.5 < V_O < V_{DD} + 0.5	V
I_{IK}	Input clamp current (V_I < 0 - TBD or V_I > V_{DD} + TBD)	20	mA
I_{OK}	Output clamp current (V_I < 0 - TBD or V_I > V_{DD} + TBD)	± 50	mA
I_{OL}	Current into any output in the low state	50	mA
T_{STG}	Storage temperature	-20 to +125	°C

1. Operation of the device at values exceeding those listed may result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under in the following table, "Recommended Operating Conditions." is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. Unless otherwise noted, all voltages are with respect at V_{SS} (ground).
3. At all times: $V_{DD\_CORE} \leq V_{DD}$ + 0.5 V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply voltage for I/O	3.2	3.3	3.46	V
V_{DD_CORE}	Supply voltage for the CPU core	2.52	2.6	2.68	V
V_{SS}	Ground (GND)	-	0	-	V
I_{OH}	High-level output current	-	-	-4.0	mA
I_{OL}	Low-level output current	-	-	8.0	mA
T_J	Operating junction temperature	-	-	105	°C
T_A	Operating ambient temperature	0	-	see note [1]	°C

1. Maximum allowable ambient temperature depends upon air flow rate and must be chosen so that the maximum junction temperature does not exceed T_J. See "Thermal Specifications and Analysis" on page 21.

DC Characteristics

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{OH}	High-level output voltage	2.6V signals	V_{DDO} = Min, I_{OH} = Max	2.4	-	-	V
		3.3V non-PCI signals	V_{DDH} = Min, I_{OH} = Max	2.4	-	-	V
		3.3V PCI signals	Iout = -500 µA	$0.9V_{DD}$	-	-	V
V_{OL}	Low-level output voltage	2.6V signals	V_{DDO} = Min, I_{OL} = Max	-	-	0.4	V
		3.3V non-PCI signals	V_{DDH} = Min, I_{OL} = Max	-	-	0.4	V
		3.3V PCI signals	Iout = 1500 µA	-	-	$0.1V_{DD}$	V
V_{IH}	High-level input voltage	2.6V signals	V_{DD_CORE} = Max	1.65	-	-	V
		PECL signals	V_{DD_CORE} = Max		V_{DD}- 0.7	-	V
		3.3 V non-PCI signals	V_{DD} = Max	2.0	-	-	V
		3.3V PCI signals	V_{DDH} = Max	$0.5V_{DD}$	-	V_{DD}+ 0.5	V
V_{IL}	Low-level input voltage	2.6V signals	V_{DD_CORE} = Min	-	-	1.15	V
		PECL signals	V_{DD_CORE} = Min		V_{DD}-1.4		V
		3.3V non-PCI signals	V_{DD} = Min	-	-	0.8	V
		3.3V PCI signals	V_{DDH} = Min	- 0.5	-	$0.3V_{DD}$	V
I_{DD}	Supply current for V_{DD}		V_{DD} = Max	-	2.2	TBA [1]	A
I_{DD_CORE}	Supply current for V_{DD_CORE}		V_{DD_CORE} = Max	-	6.2	8	A
I_{OZ}	High-impedance output current (outputs without pullups)		V_{DD} = Max, V_O = 2.4 V	-	-	20	µA
			V_{DD} = Min, V_O = 0.4 V	-	-	-20	µA
I_I	Input current (inputs without pullups)		V_{DD} = Max, V_I = V_{SS} to V_{DD}	-	-	20	µA
	Input current (inputs with pullups)		V_{DD} = Max, V_I = V_{SS} to V_{DD}	-	-	250	µA

1. To be announced

POWER REQUIREMENTS

The UltraSPARC™-II*i* CPU module requires two V_{DD} supply voltages, V_{DD} and V_{CC_CORE}, nominally at 3.3 V and 2.6 V, respectively. These supplies pass to the module through connector blades on both 120 and 180 pin connectors. The V_{DD_CORE} supply is programmable from the module through resistor stuffing options in accordance with the following table: "Vdd-Core Voltage Encoding." The digital encoding is driven on the VID[4:0] signals of the 180 pin connector pins, one through six.

Estimated power consumption is 30 Watts at 270 MHz.

Vdd-Core Voltage Encoding

Module Pins					VDD_CORE	Module Pins					VDD_CORE
VID4	VID3	VID2	VID1	VID0	V (DC)	VID4	VID3	VID2	VID1	VID0	V(DC)
0	1	1	1	1	1.30	1	1	1	1	1	No CPU Module
0	1	1	1	0	1.35	1	1	1	1	0	2.1
0	1	1	0	1	1.40	1	1	1	0	1	2.2
0	1	1	0	0	1.45	1	1	1	0	0	2.3
0	1	0	1	1	1.50	1	1	0	1	1	2.4
0	1	0	1	0	1.55	1	1	0	1	0	2.5
0	1	0	0	1	1.60	1	1	0	0	1	2.6
0	1	0	0	0	1.65	1	1	0	0	0	2.7
0	0	1	1	1	1.70	1	0	1	1	1	2.8
0	0	1	1	0	1.75	1	0	1	1	0	2.9
0	0	1	0	1	1.80	1	0	1	0	1	3.0
0	0	1	0	0	1.85	1	0	1	0	0	3.10
0	0	0	1	1	1.90	1	0	0	1	1	3.20
0	0	0	1	0	1.95	1	0	0	1	0	3.30
0	0	0	0	1	2.00	1	0	0	0	1	3.40
0	0	0	0	0	2.05	1	0	0	0	0	3.50

TIMING SPECIFICATIONS

Timing design within the module makes demands upon signal timing at the module connectors. This section describes internal module timing when it is useful to explain external requirements. For detailed information on timing and latencies see Sun publications:

- UltraSPARC–II*i* Microprocessor Data Sheet, SME1040CGA [1]
- UltraSPARC–II*i* Microprocessor User's Manual, SME1040CGA [2]

PCI

PCI_CLK and PCI_REF_CLK traces on the module are matched in length to within 0.5 in, that is, about 100 ps at a nominal length of 550 ps. These signals have no added delay and their trace lengths are also within ± 0.5 in of those of the other PCI signals. Setup, hold and propagation times are listed in the UltraSPARC™-II*i* processor component data sheet [1].

DRAM

DRAM signals are all matched to within 0.5 inches on the module.

SRAM

The UltraSPARC™-II*i* processor's second level (L2) cache is implemented using synchronous SRAMs mounted on the module. The data bus is 64 bits plus 8 parity bits. There is also a tag SRAM interfacing to a 16-bit bus that includes two parity bits. While the tag and data SRAMs share no signals, the tag implements the same timing scheme as the data SRAMs for a given module. Generally the tag SRAM timing is slightly less critical than for the data SRAMs. This is due to two factors: one, the physical layout of the data bits and address bits; and two, the additional loading on the data SRAM interface.

1. Document Part Number: 805-0086-03
2. Document Part Number: 805-0087-01

UPA

Within the module design, the following sets of clock signals are synchronous:

- UltraSPARC™-II*i* SRAM_CLK
- UltraSPARC™-II*i* UPA_CLK
- UPA_CLK input to the fast-frame-buffer ASIC external to the module
- CPU_CLK input to the UltraSPARC™-II*i* processor

Any timing mismatches between these clocks linearly degrade the timing to and from the UltraSPARC™-II*i* and fast frame buffer (FFB). The FFB uses the UPA64S data interface.

Since these signals are completely contained on the module (with the exception of the UPA_CLK), the system board must match the delay assumed by the module design.

The clock skew includes:

- Separate buffers on the module: ± 200 ps
- UltraSPARC™-II*i* and FFB sockets: ± 50 ps.
- Board fabrication variance: ± 250 ps
- Setup / hold / clock input to data-output delay differences: ± 150 ps
- System noise: ± 150 ps

When doing a system timing budget, this total skew must be added to the setup, hold, and propagation times listed for UPA and DRAM signals in the CPU component data sheet (SME1040).

The module is designed for 6 inches of motherboard trace plus 3.4 in of FFB trace plus simulated differences in ASIC / UltraSPARC™-II*i* setup times. These are internal ≈ 180 ps / inch. traces**.**

MECHANICAL SPECIFICATIONS

The UltraSPARC-IIi 270 MHz / 256 Kbyte module is characterized by:

- Dimensions: 100 mm x 130 mm x 45 mm (height)
- Heat Sink: Aluminum pin fin

Figure 5 illustrates the module and its heat sinks.

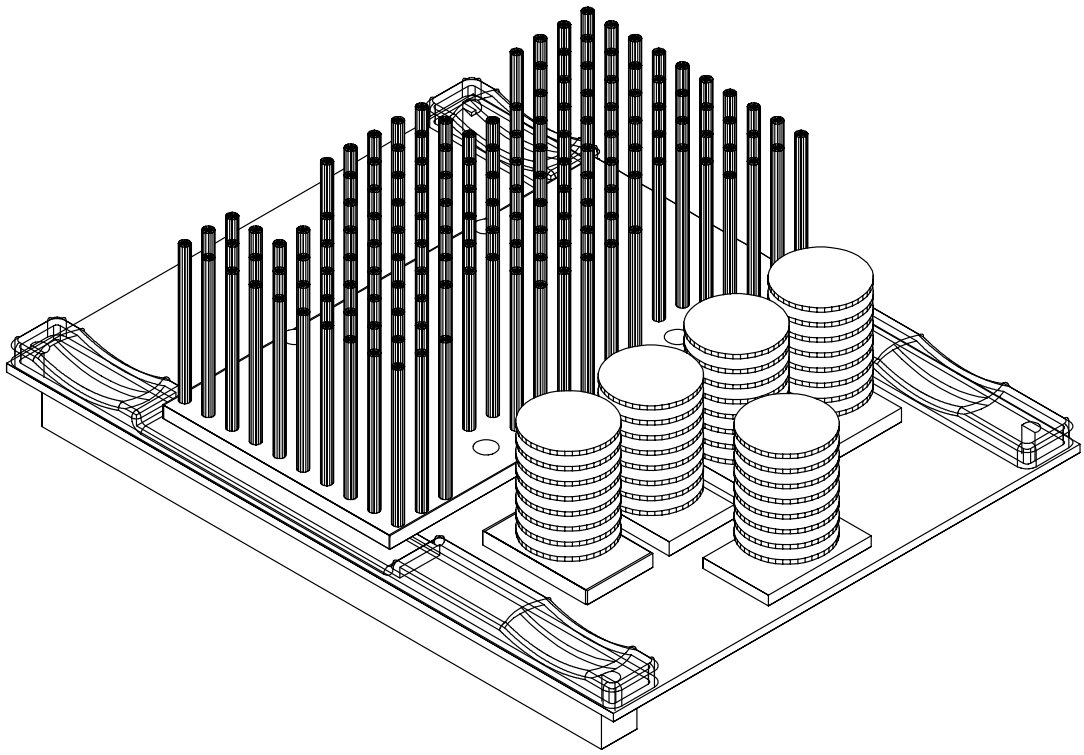
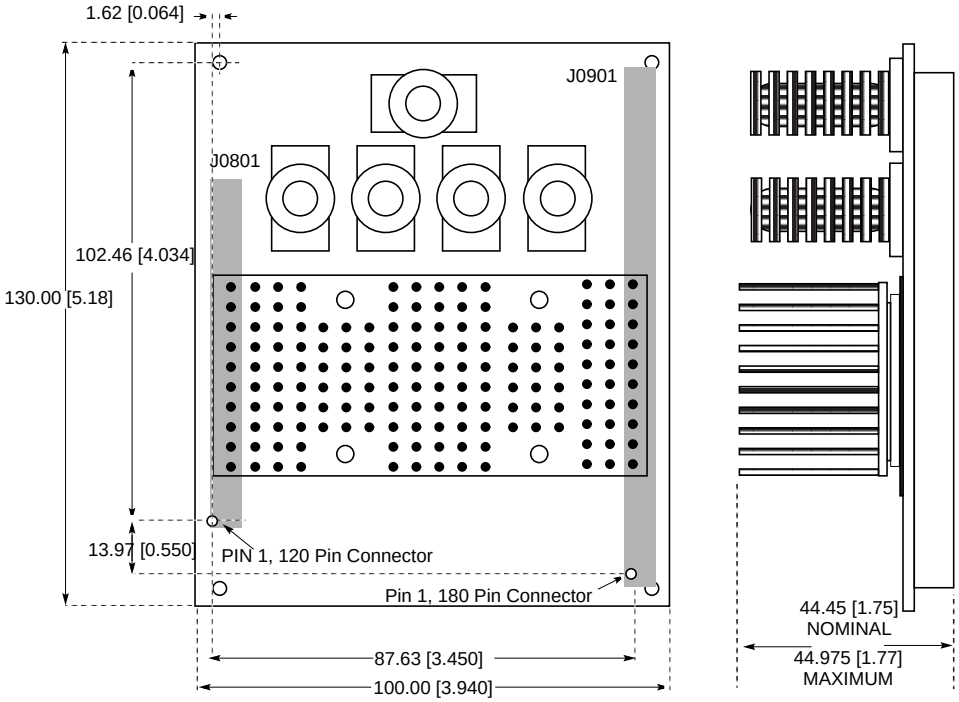


Figure 5. UltraSPARC™-II*i* CPU module with Heat Sinks



Dimensions in mm [inches]

Figure 6. Module Dimensions

JTAG INTERFACE

The UltraSPARC™-II*i* CPU module (SME5410MCZ-270) implements the IEEE 1149.1 JTAG standard to aid in board level testing. A Boundary Scan Description Language (BSDL) file is available for these devices.

AC Characteristics - JTAG Timing (estimated values)

Symbol	Parameter	Signals	Conditions	270 Mhz			Units
				Min	Typ	Max	
t_W ($\overline{TRST}$)	Test reset pulse width	$\overline{TRST}$ [1]		5	–	–	ns
t_{SU} (TDI)	Input setup time to TCK	TDI		–	3	–	ns
t_{SU} (TMS)	Input setup time to TCK	TMS		–	4	–	ns
t_H(TDI)	Input hold time to TCK	TDI		–	1.5	–	ns
t_H(TMS)	Input hold time to TCK	TMS		–	1.5	–	ns
t_{PD}(TDO)	Output delay from TCK [2]	TDO	I_{OL} = 8 mA	–	6	–	ns
t_{OH}(TDO)	Output hold time from TCK [2]	TDO	I_{OH} = -4 mA C_L = 35 pF V_{LOAD} = 1.5V	–	–	3	ns

1. $\overline{TRST}$ is an asynchronous reset.
2. TDO is referenced from falling edge of TCK.

JTAG Timing

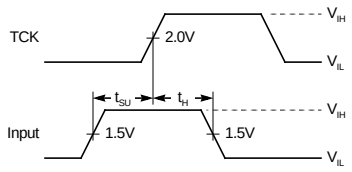


Figure 7. Voltage Waveforms - Input Setup and Hold Times

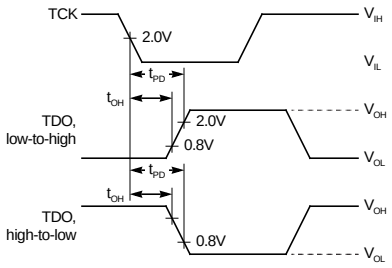


Figure 8. Voltage Waveforms - Output Propagation Delay Times

THERMAL SPECIFICATIONS AND ANALYSIS

Thermal maps of the UltraSPARC™-II*i* CPU module indicate that by keeping the CPU device cool, the SRAMs and clock circuitry on the module are also kept cool.

The operating performance of a CPU device is determined by its junction temperature. The CPU temperature specification may be provided in terms of its junction or case temperature. This section describes how to estimate the case temperature from the airflow condition. It also describes how to measure the case temperature directly in order to verify the cooling design.

Using the Heatsink Temperature method is the preferred verification method. It is distinctly more accurate than measurements taken using the Airflow Cooling Estimate method. The Case Temperature method is more difficult to perform, but also yields good results.

In all cases, the junction temperature must not exceed the device specification (typically 105 °C). The lower the junction temperature, the higher the system reliability.

The following table specifies the terms, definitions and specifications used in order to calculate thermal specifications for the UltraSPARC–II*i* CPU device.

Thermal Definitions and Specifications

Term	Definition	Specification
Tj	Device junction temperature	Can't be measured directly, must always be estimated at less than 105 °C, lower is preferred.
Tc	Case temperature	Measurable at the top-center of the device. Requires a hole in the base of the heatsink to allow the thermocouple to be in contact with the case.
Ts	Heatsink temperature	Measurable as the temperature of the base of the heatsink. Best approach is to embed a thermocouple in a cavity drilled in the heatsink base. An alternative is to place the thermocouple down between the fins / pins of the heatsink (insulated from the airflow) and in contact with the base plate of the heatsink.
Ta	Module ambient air temperature	Air temperature as it approaches the heatsink.
Pd	Power dissipation of the CPU	8 watts for the UltraSPARC–II*i* 270 MHz CPU
θjc	Junction-to-case thermal resistance of the package	This value is approximately 0.5°C / W
θcs	Case-to-heatsink thermal resistance	This value is approximately 0.1 °C / W when good thermal grease contact is made between the package and the heatsink.
θsa	Heatsink-to-air thermal resistance	This value is dependent on the heatsink design, the airflow direction, and the airflow velocity. (see Table 2)
Airflow	Free Stream Airflow	Unchanneled airflow velocity approaching the heatsink.

Case Temperature Method

The relationship between case temperature and junction temperature is described in the following thermal equation.

If Tc is known, then Tj can be calculated:

$$Tj = Tc + (Pd \times \theta jc)$$

There is good tracking between the case temperature and the heat sink temperature.

Heatsink Temperature Method (the preferred method)

Measuring the heat sink temperature is sometimes easier than measuring the case temperature. This method provides accurate results for most designs. If the heatsink temperature (Ts) is known then the following thermal equation can be used to estimate the junction temperature:

$$Tj = Ts + [Pd (\theta jc + \theta cs)]$$

Airflow Cooling Estimate Method

The relationship between air temperature and junction temperature is described in the following thermal equation:

$$Tj = Ta + [Pd (\theta jc + \theta cs + \theta sa)]$$

Determination of the ambient air temperature (Ta) and the “free-stream” air velocity is required in order to apply the airflow method. The section "Heatsink-to-Air Thermal Resistance" on page 23, uses the air velocity direction relative to the heatsink orientation to find the thermal resistance between the heat sink and air (θsa).

Note that the airflow velocity can be measured using a velocity meter. Alternatively it may be determined by knowing the performance of the fan that is supplying the airflow. Calculating the airflow velocity is difficult. It is subject to interpretation.

> ***Note:*** *The Airflow Cooling Estimate method is an estimate. Use it solely when an approximate value suffices. Accuracy can only be assured using the Case Temperature method or the Heatsink Temperature method. Apply these methods for the greatest accuracy.*

"Heatsink-to-Air Thermal Resistance" specifies the thermal resistance of the heatsink as a function of airflow velocity. Notice that the airflow direction also affects the performance of the heatsink.

Heatsink-to-Air Thermal Resistance

Air Velocity (ft./min) [1]	150	200	300	400	500	650	800	1000
θ_{SA} (°C/W) [2]	1.21	1.05	0.91	0.84	0.78	0.72	0.67	0.64

1. Channeled through the heat sinks
2. Airflow direction parallel to the shorter axis of the pin-fin heat sink (1.9"L x 3.6"W x 1.1"H)

Thermal Air flow

Air Flow Topside

150 LFM @ 30 °C up to 2,000 feet, altitude, maximum

300 LFM @ 40 °C up to 10,000 feet, altitude, maximum

Air Flow Bottom-side

100 LFM @ 30 °C up to 2,000 feet, altitude, maximum

150 LFM @ 40 °C up to 10,000 feet, altitude, maximum

MODULE CONNECTOR PIN ASSIGNMENTS

This list specifies pin assignments and the corresponding signals for the External Interface Connector (J0801): Memory / UPA64S connector.

External Interface Connector (J0801): Memory/UPA64S Signals and Pin Assignments

Pin#	Signal Name	Pin #	Signal Name
1	VID0	2	VID1
3	VID2	4	VID3
5	SPARE	6	VID4
7	GND	8	MFG_L
9	XCVR_CLK0	10	GND
11	GND	12	XCVR_CLK1
13	XCVR_CLK2	14	GND
15	GND	16	XCVR_RD_CNTL_0
17	XCVR_OEA_L	18	XCVR_SEL_L
19	XCVR_OEB_L	20	XCVR_RD_CNTL_1
21	XCVR_WR_CNTL_0	22	XCVR_WR_CNTL_1
23	SPARE	24	GND
25	GND	26	MEM_ADR2
27	MEM_ADR0	28	MEM_ADR3
29	MEM_ADR1	30	MEM_ADR6
31	MEM_ADR4	32	MEM_ADR8
33	MEM_ADR5	34	MEM_ADR9
35	MEM_ADR7	36	MEM_ADR10
37	MEM_ADR11	38	MEM_ADR12
39	GND	40	GND
41	SYS_DAT00	42	SYS_DAT02
43	SYS_DAT01	44	SYS_DAT04
45	SYS_DAT03	46	SYS_DAT06
47	SYS_DAT05	48	SYS_DAT08
49	SYS_DAT07	50	SYS_DAT10
51	SYS_DAT09	52	SYS_DAT12
53	SYS_DAT11	54	SYS_DAT14
55	SYS_DAT13	56	SYS_DAT16
57	SYS_DAT15	58	SYS_DAT18
59	SYS_DAT17	60	SYS_DAT20
61	SYS_DAT19	62	SYS_DAT22
63	SYS_DAT21	64	SYS_DAT24
65	SYS_DAT23	66	SYS_DAT26
67	SYS_DAT25	68	SYS_DAT28
69	SYS_DAT27	70	SYS_DAT30
71	SYS_DAT29	72	SYS_DAT32
73	SYS_DAT31	74	SYS_DAT34
75	SYS_DAT33	76	SYS_DAT36
77	SYS_DAT35	78	SYS_DAT37
79	GND	80	SPARE

External Interface Connector (J0801): Memory/UPA64S Signals and Pin Assignments

Pin#	Signal Name	Pin #	Signal Name
81	SPARE	82	VDD
83	MEM_WE_L	84	MEM_RAST_L <1>
85	MEM_CAS_L <0>	86	MEM_CAS_L <1>
87	MEM_RAST_L <0>	88	MEM_RAST_L <2>
89	MEM_RAST3_L <3>	90	MEM_RASB_L <0>
91	MEM_RASB_L <1>	92	MEM_RASB_L <2>
93	MEM_RASB_L <3>	94	GND
95	VDD	96	SYS_DAT38
97	SYS_DAT39	98	SYS_DAT40
99	SYS_DAT41	100	SYS_DAT42
101	SYS_DAT43	102	SYS_DAT44
103	GND	104	SYS_DAT46
105	SYS_DAT45	106	SYS_DAT48
107	SYS_DAT47	108	SYS_DAT50
109	SYS_DAT49	110	SYS_DAT52
111	SYS_DAT51	112	GND
113	SYS_DAT53	114	SYS_DAT54
115	SYS_DAT55	116	SYS_DAT56
117	SYS_DAT57	118	SYS_DAT58
119	SYS_DAT59	120	SYS_DAT60
121	SYS_DAT61	122	SYS_DAT62
123	SYS_DAT63	124	MEM_ECC0 (SYS_DAT64)
125	MEM_ECC1 (SYS_DAT65)	126	MEM_ECC2 (SYS_DAT66)
127	MEM_ECC3 (SYS_DAT67)	128	MEM_ECC4 (SYS_DAT68)
129	MEM_ECC5 (SYS_DAT69)	130	MEM_ECC6 (SYS_DAT70)
131	SPARE	132	MEM_ECC7 (SYS_DAT71)
133	UPA_ADR14	134	VDD
135	UPA_ADR13	136	UPA_ADR28
137	UPA_ADR12	138	UPA_ADR27
139	UPA_ADR11	140	UPA_ADR26
141	UPA_ADR10	142	UPA_ADR25
143	UPA_ADR09	144	UPA_ADR24
145	UPA_ADR08	146	UPA_ADR23
147	UPA_ADR07	148	UPA_ADR22
149	UPA_ADR06	150	UPA_ADR21
151	UPA_ADR05	152	UPA_ADR20
153	UPA_ADR04	154	UPA_ADR19
155	UPA_ADR03	156	UPA_ADR18
157	UPA_ADR02	158	UPA_ADR17
159	UPA_ADR01	160	UPA_ADR16
161	UPA_ADR00	162	UPA_ADR15
163	GND	164	VDD
165	UPA_CLK_POS	166	SPARE
167	UPA_CLK_NEG	168	S_DATA
169	GND	170	GND

External Interface Connector (J0801): Memory/UPA64S Signals and Pin Assignments

Pin#	Signal Name	Pin #	Signal Name
171	ADR_VLD	172	UPA_S_REPLY2
173	P_REPLY1	174	UPA_P_REPLY0
175	S_REPLY0	176	UPA_S_REPLY1
177	S_CLK	178	S_LOAD
179	VDD	180	VDD
181	GND	182	GND
183	GND	184	GND
185	VDD	186	VDD
187	VDD	188	VDD
189	GND	190	GND
191	GND	192	GND
193	VDD	194	VDD
195	VDD	196	VDD
197	GND	198	GND
199	GND	200	GND
201	VDD	202	VDD
203	VDD	204	VDD
205	GND	206	GND
207	GND	208	GND
209	VDD	210	VDD
211	VDD	212	VDD
213	GND	214	GND
215	GND	216	GND

The following list identifies the PCI, JTAG and Temperature Sense signals, and corresponding pin assignments.

PCI/JTAG/Temperature Sense Interface (J0901) (signal name and pin assignment)

Pin #	Signal Name	Pin #	Signal Name
1	VDD_CORE	2	VDD_CORE
3	GND	4	GND
5	VDD_CORE	6	VDD_CORE
7	GND	8	GND
9	GND	10	GND
11	GND	12	GND
13	VDD_CORE	14	VDD_CORE
15	GND	16	GND
17	GND	18	GND
19	VDD_CORE	20	VDD_CORE
21	GND	22	GND
23	VDD_CORE	24	VDD_CORE
25	GND	26	GND
27	GND	28	GND
29	GND	30	GND
31	VDD_CORE	32	VDD_CORE
33	GND	34	GND
35	VDD_CORE	36	VDD_CORE
37	GND	38	GND
39	PPCI_AD0	40	PPCI_AD1
41	PPCI_AD2	42	PPCI_AD3
43	PPCI_AD4	44	PPCI_AD5
45	PPCI_AD6	46	PPCI_CBE_L0
47	PPCI_AD7	48	PPCI_AD9
49	PPCI_AD8	50	PPCI_AD10
51	PPCI_AD11	52	PPCI_AD12
53	PPCI_AD13	54	PPCI_AD14
55	PPCI_AD15	56	PPCI_CBE_L1
57	PPCI_PAR	58	PPCI_SERR_L
59	SPARE	60	PPCI_REQ_L2
61	PPCI_PERR_L	62	PPCI_DEVSEL_L
63	PPCI_REQ_L3	64	PPCI_IRDY_L
65	PPCI_STOP_L	66	PPCI_CBE_L2
67	PPCI_TRDY_L	68	PPCI_AD17
69	PPCI_FRAME_L	70	PPCI_AD19
71	PPCI_AD16	72	PPCI_AD21
73	PPCI_AD18	74	PPCI_AD22
75	PPCI_AD20	76	PPCI_AD23
77	PPCI_REQ_L1	78	PPCI_CBE_L3
79	PPCI_AD24	80	PPCI_AD27
81	PPCI_AD25	82	PPCI_AD28
83	PPCI_AD26	84	PPCI_AD29
85	PPCI_AD30	86	PPCI_AD31

PCI/JTAG/Temperature Sense Interface (J0901) (signal name and pin assignment)

Pin #	Signal Name	Pin #	Signal Name
87	PPCI_GNT_L0	88	PCI_CLKSEL0
89	PCI_RESET_L	90	PPCI_REQ_L0
91	GND	92	GND
93	PCI_CLK	94	PCI_REF_CLK
95	GND	96	GND
97	PPCI_GNT_L2	98	PPCI_GNT_L1
99	SB_EMPTY0	100	PPCI_GNT_L3
101	SB_EMPTY1	102	SB_DRAIN
103	INT_NUM0	104	INT_NUM1
105	INT_NUM2	106	INT_NUM3
107	INT_NUM4	108	INT_NUM5
109	SYS_RESET_L	110	PO_RST_L
111	X_RESET_L	112	TCK
113	TDO	114	TMS
115	TDI	116	TEMP_SENSE1
117	TRST_L	118	TEMP_SENSE0
119	PCI_CLKSEL1	120	EPD
121	VDD_CORE	122	VDD_CORE
123	VDD_CORE	124	VDD_CORE
125	VDD_CORE	126	VDD_CORE
127	VDD_CORE	128	VDD_CORE
129	GND	130	GND
131	GND	132	GND
133	VDD	134	VDD
135	VDD	136	VDD
137	GND	138	GND
139	GND	140	GND
141	VDD	142	VDD
143	VDD	144	VDD

ORDERING INFORMATION

Part Number	Speed	Description
SME5410MCZ-270	270 MHz CPU, 90 MHz UPA	High performance, SPARC V9-compliant processor module with a clock generation and a 256 Kbyte L2 cache implanted in 3 RAMs. Standard interfaces include DRAMM in DIMM format, 100 MHz UPA64s, and a 66 MHz PCI.

SME5410MCZ-270

THE NETWORK IS THE COMPUTER™

Sun Microsystems, Inc.
901 San Antonio Road
Palo Alto, CA 94303-4900 USA
800 / 681-8845
www.sun.com / microelectronics

Part Number: 805-1480-03