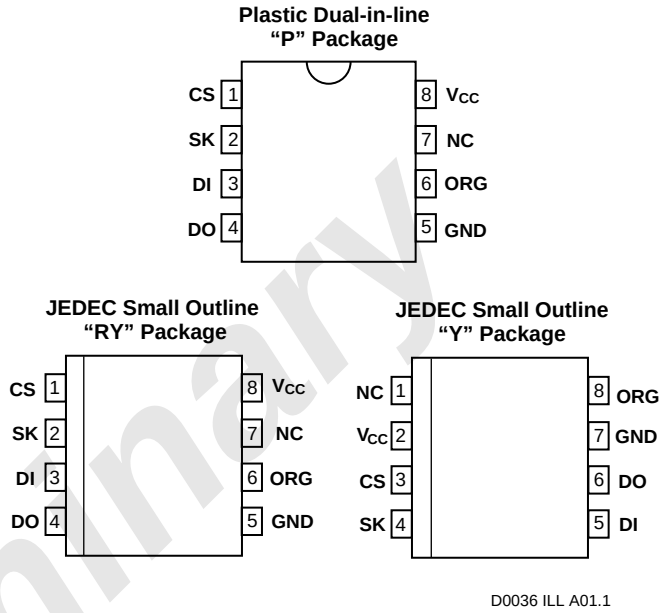
Preliminary Information

2,048-Bit Serial Electrically Erasable PROM
1.8V to 5.5V Operation

FEATURES

- **1.8V to 5.5V Operation**
- **Extended Temperature Range: -40°C to +85°C**
- **User Selectable Word length**
- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— Fully TTL compatible inputs and outputs**
  - **— Auto increment for efficient data dump**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
  - **— V_{CC} lockout inadvertent write protection (XL93LC56A)**
- **Low Power Consumption**
  - **— 1mA active**
  - **— 1μA standby**
- **Advanced Low Voltage CMOS E^2PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 100-year data retention after 100K write cycles**
  - **— Minimum of 100,000 erase/write cycles**
  - **— Unlimited read cycles**
  - **— ESD protection (EIAJ and JEDEC standard)**

PIN CONFIGURATIONS



PIN NAMES

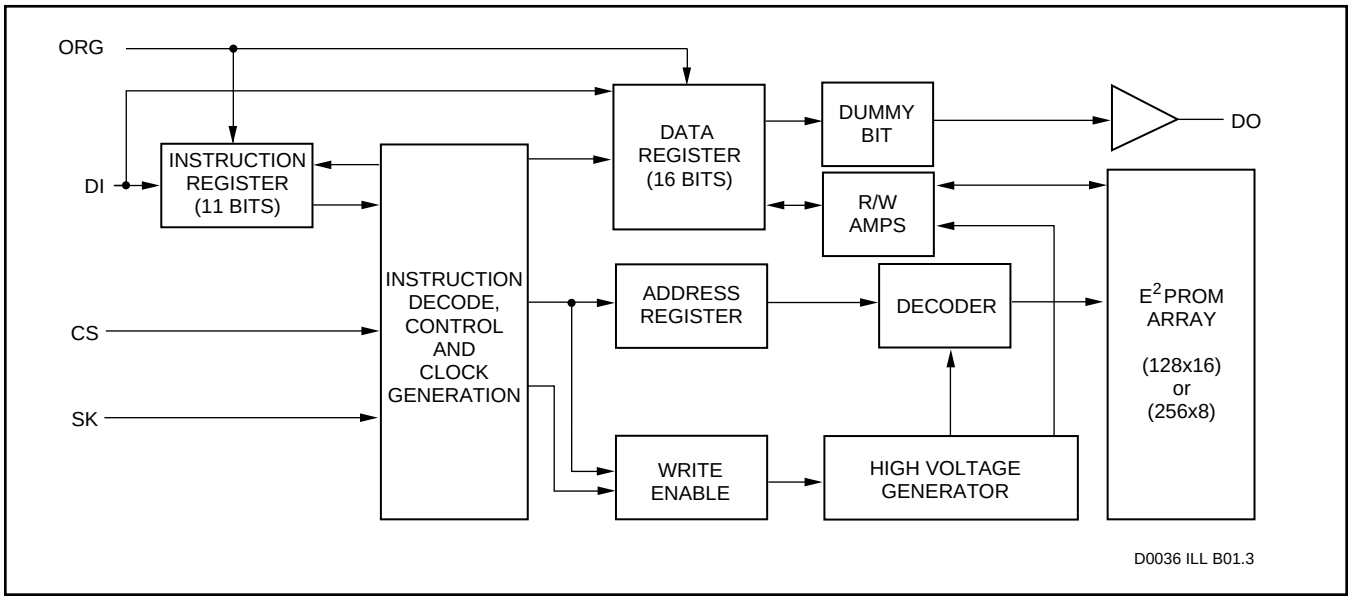
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
NC	Not Connected
ORG	Word Organization

OVERVIEW

The XL93LC56B is a cost effective 2,048-bit, nonvolatile, serial E^2PROM. It is fabricated using EXEL's advanced CMOS E^2PROM technology. The XL93LC56B provides efficient nonvolatile read/write memory arranged as 128 addresses of 16 bits each or 256 addresses of 8 bits each. Seven 11-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. A simple byte or word is written in per write instruction into the selected address location. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

BLOCK DIAGRAM



APPLICATIONS

The XL93LC56B is ideal for high volume applications requiring low power and low density storage. This device uses a cost effective, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93LC56B is designed for applications requiring up to 100,000 erase/write cycles per bit. It provides 100 years of secure data retention without power after the execution of 100,000 write cycles.

DEVICE OPERATION

The XL93LC56B is controlled by seven 11-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical “1” (the start bit). This is followed by the opcode (2 bits), the address field (8 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93LC56B will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory location into a serial shift register. (Please note that one logical “0” bit precedes the actual output data string). The output on DO changes during the LOW-TO-HIGH transitions of SK. (See Figure 2.)

Auto Increment Read Operations

In order to facilitate memory transfer operations, the XL93LC56B has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system issues a read instruction specifying a start location address. Once the addressed byte/word has been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction. See Figure 3.)

Write (WRITE)

The WRITE instruction is followed by the address and the 8 or 16 bits of data to be written. After the last data bit has been clocked in, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS, whenever CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the part is ready for another instruction. (See Figure 4.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important not to reset the READY/$\overline{\text{BUSY}}$ flag through this combination of control signals.

Write All (WRALL)

The write all (WRALL) instruction programs all memory locations with the data pattern specified in the instruction.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 5.)

Write Disable (WDS)

The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, the part powers up in the write disabled state.)

Erase

The Erase instruction (ERASE) programs the addressed memory location to all "1s." Once the address is clocked in, the falling edge of CS will initiate the internal programming cycle. After waiting a minimum 250ns, the READY/BUSY status can be monitored on DO.

Erase All (ERAL)

Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 8.)

V_{CC} Lockout (Inadvertent Write Protection)

The XL93LC56B contains a V_{CC} sensing circuit which will inhibit write operations if V_{CC} falls below VWI. For the XL93LC56B, V_{CC} = 5V±10%, the circuit will disable writes if V_{CC} is below 3.75V (typical). For the XL93LC56B-1.8, V_{CC} = 1.8V to 5.5V, the circuit will disable writes if V_{CC} is below 1.5V (typical). Therefore, in a system utilizing the XL93LC56B-1.8, close control of the system's operation should be maintained throughout the device's specified range of write capability.

XL93LC56B INSTRUCTION SET

			X16 Organization ORG=1		X8 Organization ORG=0	
Instruction	**Start Bit**	**OP Code**	**Address**	**Data**	**Address**	**Data**
READ	1	10	X(A_7-A_0)	D_n-D_0	X(A_8-A_0)	D_n-D_0
WEN (Write Enable)	1	00	11XX XXXX		11XX XXXXX	
WRITE	1	01	X(A_7-A_0)	D_{15}-D_0	X(A_8-A_0)	D_7-D_0
WRALL (Write All Registers)	1	00	01XX XXXX	D_{15}-D_0	01XX XXXXX	D_7-D_0
WDS (Write Disable)	1	00	00XX XXXX		00XX XXXXX	
ERASE	1	11	X(A_7-A_0)		X(A_8-A_0)	
ERAL (Erase All Registers)	1	00	10XX XXXX		10XX XXXXX	

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ABSOLUTE MAXIMUM RATINGS

Temperature under bias: ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... .-0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may adversely affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C

Symbol	Parameter	Conditions		XL93LC56B-1.8 1.8V -5.5V		XL93LC56B 4.5V to 5.5V		Units
				Min	Max	Min	Max	
I_{CC1}	Operating Current	CS = V_{CC} = 1.8V to 4.0V	READ		1		1	mA
	CMOS Input Levels	SK = 250KHz	WRITE		1		1.5	mA
I_{CC2}	Operating Current	CS = V_{CC} = 4.0V to 5.5V	READ		1.5		1.5	mA
	CMOS Input Levels	SK = 500KHz	WRITE		2		2	mA
I_{CC3}	Operating Current	CS = V_{CC} = 5V±10%	READ		n/a		2	mA
	CMOS Input Levels	SK = 1MHz	WRITE				3	mA
I_{SB1}	Standby Current	V_{CC} = 2V+10%			n/a		n/a	µA
I_{SB2}	Standby Current	V_{CC} = 3V+10%			1		n/a	µA
I_{SB3}	Standby Current	V_{CC} = 4V+10%			1		n/a	µA
I_{SB4}	Standby Current	V_{CC} = 5V+10%			n/a		3	µA
I_{LI}	Input Leakage	V_{IN} = 0V to V_{CC}	(CS, SK, DI)		1		1	µA
			(ORG)		10		10	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to V_{CC} CS = 0V			1		1	µA
V_{IL}	Input Low Voltage			-0.1	$0.2V_{CC}$	-0.1	0.8	V
V_{IH}	Input High Voltage			$0.8V_{CC}$	$V_{CC}^{+0.2}$	2	$V_{CC}^{+0.2}$	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA			n/a		0.4	V
V_{OH1}	Output High Voltage	I_{OH}=-400µA		n/a		2.4		V
V_{OH2}	Output Low Voltage	I_{OL}=100µA			0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH}=100µA		$V_{CC}^{-0.2}$		$V_{CC}^{-0.2}$		V
V_{WI}	Write Inhibit Threshold			n/a	n/a	2.7	4.4	V

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AC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C

Symbol	Parameter	Conditions	XL93LC56B-1.8 1.8V to 4.0V		XL93LC56B-1.8 2.7V -5.5V		XL93LC56B 4.5V to 5.5V		Units
			Min	Max	Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	250	0	500	0	1000	kHz
t_{SKH}	SK High Time		2000		1000		400		ns
t_{SKL}	SK Low Time		2000		1000		250		ns
t_{CS}	Minimum CS Low Time		1000		500		250		ns
t_{CSS}	CS Setup Time	Relative to SK	200		100		50		ns
t_{DIS}	DI Setup Time	Relative to SK	400		200		100		ns
t_{CSH}	CS Hold Time	Relative to SK	0		0		0		ns
t_{DHI}	DI Hold Time	Relative to SK	400		200		100		ns
t_{PDI}	Output Delay to “1”	AC Test		2000		1000		500	ns
t_{PDO}	Output Delay to “0”	AC Test		2000		1000		500	ns
t_{SV}	CS to Status Valid	AC Test Cl = 100pf		2000		1000		500	ns
t_{DF}	CS to DO high Z	CS = Lo to DO in Hi-Z		400		200		100	ns
t_{WP}	Write Cycle Time	CS = Low / DO = Ready		10		5		5	ms

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CAPACITANCE

T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

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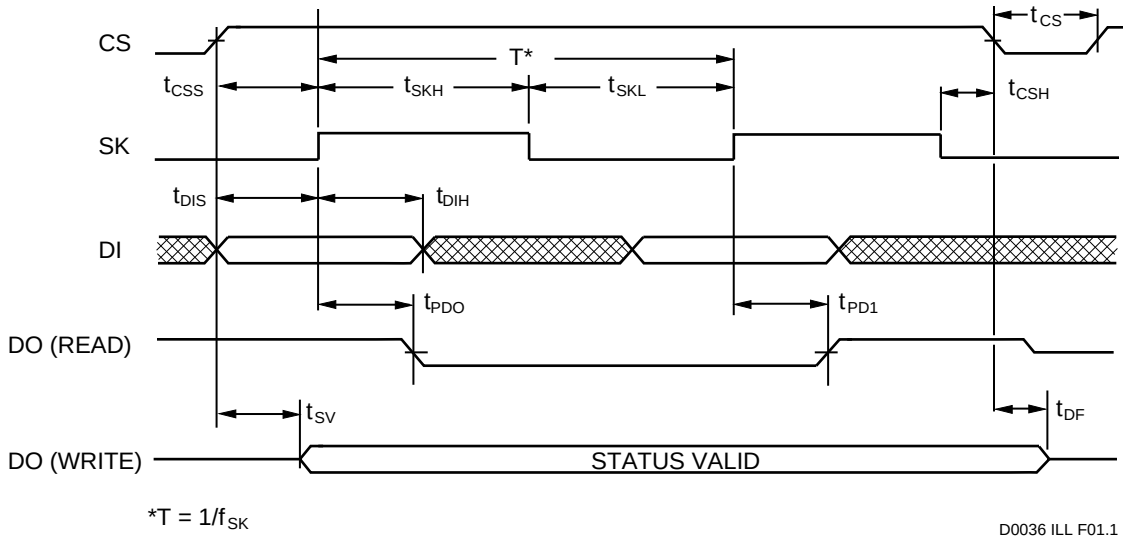


FIGURE 1. SYNCHRONOUS DATA TIMING

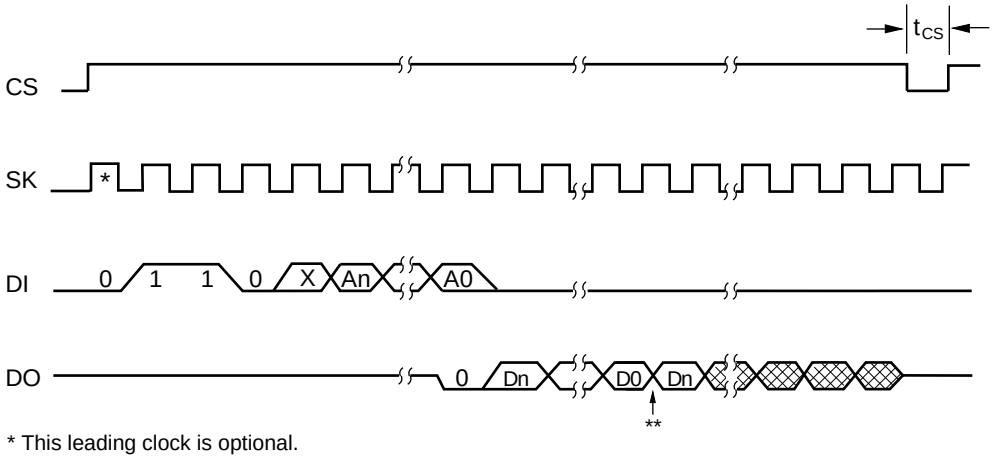
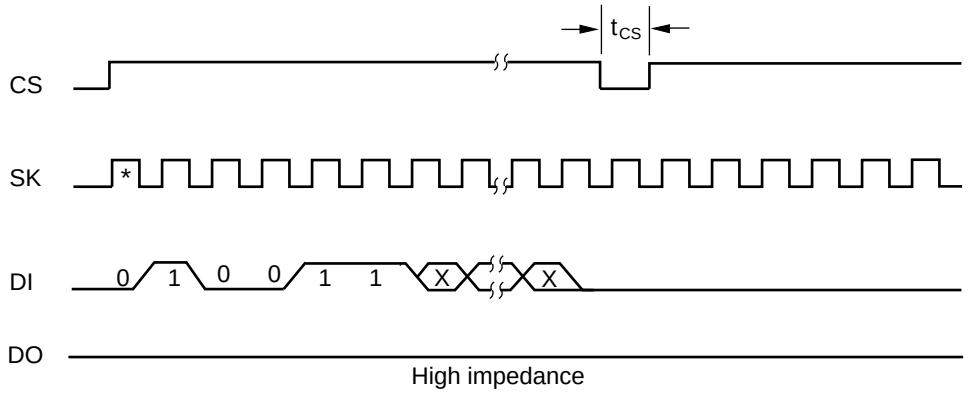


FIGURE 2. READ CYCLE TIMING



* This leading clock is optional.

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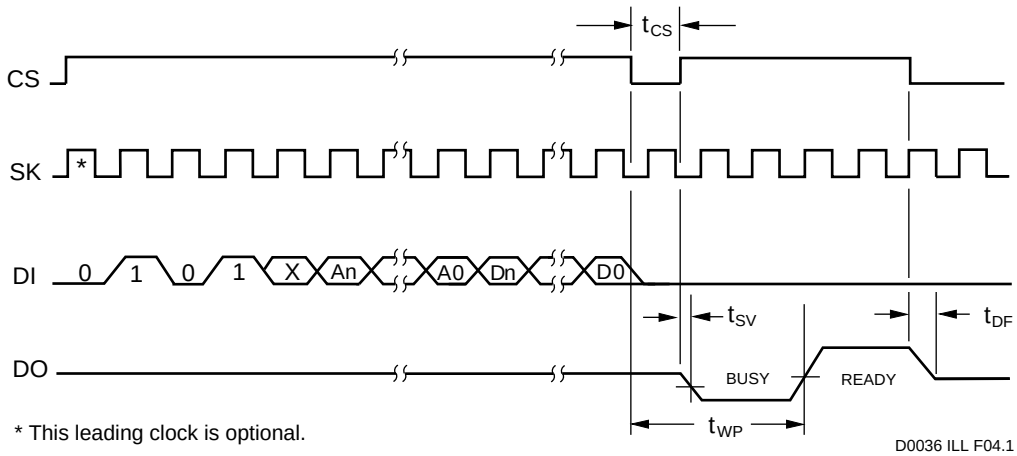
FIGURE 3. WRITE ENABLE (WEN) CYCLE TIMING



* This leading clock is optional.

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FIGURE 4. WRITE CYCLE TIMING

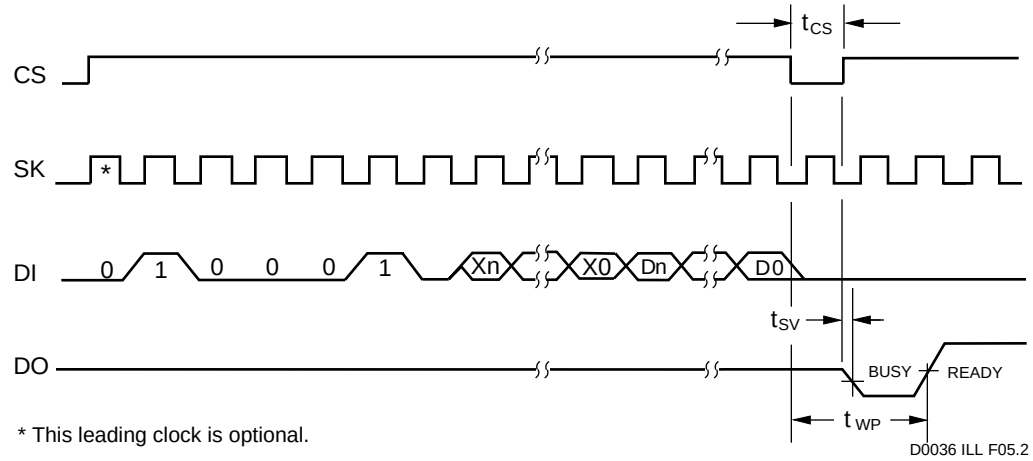


FIGURE 5. WRITE ALL (WRALL) CYCLE TIMING

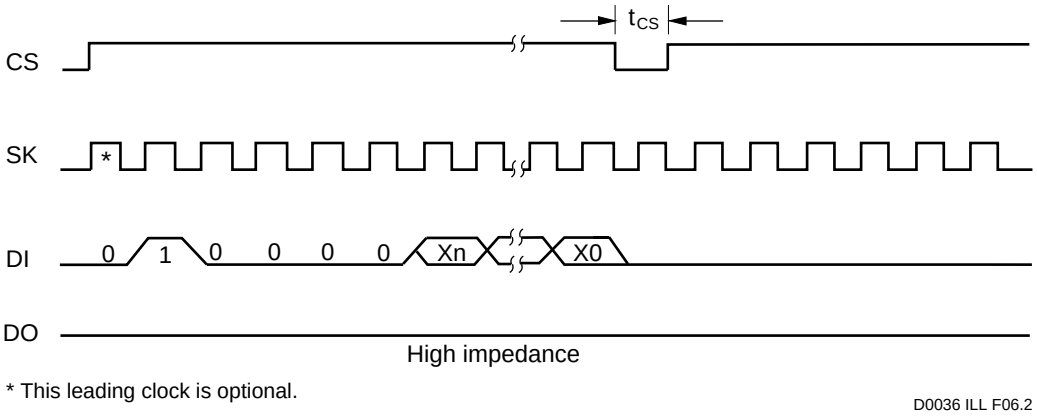
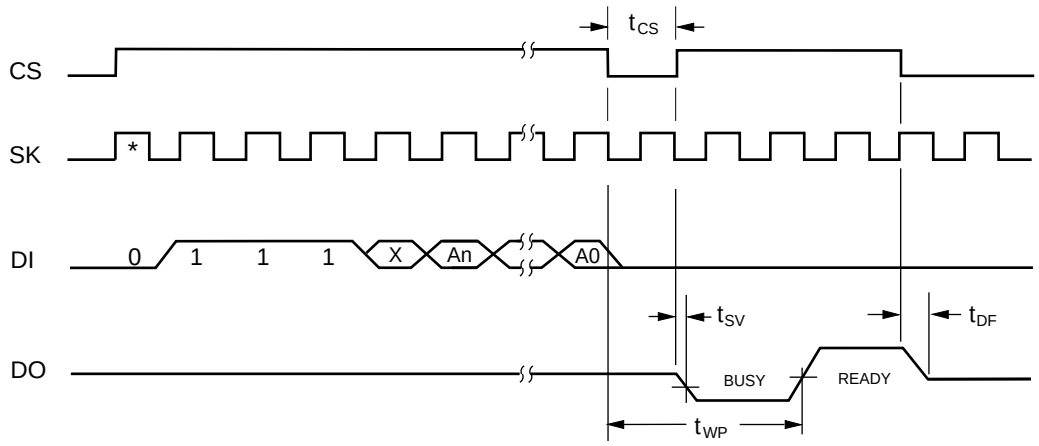


FIGURE 6. WRITE DISABLE (WDS) CYCLE TIMING



* This leading clock is optional.

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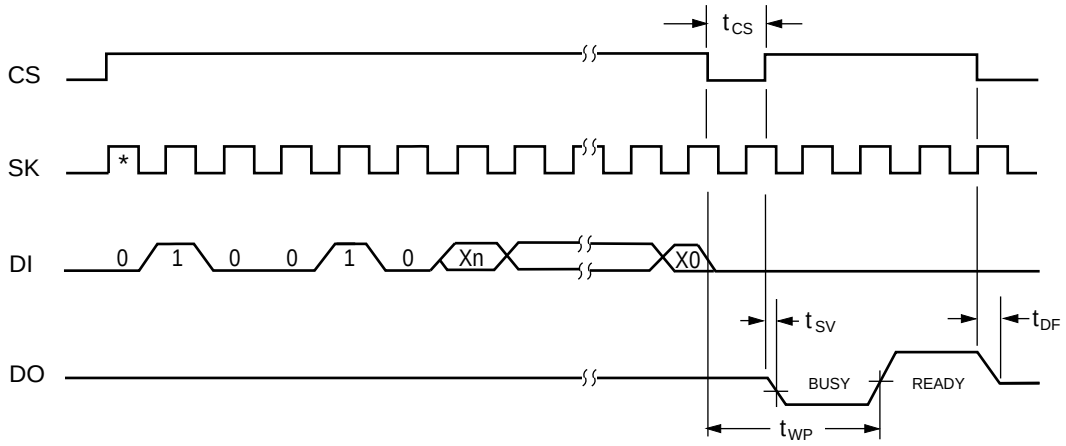
FIGURE 7. ERASE (REGISTER) CYCLE TIMING



* This leading clock is optional.

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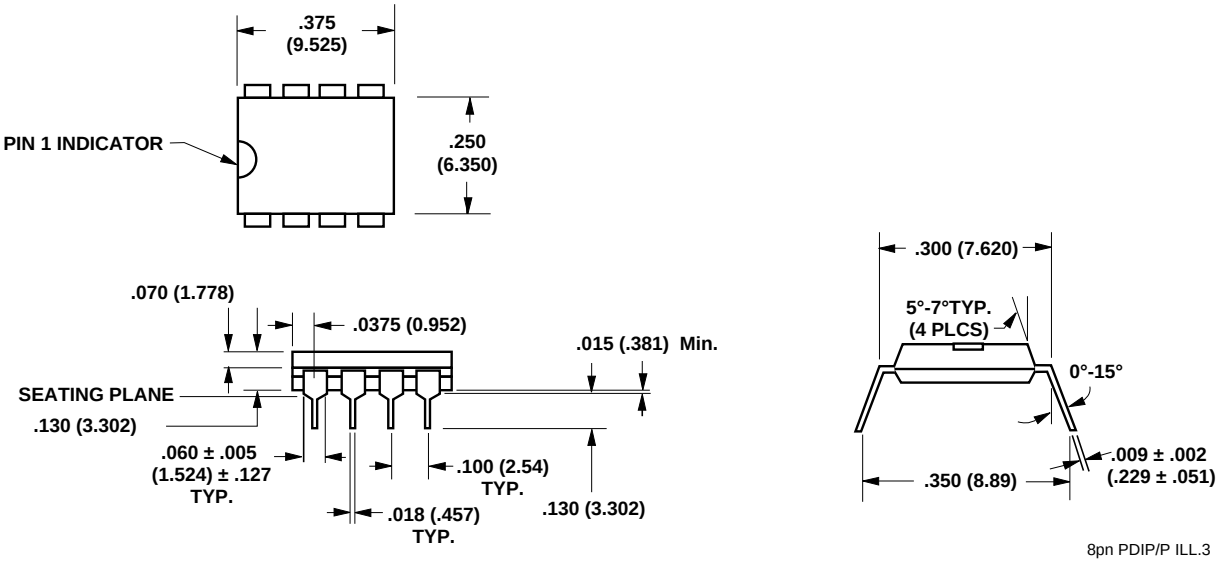
FIGURE 8. ERASE ALL (ERAL) CYCLE TIMING

PACKAGE DIAGRAMS

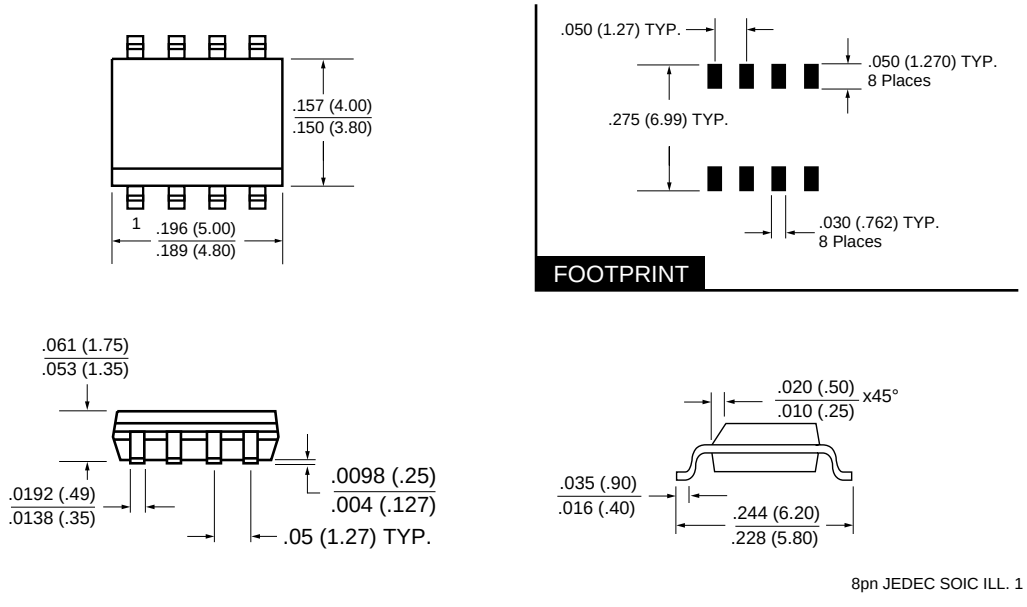
Plastic Dual-in-line (Type "P") Package (PDIP)



8pn PDIP/P ILL.3

All dimensions in inches (mm).

8 Pin SOIC (Type "Y," "RY") Package (JEDEC 150 mil body width)



8pn JEDEC SOIC ILL. 1

All dimensions in inches (mm).

* See cover page for pinout options.

ORDERING INFORMATION

Standard Configurations

Prefix Type	Part Type	Voltage	Package Range
XL	93LC56B	5V±10%, 1.8 to 5.5V	P, Y, RY

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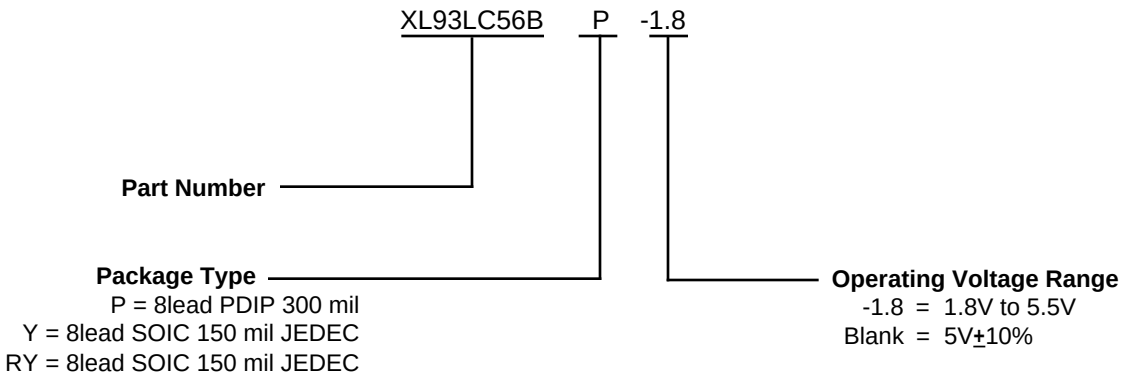
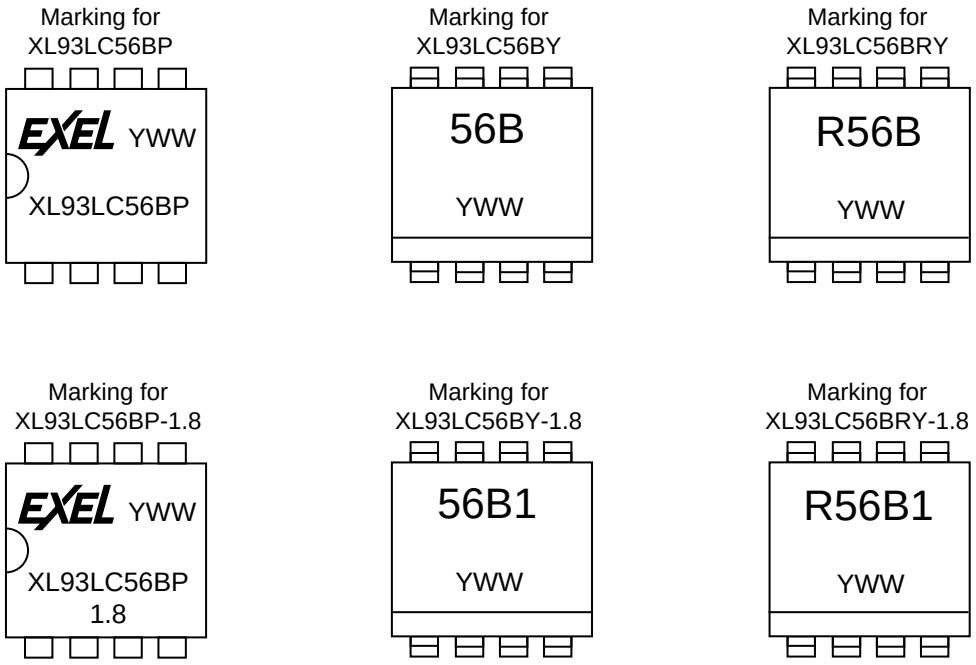
Part Numbers:



MARKING INFORMATION



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* See cover page for pinout options.

TAPE AND REEL (EMBOSSED) INFORMATION

Surface mount devices, which are normally shipped in antistatic plastic tubes, are also available mounted on embossed tape for customers using automatic placement systems. The following diagram provides general information regarding the direction of the IC's. Tape "E2" shall be designated with PIN 1 at the trail direction.