IMI4343 PHASE DETECTOR

June 1997

CMOS LSI
PLL FREQUENCY SYNTHESIZERS

PRODUCT DESCRIPTION

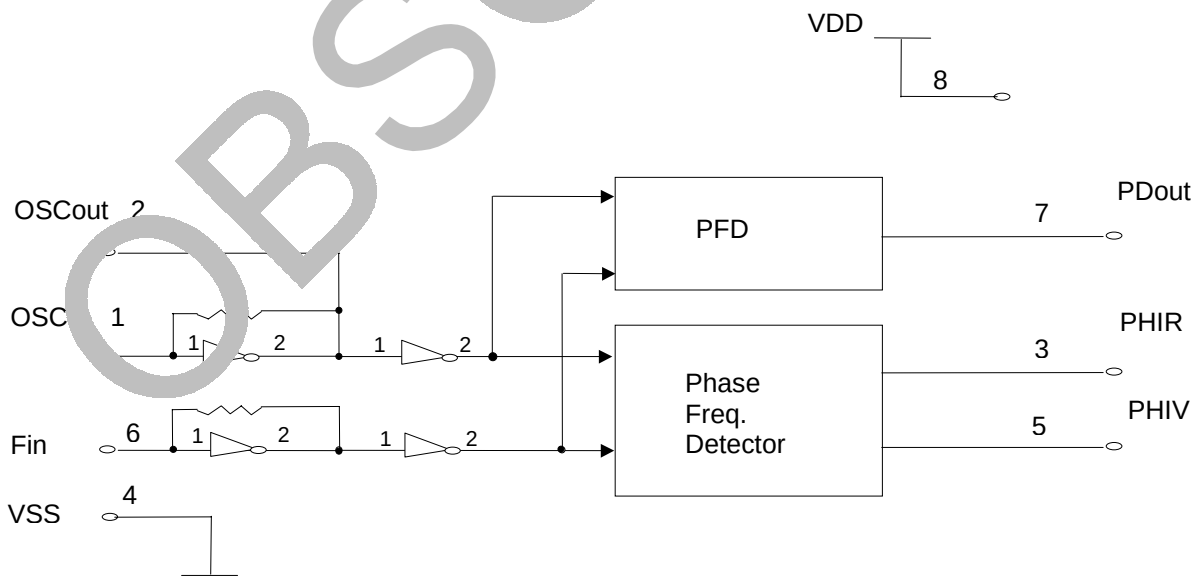
The IMI4343 is a member of a family of phase lock loop synthesizer ICs from International Microcircuits. This is a phase-frequency detector intended for use with high reference frequencies. Compatible with sinewave, ECL, TTL, and CMOS input waveforms, makes the IMI4343 extremely versatile in PLL applications.

The IMI4343 has a Type IV phase frequency detector which has eliminated by design the inherent dead zone which causes crossover distortion at the critical center lock point. The IMI circuitry enables consistent low noise loop designs using the simple single ended charge pump output. Differential charge pump outputs are also provided for those who require a more sophisticated differential active loop filter design.

PRODUCT FEATURES

- Useful input frequency > 50 MHz
- Low power consumption CMOS
- -163 dBc/Hz total phase noise floor
- No dead zone, by desi
- High gain differenti outputs
- 380 µA Current M de Ch ge Pump
- Unambiguou PLL a isition
- Zero deg phase diffe nc at lock
- ECL co patib inputs when AC coupled
- Si wave inputs w en AC coupled
- TL, CM OS inputs can be DC coupled
- On-c p 3rd overtone reference oscillator
- Sm ll SO-8 ackage for SMT available
- 3-volt 5-volt characterizations

BLOCK DIAGRAM



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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V to 7V
Voltage Relative to VDD	0.3V
Storage Temperature:	-65ºC to 150ºC
Ambient Temperature:	-45ºC to 85 ºC
Recommended Operating Range:	2.7V - 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

PIN DESCRIPTIONS

PIN NO.	NAME	DESCRIPTION
1	OSCin	This input is self biased and is designed to be AC coupled for low level sinewave signals.
2	OSCout	Reference signal output can be used in conjunction with OSCin to form an internal crystal oscillator.
6	Fin	This input is intended to be AC coupled. DC coupling can be used for CMOS logic level input signals.
4	VSS	Circuit ground.
8	VDD	Circuit positive power supply.
3	PHIR	Phase detector output. This signal goes LOW when the feedback frequency is too low.
5	PHIV	Phase detector output. This signal goes LOW when the feedback frequency is too high.
7	Pdout	Single-ended charge pump output, usually used with passive loop filters. This signal operates according to the following: þ Frequency fv>fr at the phase detector: negative pulses. þ Frequency fv<fr at the phase detector: positive pulses. þ Frequency fv = fr at the phase detector: high-impedance state.

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PLL OPERATING CHARACTERISTICS

VDD = 5 VOLTS

Characteristics		Symbol		-40ºC		25ºC			85ºC		Units	Conditions
				Min	Max	Min	Typ	Max	Min	Max		
Dynamic	Operating Frequency	fin, fosc	Sine		50			50		45	MHz	
			Square		50			50		45	MHz	
	Phase Noise Floor	PDNF					-160				dBc/Hz	
	Pin Capacitance	Cin		-	10	-	6	10	-	10	pF	
		Cout		-	10	-	6	10	-	10	pF	
Static	Input Voltages	VIL		1	1.5	-	2.75	1.5		1.5	Vdc	
		VIH		3.5	-	3.5	2.75	-	3.5	-		
	Output Voltages	VOL		-	0.05	-	0.0	0.05	-	0.05	Vdc	
		VOH		4.95	-	4.95	5.0	-	4.95	-		
	Output Current	IOL	Logic	2.4	-	2.0	2.8	-	1.6	-		
			OSCout	1.2	-	1.0	1.4	-	0.8	-	mA	VOL = 0.40
		IOH	Logic	-2.4	-	-2.0	-2.8	-	-1.6	-	mA	VOH = 4.0
			OSCout	-1.2	-	-1.0	-1.4	-	-0.8	-	mA	VOH = 4.0
	Charge Pump	Icp					380				µA	Vdd = 5V @ 25°C
	Supply Currents	IDD			10	-	7	10	-	10	mA	fosc=fin-10 MHz
		ISB		-	150	-	40	150	-	150	µA	fosc=fin=0

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PLL FREQUENCY SYNTHESIZERS

PLL OPERATING CHARACTERISTICS

VDD = 3 VOLTS

Characteristics		Symbol		-40ºC		25ºC			70ºC		Unit	Conditions
				Min	Max	Min	Typ	Max	Min	Max		
Dynamic	Operating Frequency	fin, fosc	Sine		50		-	50		45	MHz	
			Sine		50		-	50		45	MHz	
	Phase Noise Floor	PDNF					-155				dBc/Hz	
	Pin Capacitance	Cin		-	10	-	6	10			pF	
		Cout		-	10	-	6	10			pF	
Static	Input Voltages	VIL		-	0.9	-	1.35	0.9	-	1.5	Vdc	
		VIH		2.1	-	2.1	1.65	-				
	Output Voltages	VOL		-	0.05	-	0.0	0.05	-	0.[illegible]	Vdc	
		VOH		2.95	-	2.95	3.0	-	2.95	-		
	Output Current	IOL	Logic	1.6	-	1	2.0					
			OSCout	0.8	-	[illegible]	1.0	-			mA	VOL = 0.30
		IOH	Logic	-1.6	-	-1	-2.0	-			mA	VOH = 2.4
			OSCout	-1.6	-	-0.7	-1.0	-			mA	VOL = 2.4
	Charge Pump	Icp					240				µA	Vdd = 3V @ 25°C
	Supply Currents	IDD		-	5	-	3	5	-	5	mA	fosc=fin-10 MHz
		ISB		-	150		40	150			µA	fosc=fin=0

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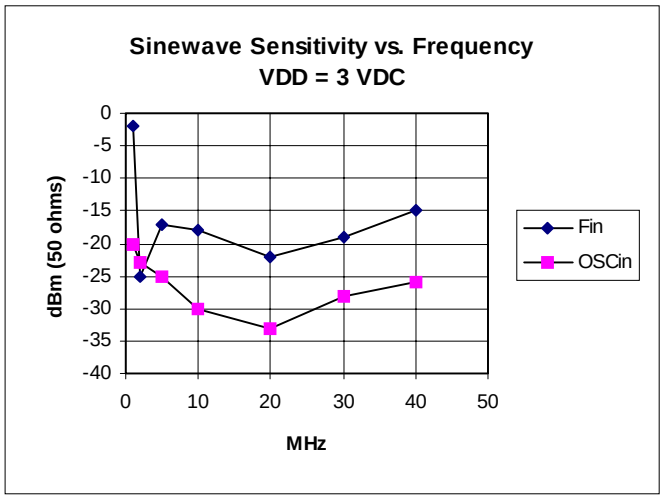

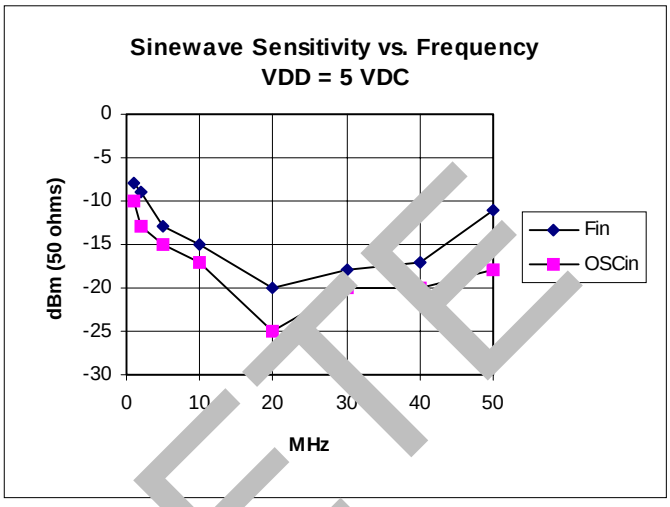

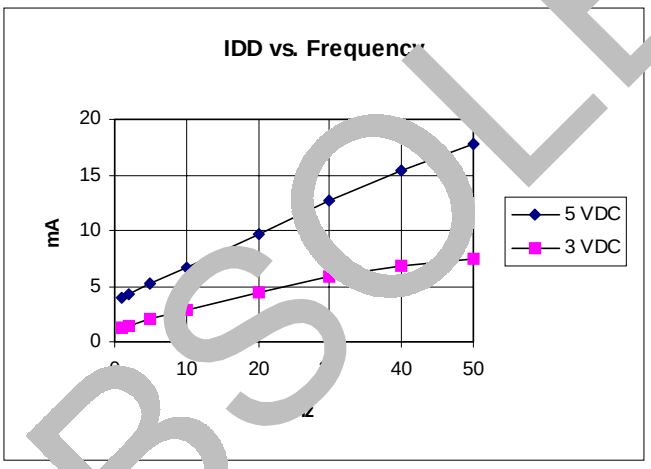

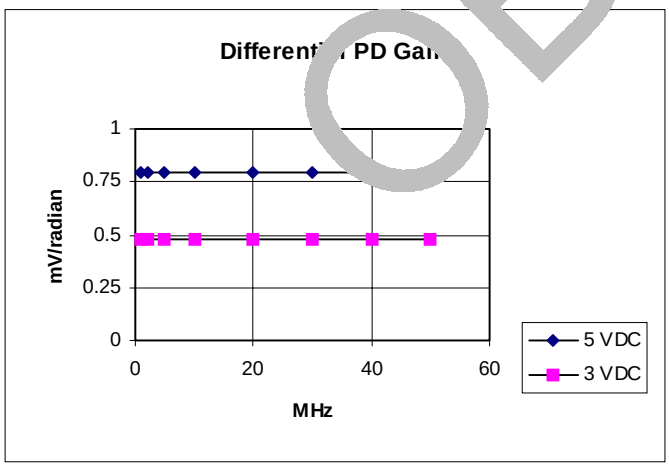

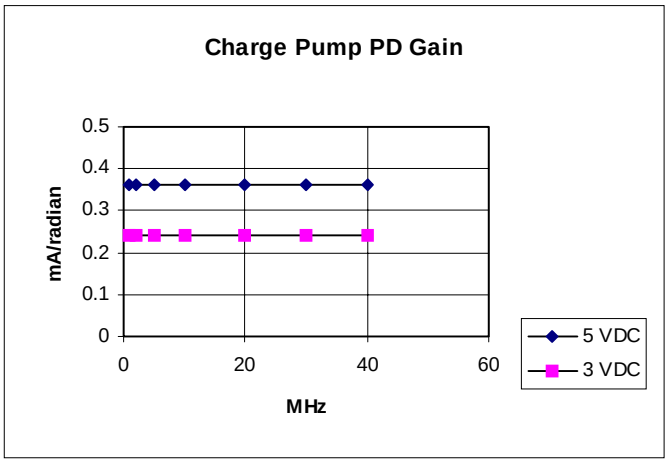

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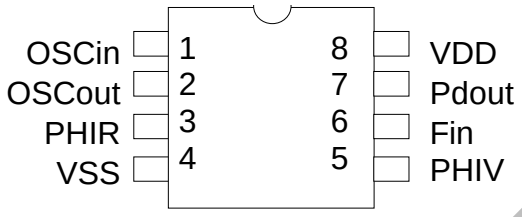
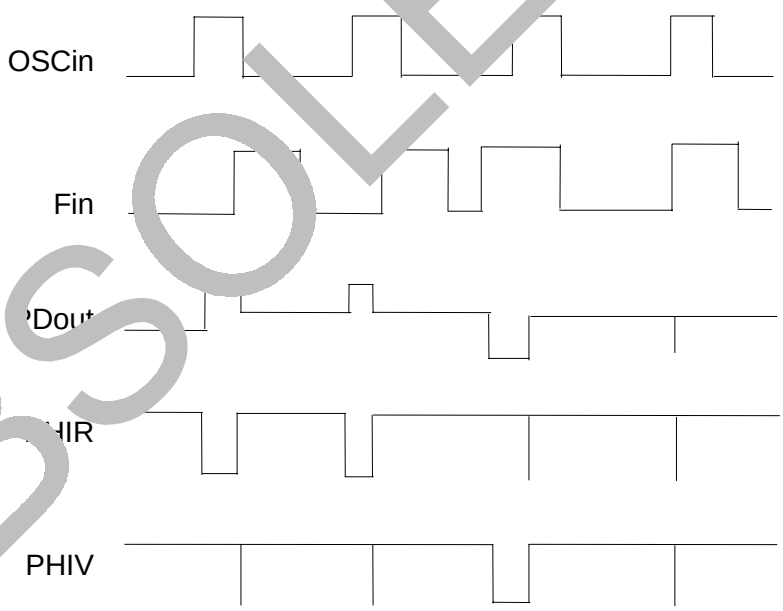
CONNECTION DIAGRAM



PHASE DETECTOR OUTPUT WAVEFORMS



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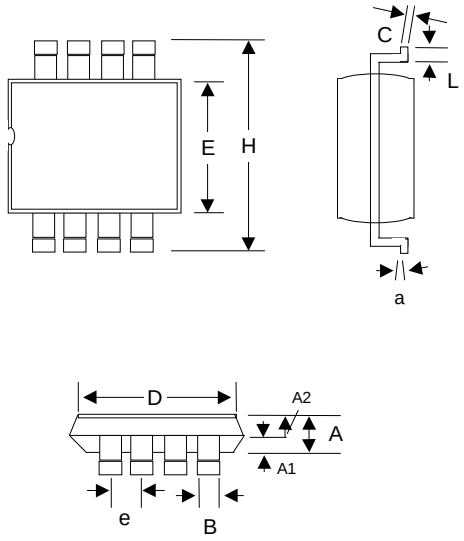
PACKAGE DRAWING AND DIMENSIONS



SOP PACKAGE

8-PIN OUTLINE DIMENSIONS

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	2.03	-	-	0.080	-
A_1	0.0020	0.009	0.0015	0.060	0.22	0.38
A2	0.090	0.092	0.111	2.29	2.34	2.39
B	0.35	0.40	0.4	0.0	.016	.018
C	-	-	-		.008	-
D	5.15	5.25	5.35	0.205	0.207	0.210
E	5.20	5.30	5.40	0.205	0.210	0.213
e		0.050 BSC			1.27 BSC	
H	7.70	7.90	8.10	0.303	0.310	0.318
a						
L	0.5	0.65	0.8	0.020	0.025	0.031

ORDERING INFORMATION

Part Number	Package Type	Production Flow
IMI4343xYB	8-Pin SOP	Industrial, -45°C to +85°C

Note: The "x" following the IMI Device Number denotes the device revision. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: 4343xYB
Date Code
Lot #

IMI4343xYB

Flow
B = Industrial, -45°C to +85°C

Package
Y = SOP

Revision

IMI Device Number