Integrated Circuit Systems, Inc.

ICS950219

Preliminary Product Preview

Programmable Timing Control Hub™ for P4™

Recommended Application:

CK-408 clock with driven mode only for Brookdale chipset with P4 processor.

Output Features:

- 3 - Pairs of differential CPU clocks (differential current mode)
- 4 - 3V66 @ 3.3V
- 10 - PCI @ 3.3V
- 1 - 48MHz @ 3.3V
- 24-48 MHz selectable output @ 3.3V
- 2 - REF @ 3.3V, 14.318MHz

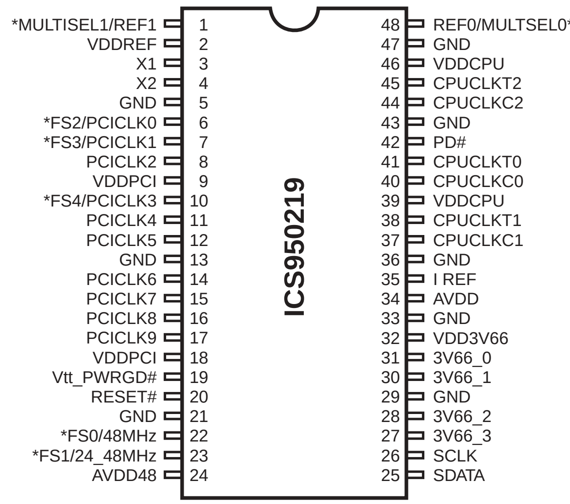
Features/Benefits:

- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I^{2}C Index read/write and block read/write operations.
- Uses external 14.318MHz crystal.

Key Specifications:

- CPU Output Jitter <150ps
- 3V66 Output Jitter <250ps
- CPU Output Skew <100ps

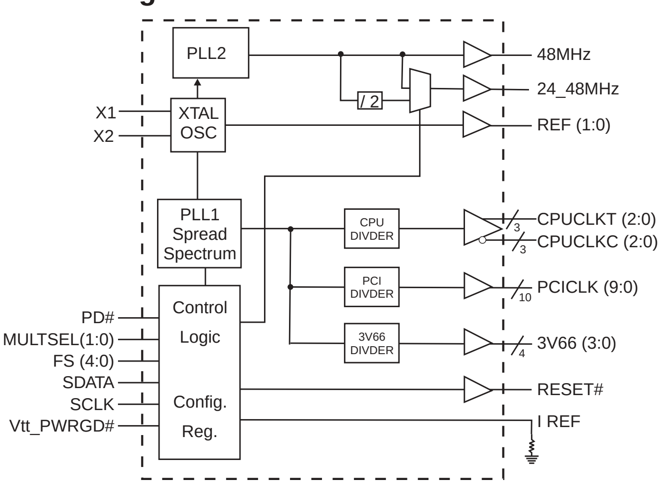
Pin Configuration



48-Pin 300-mil SSOP

* Internal Pull-up resistor of 120K to VDD

Block Diagram



Frequency Table

Bit2	Bit7	Bit6	Bit5	Bit4	CPUCLK MHz	3V66 MHz	PCICLK MHz
FS4	FS3	FS2	FS1	FS0			
0	0	0	0	0	102.00	68.00	34.00
0	0	0	0	1	105.00	70.00	35.00
0	0	0	1	0	108.00	72.00	36.00
0	0	0	1	1	111.00	74.00	37.00
0	0	1	0	0	114.00	76.00	38.00
0	0	1	0	1	117.00	78.00	39.00
0	0	1	1	0	120.00	80.00	40.00
0	0	1	1	1	123.00	82.00	41.00
0	1	0	0	0	126.00	72.00	36.00
0	1	0	0	1	130.00	74.30	37.10
0	1	0	1	0	136.00	68.00	34.00
0	1	0	1	1	140.00	70.00	35.00
0	1	1	0	0	144.00	72.00	36.00
0	1	1	0	1	148.00	74.00	37.00
0	1	1	1	0	152.00	76.00	38.00
0	1	1	1	1	156.00	78.00	39.00
1	0	0	0	0	160.00	80.00	40.00
1	0	0	0	1	164.00	82.00	41.00
1	0	0	1	0	166.66	66.66	33.33
1	0	0	1	1	170.00	68.00	34.00
1	0	1	0	0	175.00	70.00	35.00
1	0	1	0	1	180.00	72.00	36.00
1	0	1	1	0	185.00	74.00	37.00
1	0	1	1	1	190.00	76.00	38.00
1	1	0	0	0	66.80	66.80	33.40
1	1	0	0	1	100.20	66.80	33.40
1	1	0	1	0	133.60	66.80	33.40
1	1	0	1	1	200.40	66.80	33.40
1	1	1	0	0	66.66	66.66	33.33
1	1	1	0	1	100.00	66.66	33.33
1	1	1	1	0	200.00	66.66	33.33
1	1	1	1	1	133.33	66.66	33.33

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General Description

The **ICS950219** is a single chip clock solution for desktop designs using the Intel Brookdale chipset with PC133 or DDR memory. It provides all necessary clock signals for such a system.

The **ICS950219** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). ICS is the first to introduce a whole product line which offers full programmability and flexibility on a single clock device. This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. TCH also incorporates ICS's Watchdog Timer technology and a reset feature to provide a safe setting under unstable system conditions. M/N control can configure output frequency with resolution up to 0.1MHz increment. With all these programmable features ICS's, TCH makes mother board testing, tuning and improvement very simple.

Power Groups

Pin Number		**Description**
AVDD	GND	
2	47	REF output, Crystal
24	21	48MHz fixed, Fixed PLL
39	43	CPU Outputs, CPU PLL, CPU Master Clock,
VDD	GND	--
9, 18	5, 13	PCI outputs
32	29	3V66 outputs
46	36	CPU Outputs, IREF, MULTSEL

Pin Description

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	MULTSEL1 *	IN	3.3V LVTTL input for selecting the current multiplier for CPU outputs.
	REF1	OUT	3.3V, 14.318MHz reference clock output.
2, 9, 18, 24, 32, 39, 46	VDD	PWR	3.3V power supply
3	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2
4	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF)
5, 13, 21, 29, 36, 43, 47	GND	PWR	Ground pins for 3.3V supply
6	FS2 *	IN	Logic input frequency select bit. Input latched at power on.
	PCICLK0	OUT	3.3V PCI clock output
7	FS3 *	IN	Logic input frequency select bit. Input latched at power on.
	PCICLK1	OUT	3.3V PCI clock output
10	FS4 *	IN	Logic input frequency select bit. Input latched at power on.
	PCICLK3	OUT	3.3V PCI clock output
17, 16, 15, 14, 12, 11, 8	PCICLK (9:4, 2)	OUT	3.3V PCI clock outputs
19	Vtt_PWRGD#	IN	This 5V tolerant LVTTL input is a level sensitive strobe used to determine when FS (4:0) and MULTISEL inputs are valid and are ready to be sampled (active low)
20	RESET#	OUT	Real time system reset signal for frequency value or watchdog timmer timeout. This signal is active low.
27, 28, 30, 31	3V66 (3:0)	OUT	3.3V Fixed 66MHz clock outputs for HUB
22	FS0 *	IN	Logic input frequency select bit. Input latched at power on.
	48MHz	OUT	3.3V Fixed 48MHz clock output.
23	FS1 *	IN	Logic input frequency select bit. Input latched at power on.
	24_48MHz	OUT	Selectable 24 or 48 MHz output
25	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
26	SCLK	IN	Clock pin for I^2C circuitry 5V tolerant
33	GND	PWR	Ground for CORE PLL
34	AVDD	PWR	Power for CORE PLL 3.3V nominal
35	I REF	OUT	This pin establishes the reference current for the CPUCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.
42	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
44, 40, 37	CPUCLKC (2:0)	OUT	"Complementory" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
45, 41, 38	CPUCLKT (2:0)	OUT	"True" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
48	MULTSEL0 *	IN	3.3V LVTTL input for selecting the current multiplier for CPU outputs.
	REF0	OUT	3.3V, 14.318MHz reference clock output.

* Internal pull-up resistor of 120K to VDD.

Maximum Allowed Current

Condition	Max 3.3V supply consumption Max discrete cap loads, Vdd = 3.465V All static inputs = Vdd or GND
Powerdown Mode (PWRDWN# = 0)	40mA
Full Active	360mA

CPUCLK Swing Select Functions

MULTSEL0	MULTSEL1	Board Target Trace/Term Z	Reference R, Iref= Vdd/(3*Rr)	Output Current	Voh @ Z, Iref=2.32mA
0	0	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 5*Iref	0.71V @ 60
0	0	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 5*Iref	0.59V @ 50
0	1	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 6*Iref	0.85V /2 60
0	**1**	**50 ohms**	**Rr = 475 1% Iref = 2.32mA**	**Ioh = 6*Iref**	**0.71V @ 50**
1	0	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 4*Iref	0.56V @ 60
1	0	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 4*Iref	0.47V @ 50
1	**1**	**60 ohms**	**Rr = 475 1% Iref = 2.32mA**	**Ioh = 7*Iref**	**0.99V @ 60**
1	1	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 7*Iref	0.82V @ 50
0	0	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 5*Iref	0.75V @ 30
0	0	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 5*Iref	0.62V @ 20
0	1	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 6*Iref	0.90V @ 30
0	1	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 6*Iref	0.75V @ 20
1	0	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 4*Iref	0.60 @ 20
1	0	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 4*Iref	0.5V @ 20
1	1	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 7*Iref	1.05V @ 30
1	1	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 7*Iref	0.84V @ 20

General I^2C serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1*** (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)		X Byte	ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		X Byte	ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

*See notes on the following page.

Byte 0: Functionality and frequency select register (Default=0)

Bit	Description									PWD
	Bit2	Bit7	Bit6	Bit5	Bit4	CPUCLK MHz	3V66 MHz	PCICLK MHz	Spread %	
	FS4	FS3	FS2	FS1	FS0					
Bit (2,7:4)	0	0	0	0	0	102.00	68.00	34.00	+/-0.25% Center spread	Note 1
	0	0	0	0	1	105.00	70.00	35.00	+/-0.25% Center spread	
	0	0	0	1	0	108.00	72.00	36.00	+/-0.25% Center spread	
	0	0	0	1	1	111.00	74.00	37.00	+/-0.25% Center spread	
	0	0	1	0	0	114.00	76.00	38.00	+/-0.25% Center spread	
	0	0	1	0	1	117.00	78.00	39.00	+/-0.25% Center spread	
	0	0	1	1	0	120.00	80.00	40.00	+/-0.25% Center spread	
	0	0	1	1	1	123.00	82.00	41.00	+/-0.25% Center spread	
	0	1	0	0	0	126.00	72.00	36.00	+/-0.25% Center spread	
	0	1	0	0	1	130.00	74.30	37.10	+/-0.25% Center spread	
	0	1	0	1	0	136.00	68.00	34.00	+/-0.25% Center spread	
	0	1	0	1	1	140.00	70.00	35.00	+/-0.25% Center spread	
	0	1	1	0	0	144.00	72.00	36.00	+/-0.25% Center spread	
	0	1	1	0	1	148.00	74.00	37.00	+/-0.25% Center spread	
	0	1	1	1	0	152.00	76.00	38.00	+/-0.25% Center spread	
	0	1	1	1	1	156.00	78.00	39.00	+/-0.25% Center spread	
	1	0	0	0	0	160.00	80.00	40.00	+/-0.25% Center spread	
	1	0	0	0	1	164.00	82.00	41.00	+/-0.25% Center spread	
	1	0	0	1	0	166.60	66.66	33.33	+/-0.25% Center spread	
	1	0	0	1	1	170.00	68.00	34.00	+/-0.25% Center spread	
	1	0	1	0	0	175.00	70.00	35.00	+/-0.25% Center spread	
	1	0	1	0	1	180.00	72.00	36.00	+/-0.25% Center spread	
	1	0	1	1	0	185.00	74.00	37.00	+/-0.25% Center spread	
	1	0	1	1	1	190.00	76.00	38.00	+/-0.25% Center spread	
	1	1	0	0	0	66.80	66.80	33.40	+/-0.25% Center spread	
	1	1	0	0	1	100.20	66.80	33.40	+/-0.25% Center spread	
	1	1	0	1	0	133.60	66.80	33.40	+/-0.25% Center spread	
	1	1	0	1	1	200.40	66.80	33.40	+/-0.25% Center spread	
	1	1	1	0	0	66.66	66.66	33.33	0 to -0.5% Down spread	
	1	1	1	0	1	100.00	66.66	33.33	0 to -0.5% Down spread	
	1	1	1	1	0	200.00	66.66	33.33	0 to -0.5% Down spread	
	1	1	1	1	1	133.33	66.66	33.33	0 to -0.5% Down spread	
Bit 3	0 - Frequency is selected by hardware select, latched inputs 1 - Frequency is selected by Bit 2,7:4									0
Bit 1	0 - Normal 1 - Spread spectrum enable									0
Bit 0	0 - Watch dog safe frequency will be selected by latch inputs 1 - Watch dog safe frequency will be programmed by Byte 10 bit (4:0)									0

Notes:

1. Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

Byte 1: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit7	45,44	1	CPUT/C2
Bit6	38,37	1	CPUT/C1
Bit5	41,40	1	CPUT/C0
Bit4	-	X	FS4 Read back
Bit3	-	X	FS3 Read back
Bit2	-	X	FS2 Read back
Bit1	-	X	FS1 Read back
Bit0	-	X	FS0 Read back

Byte 2: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit7	-	1	Reserved
Bit6	17	1	PCICLK_9
Bit5	16	1	PCICLK_8
Bit4	15	1	PCICLK_7
Bit3	14	1	PCICLK_6
Bit2	12	1	PCICLK_5
Bit1	11	1	PCICLK_4
Bit0	10	1	PCICLK_3

Byte 3: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit7	23	1	48MHz_1
Bit6	22	1	48MHz_0
Bit5	-	1	Reset gear shift detect 1 = Enable, 0 = Disable
Bit4	-	X	Reserved
Bit3	-	0	Sel 24_48 MHz; 0 = 24 MHz, 1 = 48 MHz
Bit2	8	1	PCICLK_2
Bit1	7	1	PCICLK_1
Bit0	6	1	PCICLK_0

Byte 4: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	-	X	MultiSEL0 (read back)
Bit 6	-	X	MultiSEL1 (Read back)
Bit 5	31	1	3V66-0
Bit 4	30	1	3V66-1
Bit 3	48	1	REF0
Bit 2	1	1	REF1
Bit 1	27	1	3V66_3
Bit 0	28	1	3V66_2

Notes:

1. PWD = Power on Default
2. For disabled clocks, they stop low for single ended clocks. Differential CPU clocks stop with CPUCLKT at high, CPUCLKC off, and external resistor termination will bring CPUCLKC low.

Byte 5: Programming Edge Rate
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	X	1	(Reserved)
Bit 5	X	1	(Reserved)
Bit 4	X	1	(Reserved)
Bit 3	X	1	(Reserved)
Bit 2	X	1	(Reserved)
Bit 1	X	1	Async. 3V66 control bit 0 : 3V66 / PCI = 64/32 MHz asynchronous with CPU 1 : 3V66 / PCI = 66.6/33.3 MHz synchronous with CPU
Bit 0	X	0	(Reserved)

Byte 6: Vendor ID Register
(1 = enable, 0 = disable)

Bit	Name	PWD	Description
Bit 7	Revision ID Bit3	X	Revision ID values will be based on individual device's revision
Bit 6	Revision ID Bit2	X	
Bit 5	Revision ID Bit1	X	
Bit 4	Revision ID Bit0	X	
Bit 3	Vendor ID Bit3	0	(Reserved)
Bit 2	Vendor ID Bit2	0	(Reserved)
Bit 1	Vendor ID Bit1	0	(Reserved)
Bit 0	Vendor ID Bit0	1	(Reserved)

Byte 7: Revision ID and Device ID Register

Bit	Name	PWD	Description
Bit 7	Device ID7	0	Device ID values will be based on individual device "28H" in this case.
Bit 6	Device ID6	0	
Bit 5	Device ID5	1	
Bit 4	Device ID4	0	
Bit 3	Device ID3	1	
Bit 2	Device ID2	0	
Bit 1	Device ID1	0	
Bit 0	Device ID0	0	

Byte 8: Byte Count Read Back Register

Bit	Name	PWD	Description
Bit 7	Byte7	0	Note: Writing to this register will configure byte count and how many bytes will be read back, default is $0F_H$ = 15 bytes.
Bit 6	Byte6	0	
Bit 5	Byte5	0	
Bit 4	Byte4	0	
Bit 3	Byte3	1	
Bit 2	Byte2	1	
Bit 1	Byte1	1	
Bit 0	Byte0	1	

Byte 9: Watchdog Timer Count Register

Bit	Name	PWD	Description
Bit 7	WD7	0	The decimal representation of these 8 bits correspond to X • 290ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 8 • 290ms = 2.3 seconds.
Bit 6	WD6	0	
Bit 5	WD5	0	
Bit 4	WD4	0	
Bit 3	WD3	1	
Bit 2	WD2	0	
Bit 1	WD1	0	
Bit 0	WD0	0	

Byte 10: Programming Enable bit 8 Watchdog Control Register

Bit	Name	PWD	Description
Bit 7	Program Enable	0	Programming Enable bit 0 = no programming. Frequencies are selected by HW latches or Byte0 1 = enable all I²C programing.
Bit 6	WD Enable	0	Watchdog Enable bit. This bit will over write WDEN latched value. 0 = disable, 1 = Enable.
Bit 5	WD Alarm	0	Watchdog Alarm Status 0 = normal 1= alarm status
Bit 4	SF4	0	Watchdog safe frequency bits. Writing to these bits will configure the safe frequency corrsponding to Byte 0 Bit 2, 7:4 table
Bit 3	SF3	1	
Bit 2	SF2	0	
Bit 1	SF1	0	
Bit 0	SF0	0	

Byte 11: VCO Frequency M Divider (Reference divider) Control Register

Bit	Name	PWD	Description
Bit 7	Ndiv 8	X	N divider bit 8
Bit 6	Mdiv 6	X	The decimal respresentation of Mdiv (6:0) correspsod to the reference divider value. Default at power up is equal to the latched inputs selection.
Bit 5	Mdiv 5	X	
Bit 4	Mdiv 4	X	
Bit 3	Mdiv 3	X	
Bit 2	Mdiv 2	X	
Bit 1	Mdiv 1	X	
Bit 0	Mdiv 0	X	

Byte 12: VCO Frequency N Divider (VCO divider) Control Register

Bit	Name	PWD	Description
Bit 7	Ndiv 7	X	The decimal representation of Ndiv (8:0) correspond to the VCO divider value. Default at power up is equal to the latched inputs selecton. Notice Ndiv 8 is located in Byte 11.
Bit 6	Ndiv 6	X	
Bit 5	Ndiv 5	X	
Bit 4	Ndiv 4	X	
Bit 3	Ndiv 3	X	
Bit 2	Ndiv 2	X	
Bit 1	Ndiv 1	X	
Bit 0	Ndiv 0	X	

Byte 13: Spread Spectrum Control Register

Bit	Name	PWD	Description
Bit 7	SS 7	X	The Spread Spectrum (12:0) bit will program the spread precentage. Spread precent needs to be calculated based on the VCO frequency, spreading profile, spreading amount and spread frequency. It is recommended to use ICS software for spread programming. Default power on is latched FS divider.
Bit 6	SS 6	X	
Bit 5	SS 5	X	
Bit 4	SS 4	X	
Bit 3	SS 3	X	
Bit 2	SS 2	X	
Bit 1	SS 1	X	
Bit 0	SS 0	X	

Byte 14: Spread Spectrum Control Register

Bit	Name	PWD	Description
Bit 7	Reserved	X	Reserved
Bit 6	Reserved	X	Reserved
Bit 5	Reserved	X	Reserved
Bit 4	SS 12	X	Spread Spectrum Bit 12
Bit 3	SS 11	X	Spread Spectrum Bit 11
Bit 2	SS 10	X	Spread Spectrum Bit 10
Bit 1	SS 9	X	Spread Spectrum Bit 9
Bit 0	SS 8	X	Spread Spectrum Bit 8

Byte 15: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	CPUDIV3	X	CPU2 clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 6	CPUDIV2	X	
Bit 5	CPUDIV1	X	
Bit 4	CPUDIV0	X	
Bit 3	CPU Div 3	X	CPU(1:0) clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 2	CPU Div 2	X	
Bit 1	CPU Div 1	X	
Bit 0	CPU Div 0	X	

Byte 16: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	3V66 Div 3	X	3V66(3:2) clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 6	3V66 Div 2	X	
Bit 5	3V66 Div 1	X	
Bit 4	3V66 Div 0	X	
Bit 3	3V66 Div 3	X	3V66(1:0) clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 2	3V66 Div 2	X	
Bit 1	3V66 Div 1	X	
Bit 0	3V66 Div 0	X	

Byte 17: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	3V66(3:2)_INV	X	3V66(3:2) Phase Inversion bit
Bit 6	3V66(1:0)_INV	X	3V66(1:0) Phase Inversion bit
Bit 5	CPU_INV	X	CPUCLK_2 Phase Inversion bit
Bit 4	CPU_INV	X	CPUCLK Phase Inversion bit
Bit 3	PCI Div 3	X	PCI clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 2. Default at power up is latched FS divider.
Bit 2	PCI Div 2	X	
Bit 1	PCI Div 1	X	
Bit 0	PCI Div 0	X	

Table 1

Div (3:2) / Div (1:0)	00	01	10	11
00	/2	/4	/8	/16
01	/3	/6	/12	/24
10	/5	/10	/20	/40
11	/7	/14	/28	/56

Table 2

Div (3:2) / Div (1:0)	00	01	10	11
00	/4	/8	/16	/32
01	/3	/6	/12	/24
10	/5	/10	/20	/40
11	/9	/18	/36	/72

Byte 18: Group Skew Control Register

Bit	Name	PWD	Description
Bit 7	CPU_Skew 1	0	These 2 bits delay the CPUCLKC/T2 with respect to CPUCLKC/T (1:0) 00 = 0ps 01 = 250ps 10 = 500ps 11 =750ps
Bit 6	CPU_Skew 0	1	
Bit 5	Reserved	0	Reserved
Bit 4	Reserved	0	Reserved
Bit 3	CPU_Skew 1	0	These 2 bits delay the CPUCLKC/T (1:0) clock with respect to CPUCLKC/T2 00 = 0ps 01 = 250ps 10 = 500ps 11 = 750ps
Bit 2	CPU_Skew 0	1	
Bit 1	Reserved	0	Reserved
Bit 0	Reserved	0	Reserved

Byte 19: Group Skew Control Register

Bit	Name	PWD	Programming Sequence						
Bit 7	These 4bits control CPU-3V66(3:2)	0		0	0	0	0	0ps	Reserved
Bit 6		1		0	1	0	0	150ps	Reserved
Bit 5		0		1	0	0	0	300ps	Reserved
Bit 4		0		1	1	0	0	450ps	Reserved
Bit 3	These 4 bits control CPU-3V66(1:0)	0		1	1	0	1	600ps	Reserved
Bit 2		1		1	1	1	0	750ps	Reserved
Bit 1		0		1	1	1	1	900ps	Reserved
Bit 0		0		Reserved					Reserved

Byte 20: Group Skew Control Register

Bit	Name	PWD	Programming Sequence						
Bit 7	These 4bits control CPU-PCI(9:0)	1		0	0	0	0	0ps	Reserved
Bit 6		0		0	1	0	0	150ps	Reserved
Bit 5		0		1	0	0	0	300ps	Reserved
Bit 4		0		1	1	0	0	450ps	Reserved
Bit 3	Resreved	1		1	1	0	1	600ps	Reserved
Bit 2		0		1	1	1	0	750ps	Reserved
Bit 1		0		1	1	1	1	900ps	Reserved
Bit 0		0		Reserved					Reserved

Byte 21: Slew Rate Control Register

Bit	Name	PWD	Description
Bit 7	PCICLK_2_Slew 1	1	PCICLK2 clock slew rate control bits.
Bit 6	PCICLK_2_Slew 1	0	01 = strong:11 = normal; 10 = weak
Bit 5	PCICLK (1:0)_Slew 0	1	PCICLK(1:0) clock slew rate control bits.
Bit 4	PCICLK (1:0)_Slew 0	0	01 = strong: 11 = normal; 10 = weak
Bit 3	3V66 (3:2)_Slew 1	1	3V66 (2:1) clock slew rate control bits.
Bit 2	3V66 (3:2)_Slew 1	0	01 = strong: 11 = normal; 10 = weak
Bit 1	3V66 (1:0)_Slew 1	1	3V66 (1:0) clock slew rate control bits.
Bit 0	3V66 (1:0)_Slew 0	0	01 = strong: 11 = normal; 10 = weak

Byte 22: Slew Rate Control Register

Bit	Name	PWD	Description
Bit 7	REF Slew 1	1	REF clock slew rate control bits.
Bit 6	REF Slew 0	0	01 = strong: 11 = normal; 10 = weak
Bit 5	PCI (9:7) Slew 1	1	PCI (9:7)) clock slew rate control bits.
Bit 4	PCI (9:7) Slew 0	0	01 = strong: 11 = normal; 10 = weak
Bit 3	PCI (6:5) Slew 1	1	PCI (6:5) clock slew rate control bits.
Bit 2	PCI (6:5) Slew 0	0	01 = strong: 11 = normal; 10 = weak
Bit 1	PCI (4:3) Slew 1	1	PCI (4:3) clock slew rate control bits.
Bit 0	PCI (4:3) Slew 0	0	01 = strong: 11 = normal; 10 = weak

Byte 23: Slew Rate Control Register

Bit	Name	PWD	Description
Bit 7	Reserved	X	Reserved
Bit 6	Reserved	X	
Bit 5	Reserved	1	
Bit 4	Reserved	0	
Bit 3	48MHz Slew 1	1	48MHz clock slew rate control bits.
Bit 2	48MHz Slew 0	0	01 = strong: 11 = normal; 10 = weak
Bit 1	24_48MHz Slew 1	1	24_48MHz clock slew rate control bits.
Bit 0	24_48MHz Slew 0	0	01 = strong: 11 = normal; 10 = weak

Absolute Maximum Ratings

Supply Voltage . . . . 5.5 V
Logic Inputs . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . 0°C to +70°C
Case Temperature . . . . 115°C
Storage Temperature . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V ±5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			mA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66M			100	mA
		C_L = Full load			360	mA
Power Down Supply Current	$I_{DD3.3PD}$	IREF=2.32			25	mA
		IREF= 5mA			45	mA
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{out}	Out put pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	mS
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.			3	mS
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	mS
Delay	t_{PZH},t_{PZH}	output enable delay (all outputs)	1		10	nS
	t_{PLZ},t_{PZH}	output disable delay (all outputs)	1		10	nS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Z_O	$V_O = V_X$	3000			Ω
Output High Voltage	V_{OH}	V_R = 475W ±1%; IREF = 2.32mA; I_{OH} = 6*IREF		0.71	1.2	V
Output High Current	I_{OH}			-13.92		mA
Rise Time[1]	t_r	V_{OL} = 20%, V_{OH} = 80%	175		700	ps
Differential Crossover Voltage[1]	V_X	Note 3	45	50	55	%
Duty Cycle[1]	d_t	V_T = 50%	45	51	55	%
Skew[1], CPU to CPU	t_{sk}	V_T = 50%			100	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc}$	$V_T = V_X$			150	ps

Notes:

1 - Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F0[1]			33.33		MHz
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}$*(0.5)	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			500	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L =10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			66.66		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}$*(0.5)	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			500	ps
Jitter	tjcyc-cyc[1]	V_T = 1.5 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 48MHz

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_O[1]	$V_O = V_{DD}$*(0.5)		48		MHz
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}$*(0.5)	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-29		-23	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	29		27	mA
48DOT Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		1	ns
48DOT Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		1	ns
VCH 48 USB Rise Time	t_r[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns
VCH 48 USB Fall Time	tf[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns
48 DOT to 48 USB Skew	tskew[1]	VT=1.5V			1	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			350	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L =10-20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}$*(0.5)	20		60	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-29		-23	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	29		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		4	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		4	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps

[1]Guarenteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period. Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

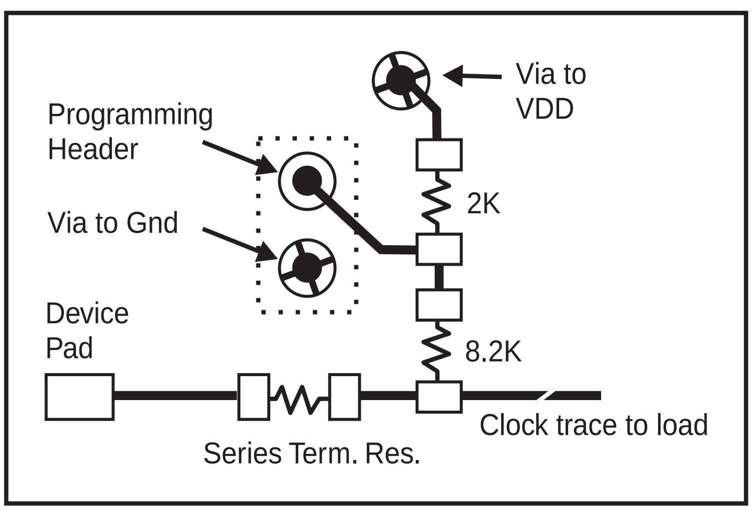
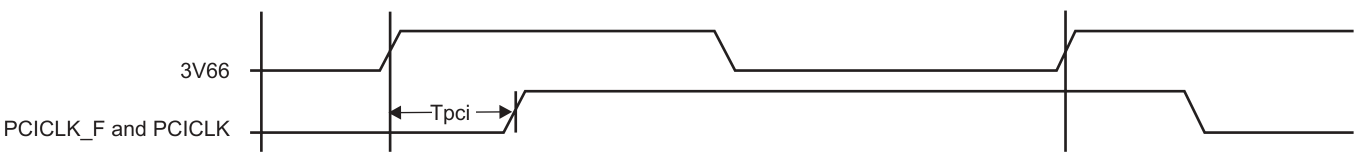


Fig. 1

Third party brands and names are the property of their respective owners.

Un-Buffered Mode 3V66 & PCI Phase Relationship

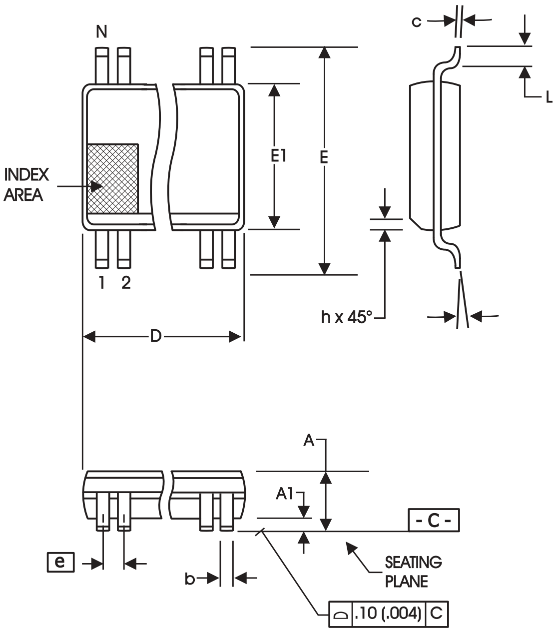
All 3V66 clocks are to be in pphase with each other. In the case where 3V66_1 is configured as 48MHz VCH clock, there is no defined phase relationship between 3V66_1/VCH and other 3V66 clocks. The PCI group should lag 3V66 by the standard skew described below as Tpci.



Group Skews at Common Transition Edges: (Un-Buffered Mode)

GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3V66	3V66	3V66 pin to pin skew	0		500	ps
PCI	PCI	PCI_F and PCI pin to pin skew	0		500	ps
3V66 to PCI	$S_{3V66\text{-}PCI}$	3V66 leads 33MHz PCI	1.5		3.5	ns

[1]Guarenteed by design, not 100% tested in production.



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS950219yFT

Example:

ICS XXXX y F - T

- **Designation for tape and reel packaging** (T)
- **Package Type** (F)
  F=SSOP
- **Revision Designator** (y) (will not correlate with datasheet revision)
- **Device Type** (XXXX)
- **Prefix** (ICS)
  ICS = Standard Device

Registered Company

ISO

9001

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