

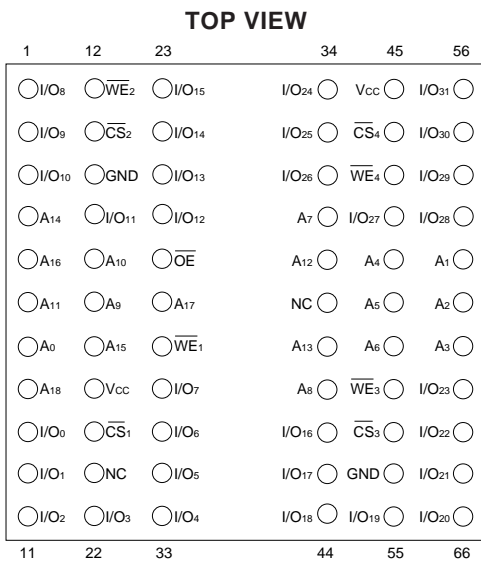
512Kx32 5V FLASH MODULE, SMD 5962-94612

FEATURES

- Access Times of 60, 70, 90, 120, 150ns
- Packaging
 - 66 pin, PGA Type, 1.075" square, Hermetic Ceramic HIP (Package 400⁽¹⁾)
 - 68 lead, 40mm, Low Capacitance Hermetic CQFP (Package 501)
 - 68 lead, 40mm, Low Profile 3.5mm (0.140"), CQFP (Package 502)
 - 68 lead, 22.4mm (0.880") Low Profile CQFP (G2U), 3.5mm (0.140") high, (Package 510)
 - 68 lead, 23.9mm (0.940") Low Profile CQFP (G1U), 3.5mm (0.140") high, (Package 519)
- 100,000 Erase/Program Cycles Minimum
- Sector Architecture
 - 8 equal size sectors of 64KBytes each
 - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 512Kx32
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming. 5V ±10% Supply.
- Low Power CMOS, 6.5mA Standby
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Built-in Decoupling Caps for Low Noise Operation
- Page Program Operation and Internal Program Control Time
- Weight
 - WF512K32-XG2UX5 - 8 grams typical
 - WF512K32-XH1X5 - 13 grams typical
 - WF512K32-XG4X5 - 20 grams typical
 - WF512K32-XG4TX5 - 20 grams typical
 - WF512K32-XG1UX5 - 5 grams typical

1. Call factory for PGA type (HIP) package options.
Note: See Flash Programming Application Note 4M5 for algorithms.

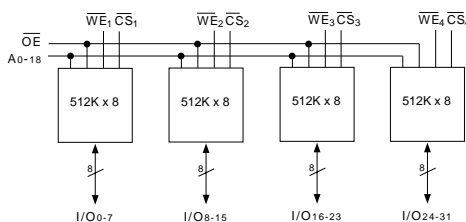
FIG. 1 PIN CONFIGURATION FOR WF512K32N-XH1X5



PIN DESCRIPTION

I/O ₀₋₃₁	Data Inputs/Outputs
A ₀₋₁₈	Address Inputs
$\overline{\text{WE}}_{1-4}$	Write Enables
$\overline{\text{CS}}_{1-4}$	Chip Selects
$\overline{\text{OE}}$	Output Enable
V _{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



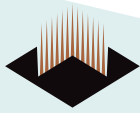


FIG. 2 PIN CONFIGURATION FOR WF512K32F-XG4X5 (Low Capacitance) AND WF512K32-XG4TX5

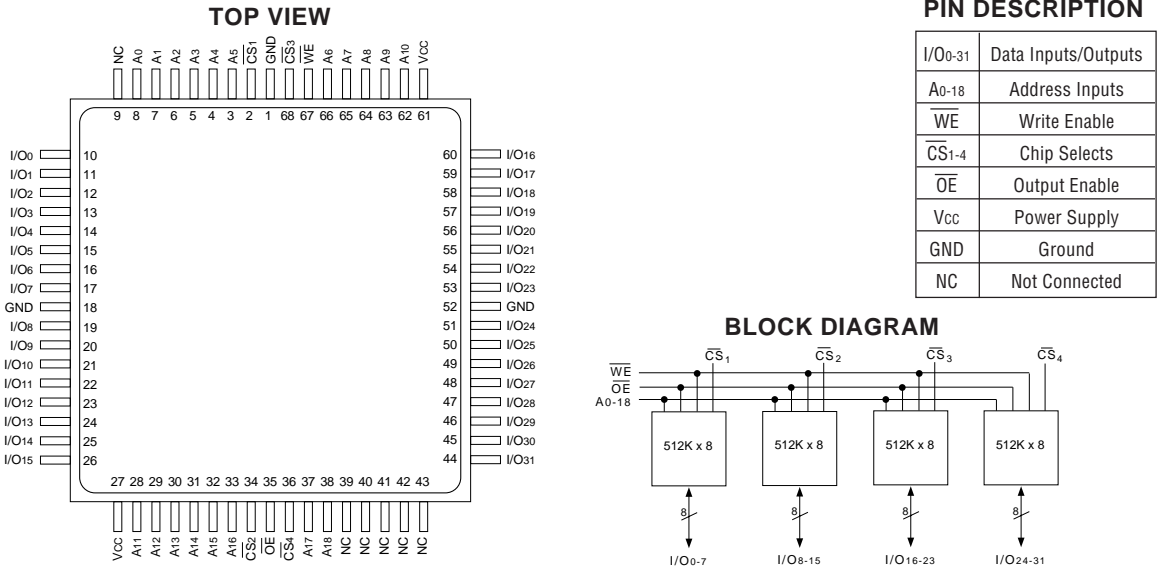
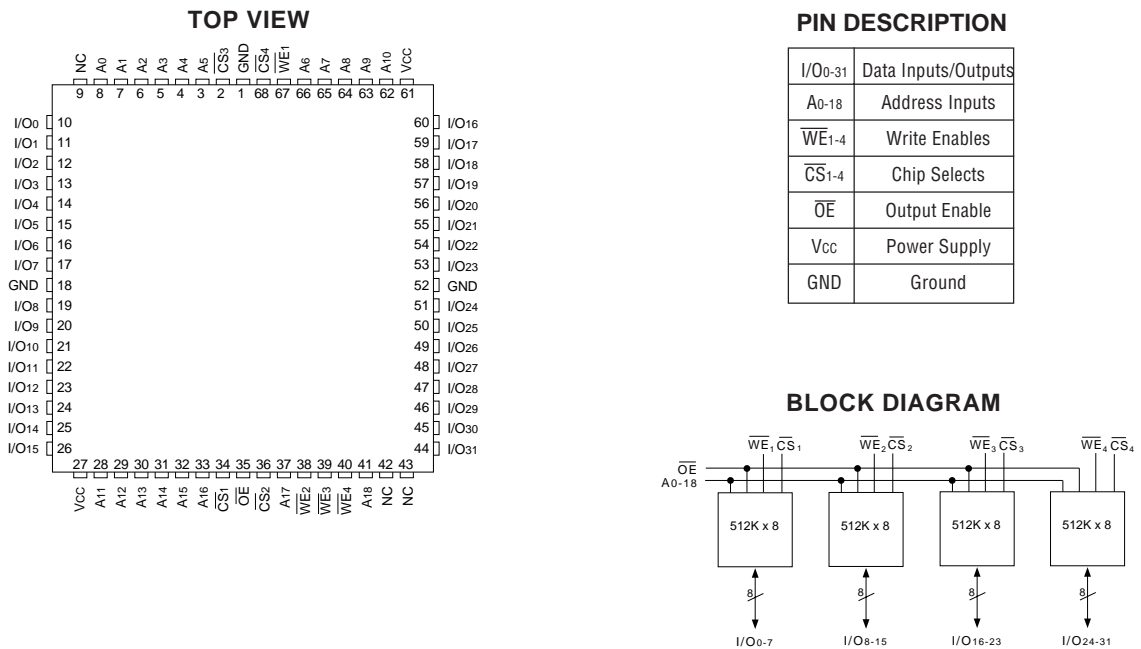
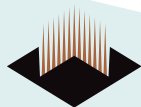


FIG. 3 PIN CONFIGURATION FOR WF512K32-XG2UX5 AND WF512K32-XG1UX5





ABSOLUTE MAXIMUM RATINGS (1)

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (V _{CC})	-2.0 to +7.0	V
Signal voltage range (any pin except A ₉) (2)	-2.0 to +7.0	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Data Retention (Mil Temp)	20 years	
Endurance - write/erase cycles (Mil Temp)	100,000 cycles min.	
A ₉ Voltage for sector protect (V _{ID}) (3)	-2.0 to +14.0	V

NOTES:

- Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods of up to 20ns.
- Minimum DC input voltage on A₉ pin is -0.5V. During voltage transitions, A₉ may overshoot V_{SS} to -2V for periods of up to 20ns. Maximum DC input voltage on A₉ is +13.5V which may overshoot to 14.0 V for periods up to 20ns.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.0	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C
Operating Temp. (Ind.)	T _A	-40	+85	°C
A ₉ Voltage for Sector Protect	V _{ID}	11.5	12.5	V

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND or V _{CC}		10	μA
Output Leakage Current	I _{LOx32}	V _{CC} = 5.5, V _{IN} = GND or V _{CC}		10	μA
V _{CC} Active Current for Read (1)	I _{CC1}	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5\text{MHz}$		190	mA
V _{CC} Active Current for Program or Erase (2)	I _{CC2}	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}$		240	mA
V _{CC} Standby Current	I _{CC4}	V _{CC} = 5.5, CS = V _{IH} , f = 5MHz		6.5	mA
V _{CC} Static Current	I _{CC3}	V _{CC} = 5.5, CS = V _{IH}		0.6	mA
Output Low Voltage	V _{OL}	I _{OL} = 8.0 mA, V _{CC} = 4.5		0.45	V
Output High Voltage	V _{OH1}	I _{OH} = 2.5 mA, V _{CC} = 4.5	0.85 x V _{CC}		V
Low V _{CC} Lock-Out Voltage	V _{LKO}		3.2	4.2	V

DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

NOTES:

- The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with \overline{OE} at V_{IH}.
- I_{CC} active while Embedded Algorithm (program or erase) is in progress.

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
\overline{OE} capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	50	pF
\overline{WE} 1-4 capacitance HIP (PGA)	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
CQFP G4T			50	
CQFP G2U/G1U			15	
\overline{CS} 1-4 capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	50	pF

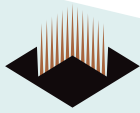
This parameter is guaranteed by design but not tested.

LOW CAPACITANCE CQFP

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
\overline{OE} capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	32	pF
CQFP G4 capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	32	pF
\overline{CS} 1-4 capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	15	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	15	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	32	pF

This parameter is guaranteed by design but not tested.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, \overline{CS} CONTROLLED

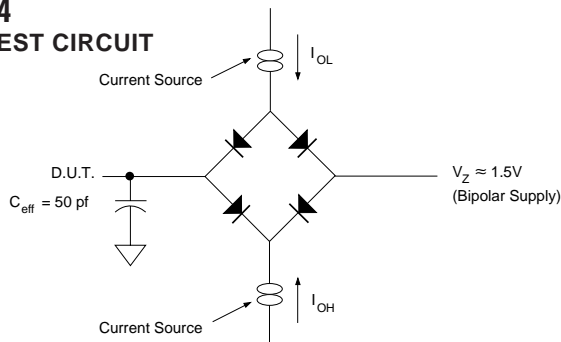
($V_{CC} = 5.0V$, $V_{SS} = 0V$, $T_A = -55^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	60		70		90		120		150		ns
Write Enable Setup Time	twLEL	tws	0		0		0		0		0		ns
Chip Select Pulse Width	teLEH	tCP	40		45		45		50		50		ns
Address Setup Time	tAVEL	tAS	0		0		0		0		0		ns
Data Setup Time	tdVEH	tDS	40		45		45		50		50		ns
Data Hold Time	teHDX	tDH	0		0		0		0		0		ns
Address Hold Time	teLAX	tAH	40		45		45		50		50		ns
Chip Select Pulse Width High	teHEL	tCPH	20		20		20		20		20		ns
Duration of Byte Programming Operation (1)	twHHH1			300		300		300		300		300	μ s
Sector Erase Time (2)	twHHH2			15		15		15		15		15	sec
Read Recovery Time	tgHEL		0		0		0		0		0		ns
Chip Programming Time				11		11		11		11		11	sec
Chip Erase Time (3)				64		64		64		64		64	sec

NOTES:

1. Typical value for t_{WHH1} is 7 μ s.
2. Typical value for t_{WHH2} is 1sec.
3. Typical value for Chip Erase Time is 8sec.

FIG. 4
AC TEST CIRCUIT

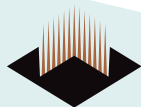


AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0$, $V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance $Z_0 = 75 \Omega$.
 V_Z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, \overline{WE} CONTROLLED

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	60		70		90		120		150		ns
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		0		0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{WP}	40		45		45		50		50		ns
Address Setup Time	t _{AVWH}	t _{AS}	0		0		0		0		0		ns
Data Setup Time	t _{DVWH}	t _{DS}	40		45		45		50		50		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		0		0		ns
Address Hold Time	t _{WHAX}	t _{AH}	40		45		45		50		50		ns
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	20		20		20		20		20		ns
Duration of Byte Programming Operation (1)	t _{WHWH1}			300		300		300		300		300	μs
Sector Erase Time (2)	t _{WHWH2}			15		15		15		15		15	sec
Read Recovery Time before Write	t _{GHWL}		0		0		0		0		0		ns
V _{CC} Set-up Time		t _{VCS}	50		50		50		50		50		μs
Chip Programming Time				11		11		11		11		11	sec
Output Enable Setup Time		t _{OES}	0		0		0		0		0		ns
Output Enable Hold Time (4)		t _{OEH}	10		10		10		10		10		ns
Chip Erase Time (3)				64		64		64		64		64	sec

NOTES:

1. Typical value for t_{WHWH1} is 7μs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 8sec.
4. For Toggle and Data Polling.

AC CHARACTERISTICS – READ ONLY OPERATIONS

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{TRC}	60		70		90		120		150		ns
Address Access Time	t _{AVQV}	t _{ACC}		60		70		90		120		150	ns
Chip Select Access Time	t _{ELQV}	t _{CCE}		60		70		90		120		150	ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		30		35		35		50		55	ns
Chip Select to Output High Z (1)	t _{EHQZ}	t _{DF}		20		20		20		30		35	ns
Output Enable High to Output High Z (1)	t _{GHQZ}	t _{DF}		20		20		20		30		35	ns
Output Hold from Address, CS or OE Change, whichever is First	t _{AXQX}	t _{OH}	0		0		0		0		0		ns

1. Guaranteed by design, but not tested



FIG. 5
AC WAVEFORMS FOR READ OPERATIONS

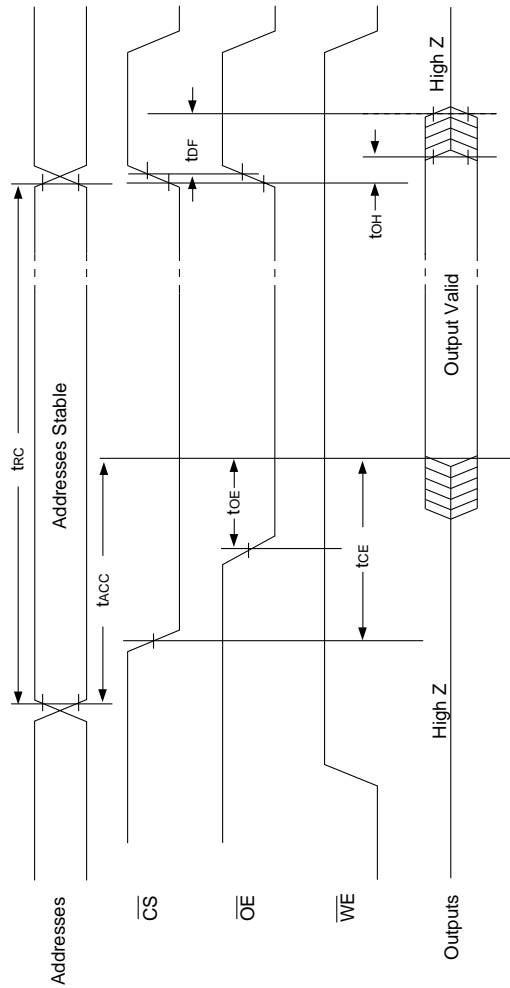
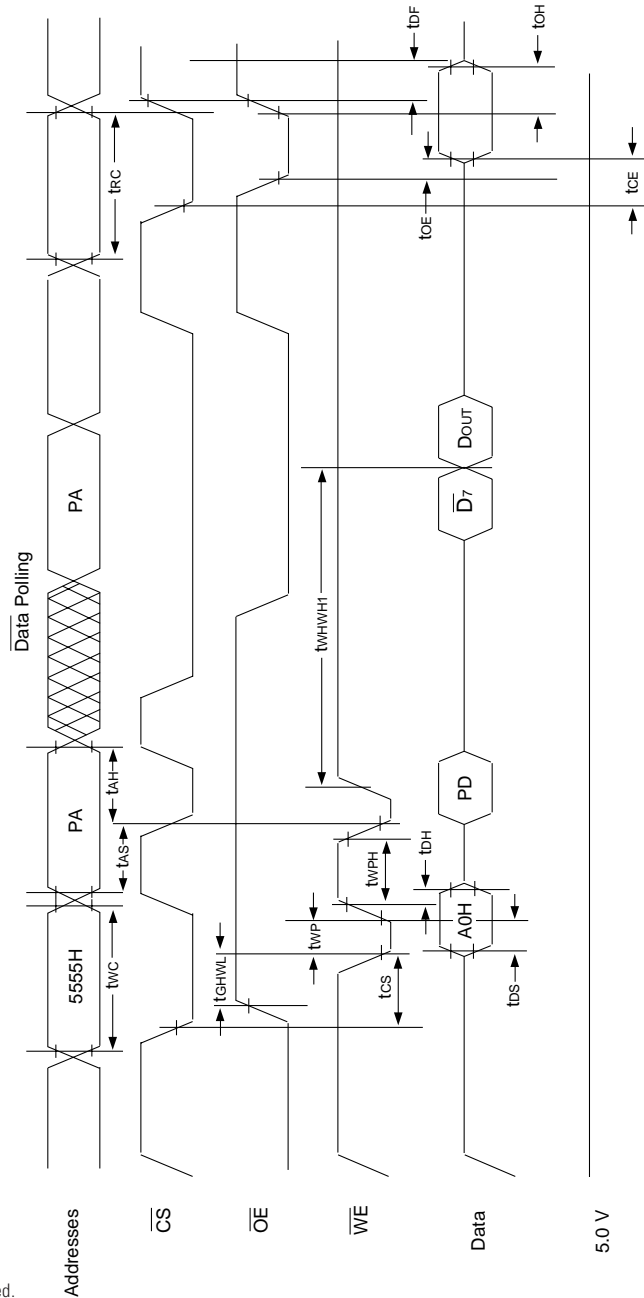




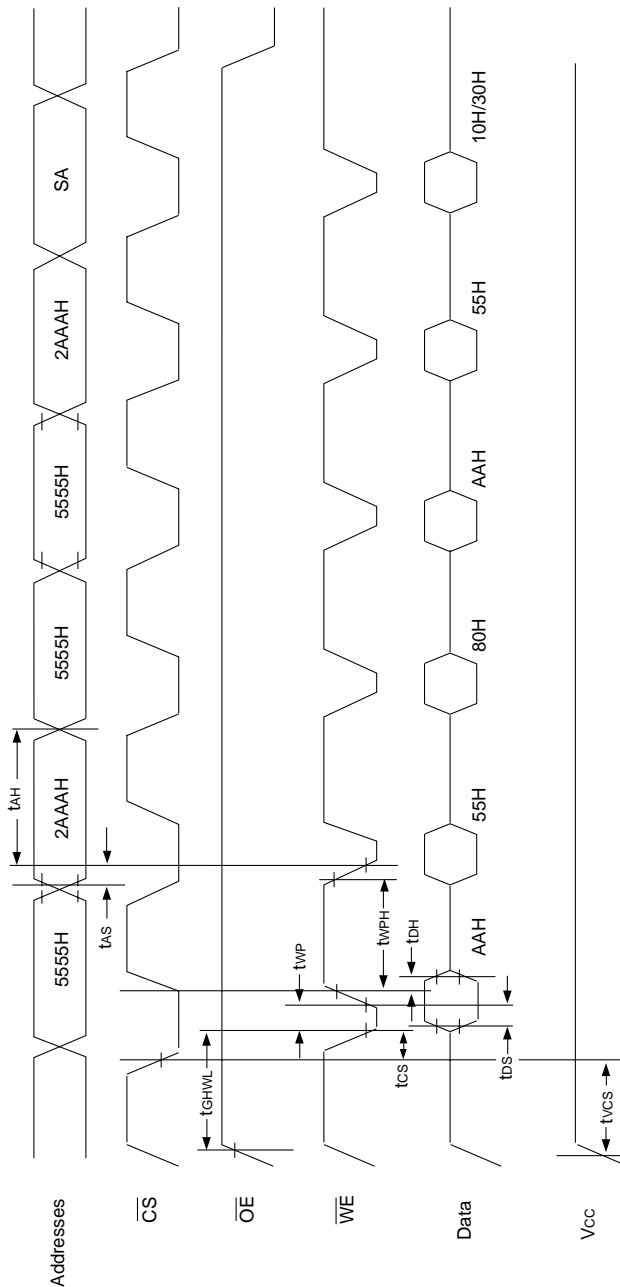
FIG. 6
WRITE/ERASE/PROGRAM
OPERATION, WE CONTROLLED



- NOTES:**
1. PA is the address of the memory location to be programmed.
 2. PD is the data to be programmed at byte address.
 3. $\overline{D7}$ is the output of the complement of the data written to the device (for each chip).
 4. DOUT is the output of the data written to the device.
 5. Figure indicates last two bus cycles of four bus cycle sequence.



FIG. 7
AC WAVEFORMS CHIP/SECTOR
ERASE OPERATIONS



NOTE:

1. SA is the sector address for Sector Erase.



FIG. 8
AC WAVEFORMS FOR DATA POLLING
DURING EMBEDDED ALGORITHM OPERATIONS

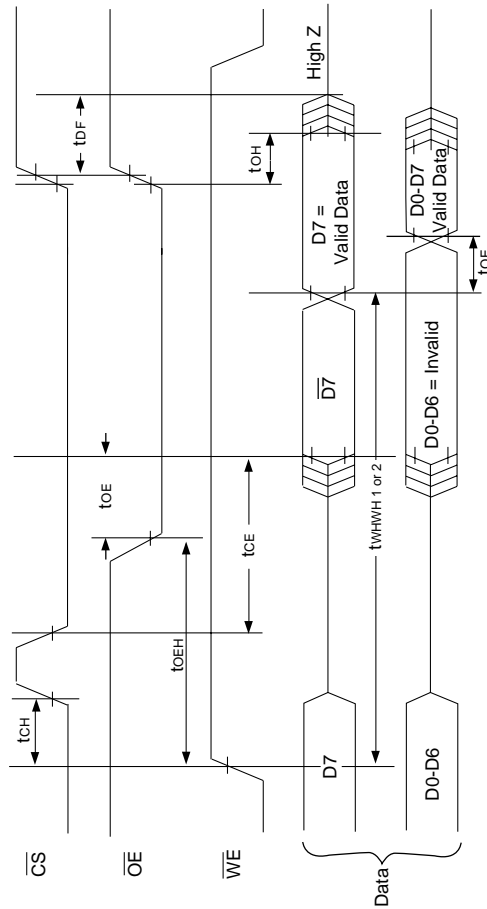
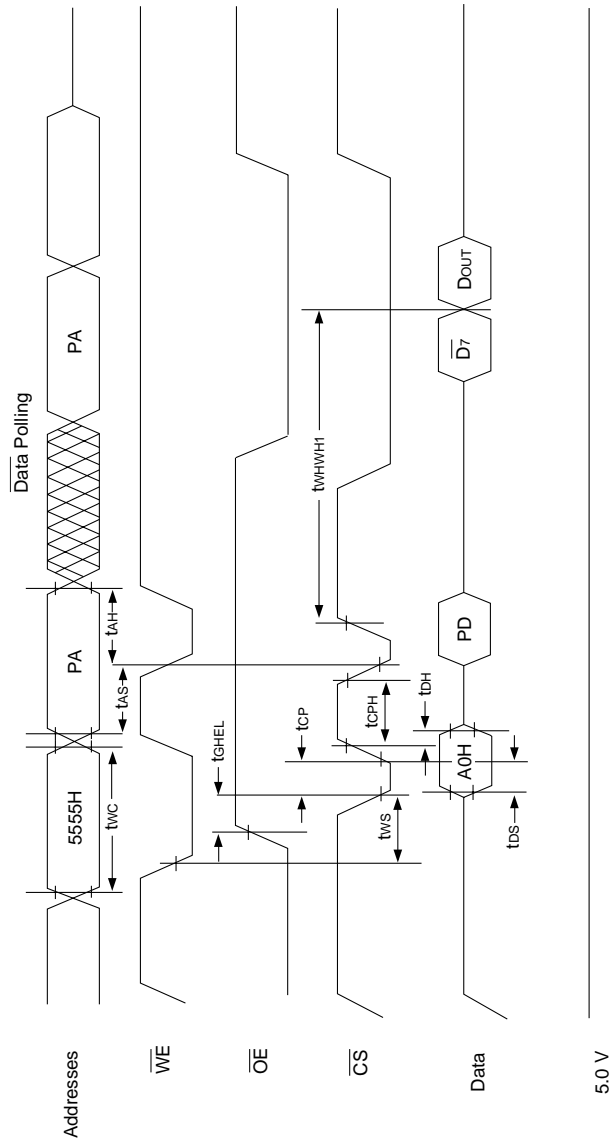




FIG. 9
ALTERNATE \overline{CS} CONTROLLED
PROGRAMMING OPERATION TIMINGS

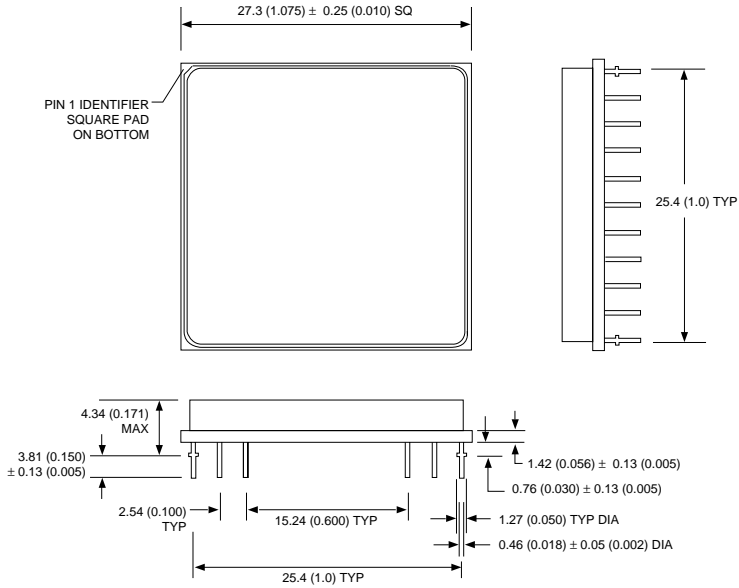


NOTES:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7 is the output of the complement of the data written to the device (for each chip).
4. Dout is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.



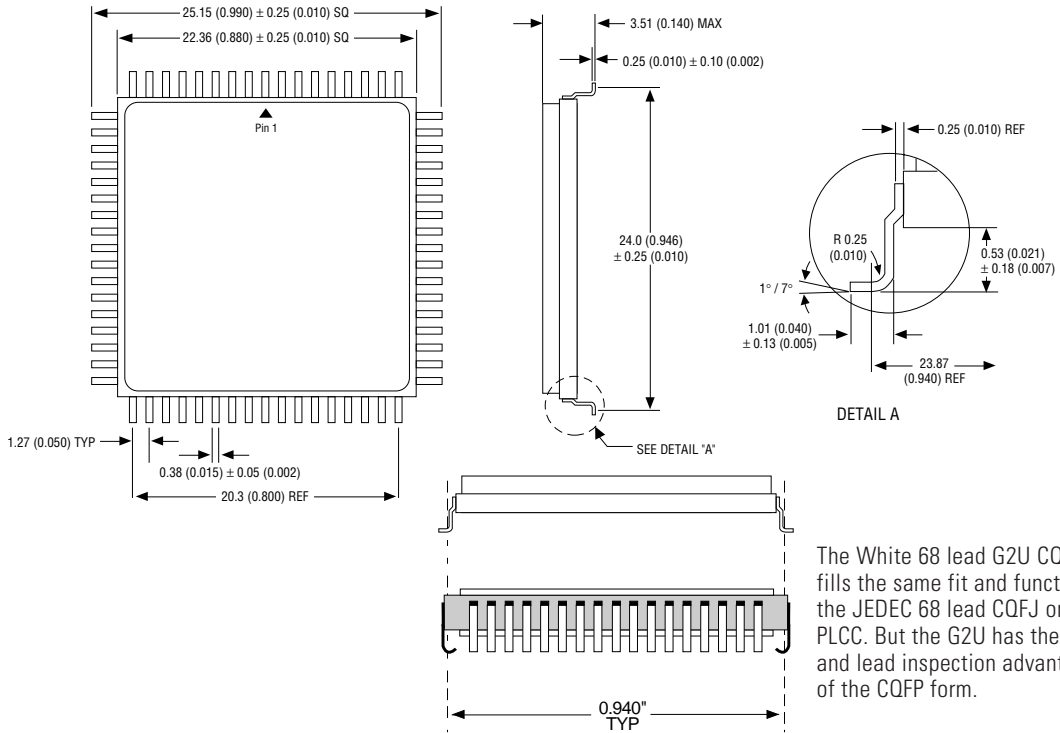
PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



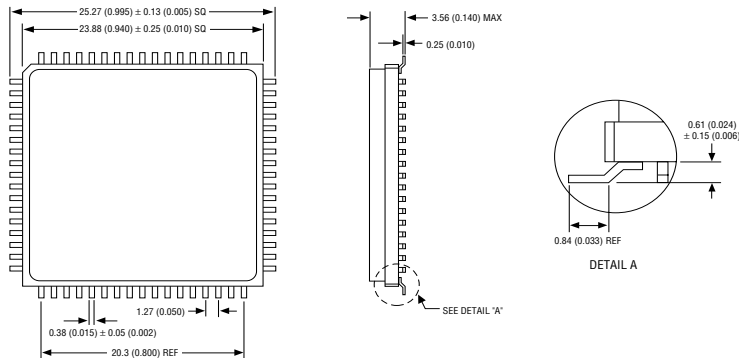
PACKAGE 510: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)



The White 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

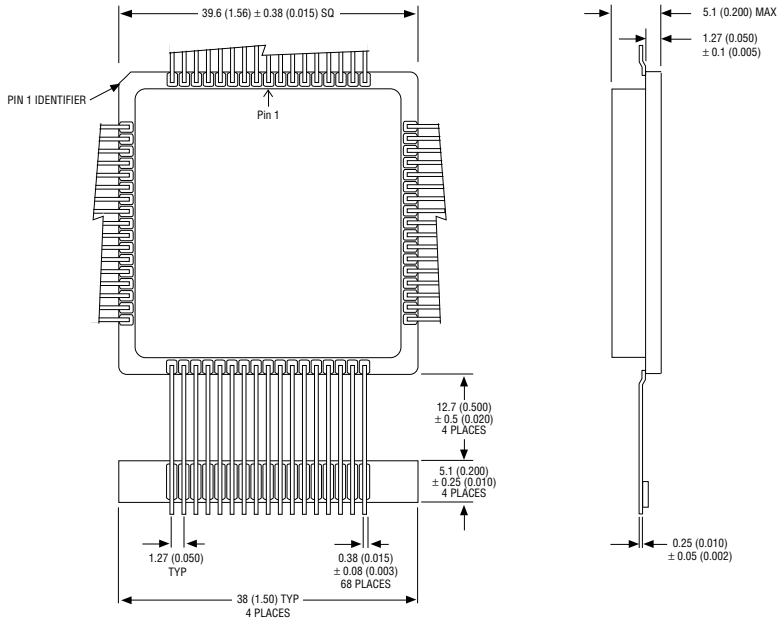
PACKAGE 519: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1U)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

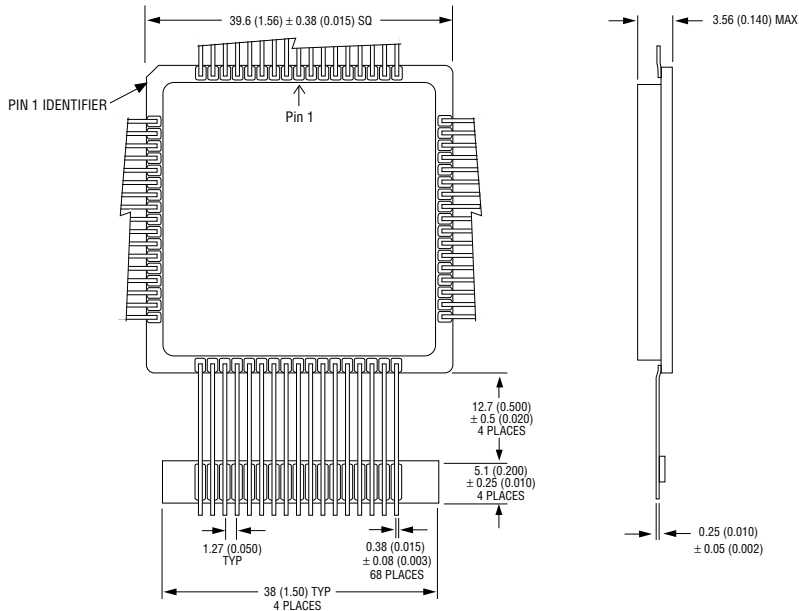


PACKAGE 501: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W F 512K32 X - XXX X X 5 X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

V_{PP} PROGRAMMING VOLTAGE

5 = 5 V

DEVICE GRADE:

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE TYPE:

- H1 = 1.075" sq. Ceramic Hex In Line Package, HIP (Package 400*)
- G2U = 22.4mm Low Profile CQFP (Package 510)
- G1U = 23.9mm Low Profile CQFP (Package 519)
- G4 = 40mm Low Capacitance, CQFP (Package 501)
- G4T = 40mm Low Profile CQFP (Package 502)

ACCESS TIME (ns)

IMPROVEMENT MARK

- N = No Connect at pins 21 and 39 in HIP for Upgrade (H1 only)*
- F = Low Capacitance Device (G4 only)

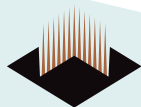
ORGANIZATION, 512K x 32

User configurable as 1M x 16 or 2M x 8

Flash

WHITE ELECTRONIC DESIGNS CORP.

* Call factory for PGA type (HIP) package options.



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
512K x 32 Flash Module	150ns	66 pin HIP (H1) 1.075" sq.	5962-94612 01HUX
512K x 32 Flash Module	120ns	66 pin HIP (H1) 1.075" sq.	5962-94612 02HUX
512K x 32 Flash Module	90ns	66 pin HIP (H1) 1.075" sq.	5962-94612 03HUX
512K x 32 Flash Module	70ns	66 pin HIP (H1) 1.075" sq.	5962-94612 04HUX
512K x 32 Flash Module	150ns	68 lead CQFP Low Profile (G4T)	5962-94612 01HTX
512K x 32 Flash Module	120ns	68 lead CQFP Low Profile (G4T)	5962-94612 02HTX
512K x 32 Flash Module	90ns	68 lead CQFP Low Profile (G4T)	5962-94612 03HTX
512K x 32 Flash Module	70ns	68 lead CQFP Low Profile (G4T)	5962-94612 04HTX
512K x 32 Flash Module	150ns	68 lead Low Capacitance CQFP (G4)	5962-94612 01HNX
512K x 32 Flash Module	120ns	68 lead Low Capacitance CQFP (G4)	5962-94612 02HNX
512K x 32 Flash Module	90ns	68 lead Low Capacitance CQFP (G4)	5962-94612 03HNX
512K x 32 Flash Module	70ns	68 lead Low Capacitance CQFP (G4)	5962-94612 04HNX
512K x 32 Flash Module	150ns	68 lead CQFP/J (G2U)	5962-94612 01HZX
512K x 32 Flash Module	120ns	68 lead CQFP/J (G2U)	5962-94612 02HZX
512K x 32 Flash Module	90ns	68 lead CQFP/J (G2U)	5962-94612 03HZX
512K x 32 Flash Module	70ns	68 lead CQFP/J (G2U)	5962-94612 04HZX
512K x 32 Flash Module	150ns	68 lead CQFP/J (G1U)	5962-94612 01H9X
512K x 32 Flash Module	120ns	68 lead CQFP/J (G2U)	5962-94612 02H9X
512K x 32 Flash Module	90ns	68 lead CQFP/J (G2U)	5962-94612 03H9X
512K x 32 Flash Module	70ns	68 lead CQFP/J (G2U)	5962-94612 04H9X