



# FAST CMOS BUS INTERFACE LATCH

IDT74FCT841AT/BT/CT/DT

## FEATURES:

- Low input and output leakage  $\leq 1\mu\text{A}$  (max.)
- CMOS power levels
- True TTL input and output compatibility
  - $V_{OH} = 3.3\text{V}$  (typ.)
  - $V_{OL} = 0.3\text{V}$  (typ.)
- Meets or exceeds JEDEC standard 18 specifications
- Available in SOIC, SSOP, and QSOP packages
- A, B, C and D speed grades
- High drive outputs (-15mA  $I_{OH}$ , 48mA  $I_{OL}$ )
- Power off disable outputs permit "live insertion"

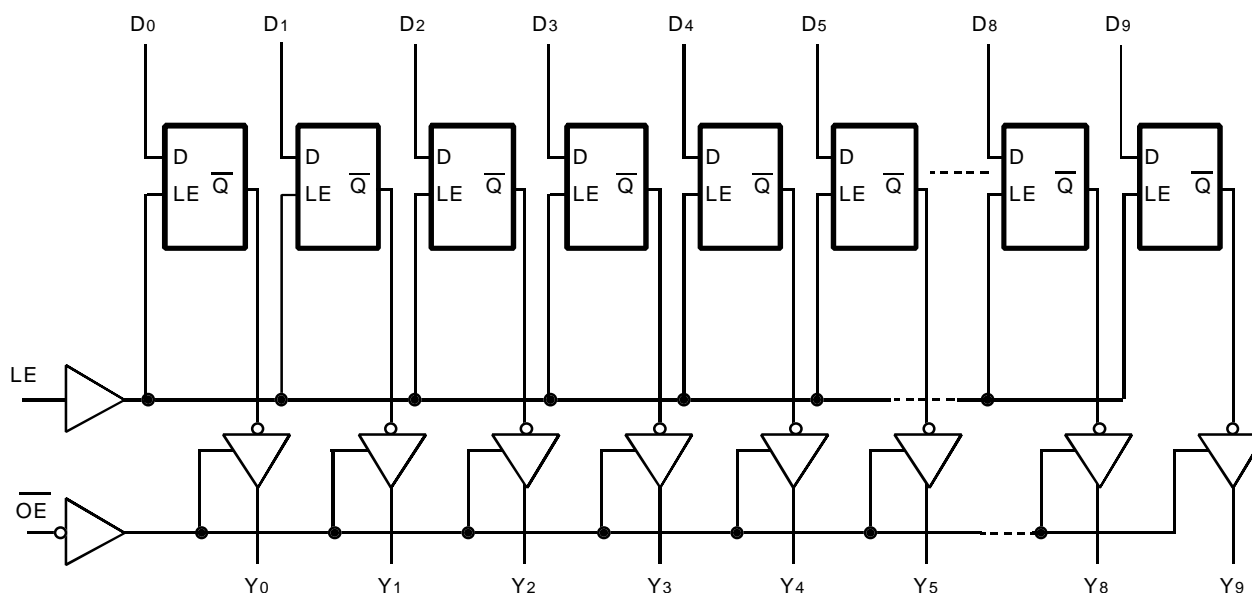
## DESCRIPTION:

The FCT841T series is built using an advanced dual metal CMOS technology.

The FCT841T bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The FCT841T are buffered, 10-bit wide versions of the popular FCT373T function. They are ideal for use as an output port requiring high  $I_{OL}/I_{OH}$ .

All of the FCT841T high-performance interface family can drive large capacitive loads, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes to ground and all outputs are designed for low-capacitance bus loading in high-impedance state.

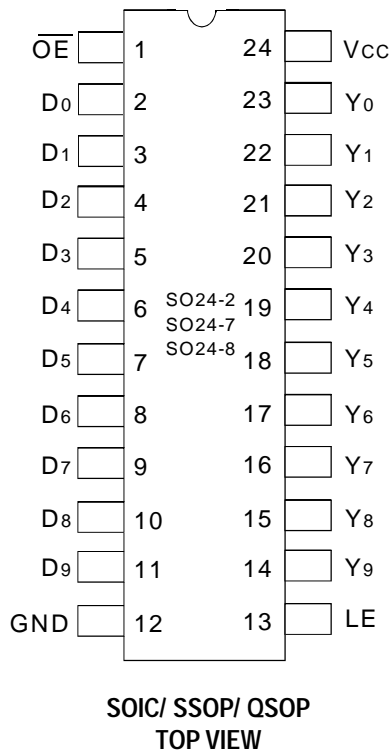
## FUNCTIONAL BLOCK DIAGRAM



INDUSTRIAL TEMPERATURE RANGE

AUGUST 2000

## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-60 to +120	mA

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### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.
- Inputs and V<sub>CC</sub> terminals only.
- Outputs and I/O terminals only.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

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### NOTE:

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Name	I/O	Description
D <sub>i</sub>	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y <sub>i</sub>	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs V <sub>i</sub> are in high-impedance (off) state.

## FUNCTION TABLE (1)

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D <sub>i</sub>	Q <sub>i</sub>	Y <sub>i</sub>	
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched (High Z)
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

### NOTE:

- H = HIGH  
L = LOW  
X = Don't Care  
NC = No Change  
Z = High-Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{IL}$	Input LOW Current <sup>(4)</sup>		$V_I = 0.5\text{V}$	—	—	$\pm 1$	
$I_{OZH}$	High Impedance Output Current (3-State Output Pins) <sup>(4)</sup>	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_O = 0.5\text{V}$	—	—	$\pm 1$	
$I_I$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	$\pm 1$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$V_H$	Input Hysteresis	—		—	200	—	mV
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$		—	0.01	1	mA

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -8\text{mA}$	2.4	3.3	—	V
			$I_{OH} = -15\text{mA}$	2	3	—	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 48\text{mA}$	—	0.3	0.5	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-120	-225	mA
$I_{OFF}$	Input/Output Power Off Leakage <sup>(5)</sup>	$V_{CC} = 0\text{V}, V_{IN} \text{ or } V_O \leq 4.5\text{V}$		—	—	$\pm 1$	$\mu\text{A}$

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .
- This parameter is guaranteed but not tested.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V <sup>(3)</sup>		—	0.5	2	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open $\overline{OE}$ = GND LE = V <sub>CC</sub> One Input Toggling 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	0.15	0.25	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V <sub>CC</sub> One Bit Toggling	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	1.5	3.5	mA
		V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V <sub>CC</sub> One Bit Toggling	V <sub>IN</sub> = 3.4 V <sub>IN</sub> = GND	—	1.8	4.5	
		V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V <sub>CC</sub> Eight Bits Toggling	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	3	6 <sup>(5)</sup>	
		V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V <sub>CC</sub> Eight Bits Toggling	V <sub>IN</sub> = 3.4 V <sub>IN</sub> = GND	—	5	14 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V). All other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 I<sub>CC</sub> = Quiescent Current  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 f<sub>i</sub> = Input Frequency  
 N<sub>i</sub> = Number of Inputs at f<sub>i</sub>  
 All currents are in milliamps and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

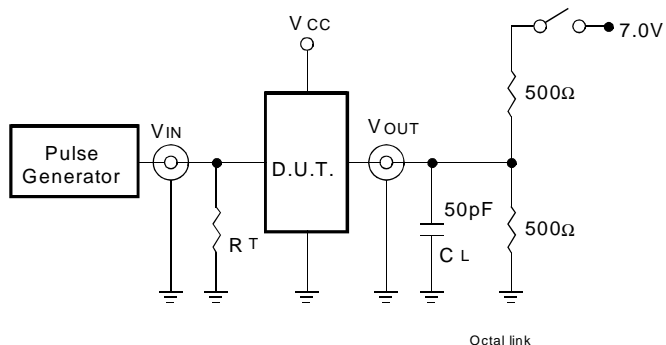
Symbol	Parameter	Conditions <sup>(1)</sup>	FCT841AT		FCT841BT		FCT841CT		FCT841DT		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D <sub>i</sub> to Y <sub>1</sub> (LE = HIGH)	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	9	1.5	6.5	1.5	5.5	1.5	4.2	ns
		C <sub>L</sub> = 300pF <sup>(4)</sup> R <sub>L</sub> = 500Ω	1.5	13	1.5	13	1.5	13	1.5	8	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LE to Y <sub>1</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	12	1.5	8	1.5	6.4	1.5	4	ns
		C <sub>L</sub> = 300pF <sup>(4)</sup> R <sub>L</sub> = 500Ω	1.5	16	1.5	15.5	1.5	15	1.5	8	
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\overline{OE}$ to Y <sub>1</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	11.5	1.5	8	1.5	6.5	1.5	4.8	ns
		C <sub>L</sub> = 300pF <sup>(4)</sup> R <sub>L</sub> = 500Ω	1.5	23	1.5	14	1.5	12	1.5	9	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{OE}$ to Y <sub>1</sub>	C <sub>L</sub> = 5pF <sup>(4)</sup> R <sub>L</sub> = 500Ω	1.5	7	1.5	6	1.5	5.7	1.5	4	ns
		C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	8	1.5	7	1.5	6	1.5	4	
t <sub>SU</sub>	Data to LE Set-up Time	C <sub>L</sub> = 50pF	2.5	—	2.5	—	2.5	—	1.5	—	ns
t <sub>H</sub>	Data to LE Hold Time	R <sub>L</sub> = 500Ω	2.5	—	2.5	—	2.5	—	1	—	ns
t <sub>w</sub>	LE Pulse Width HIGH <sup>(3)</sup>		4	—	4	—	4	—	3	—	ns

### NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.
4. These conditions are guaranteed but not tested.

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

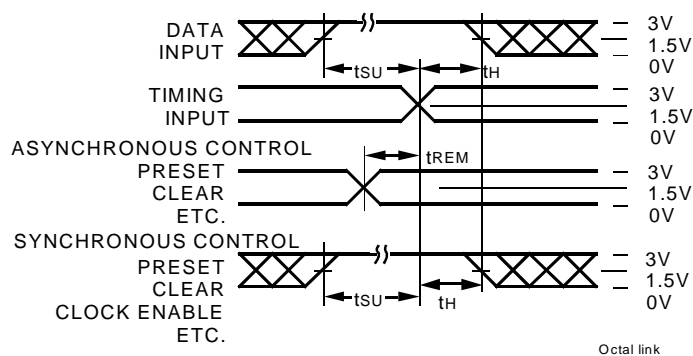
Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

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#### DEFINITIONS:

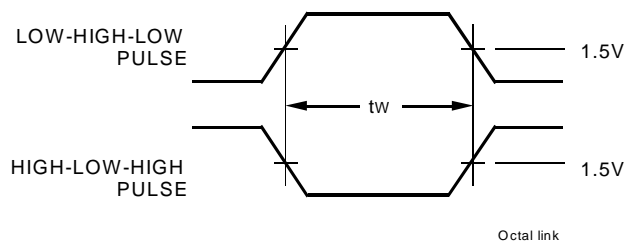
CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

### SET-UP, HOLD, AND RELEASE TIMES



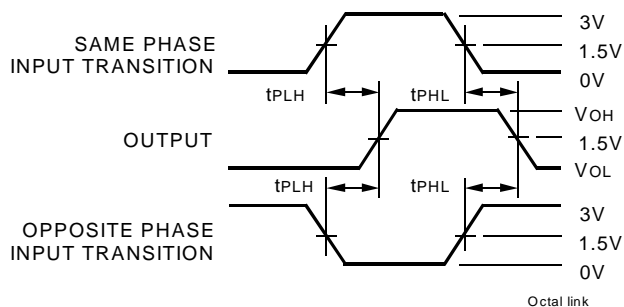
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### PULSE WIDTH



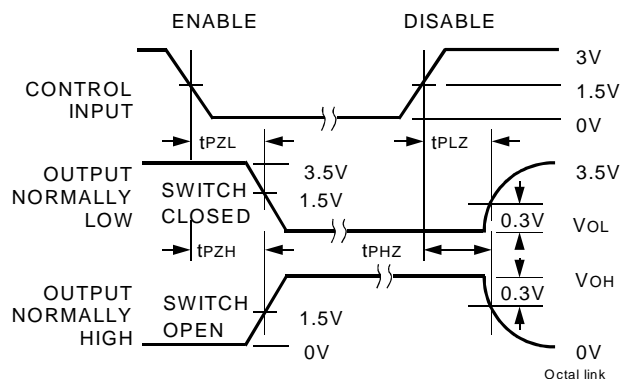
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### PROPAGATION DELAY



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### ENABLE AND DISABLE TIMES

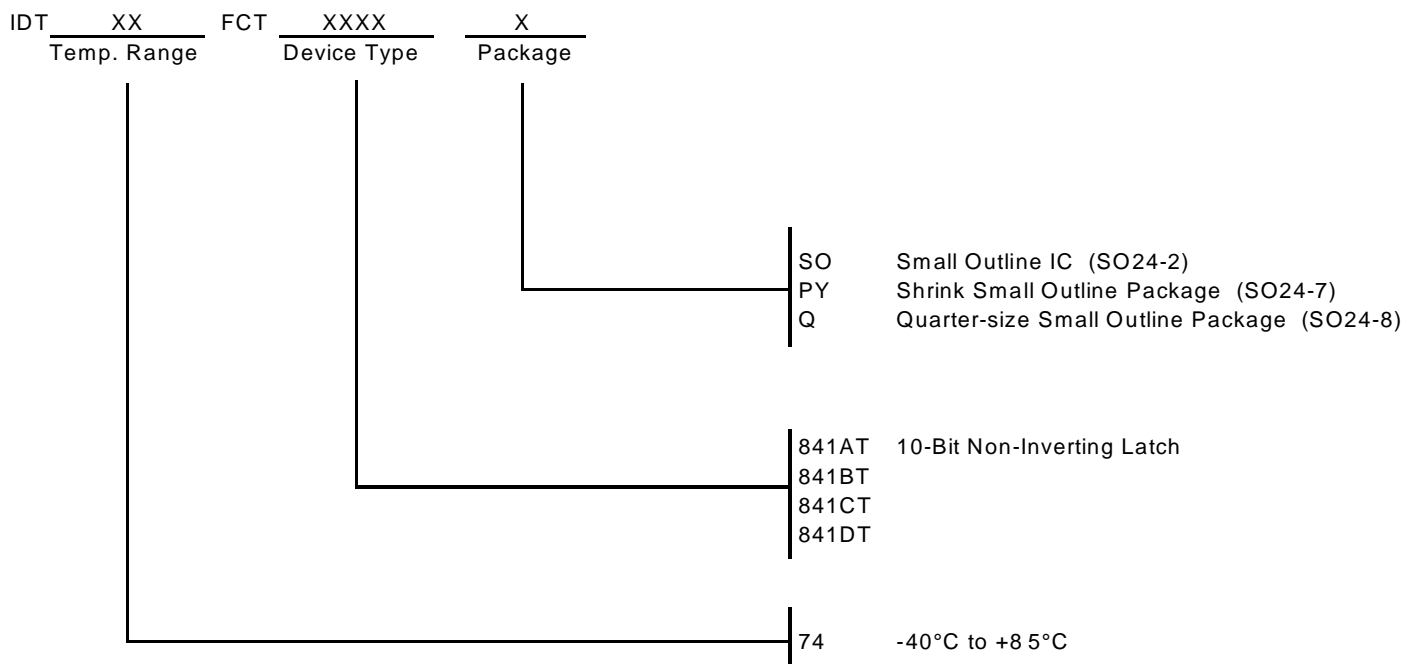


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#### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_f \leq 2.5\text{ns}$ ;  $t_r \leq 2.5\text{ns}$

## ORDERING INFORMATION



**CORPORATE HEADQUARTERS**  
2975 Stender Way  
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800-345-7015 or 408-727-6116  
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