Gate Counting Methodology for APEX 20K Devices

September 1999, ver. 1.01 Application Note 110

Introduction

Altera's APEX™ 20K device family offers an innovative combination of look-up table (LUT) logic, product-term logic, and embedded memory. Ranging from 162,000 to 2,500,000 maximum system gates, the revolutionary APEX 20K architecture offers System-on-a-Programmable-Chip™ integration, allowing designers to combine functions best suited for LUT, product-term logic, and memory into one device. The LUT architecture can be used to implement register-intensive data path and arithmetic functions. Product-term logic can be used for high fan-in combinatorial functions at high speeds. APEX 20K programmable logic devices (PLDs) are the first devices to combine these architectures to provide the performance, flexibility, and efficiency that designers require.

This application note describes the gate counting method used for the APEX 20K device family and defines gate counting terminology. It shows how logic array and embedded array gates are calculated. APEX 20K gates are compared to gate array gates, using LSI Logic's LCA300K family of standard "sea-of-gates" gate arrays as a reference.

Gate Count Specifications

Tables 1 and 2 show the features, including gate count specifications, for APEX 20K devices.

Table 1. APEX 20K Device Features *Note (1)*

Feature	EP20K60E	EP20K100E EP20K100	EP20K160E	EP20K200E EP20K200	EP20K300E
Typical Gates	60,000	100,000	160,000	200,000	300,000
Maximum System Gates	162,000	263,000	404,000	526,000	728,000
Logic Elements (LEs)	2,560	4,160	6,400	8,320	11,520
Embedded System Blocks	16	26	40	52	72
Maximum RAM Bits	32,768	53,248	81,920	106,496	147,456
Maximum Macrocells	256	416	640	832	1,152
Maximum I/O Pins	204	252	316	382	408

Table 2. APEX 20K Device Features *Note (1)*

Feature	EP20K400E EP20K400	EP20K600E	EP20K1000E	EP20K1500E
Typical Gates	400,000	600,000	1,000,000	1,500,000
Maximum System Gates	1,052,000	1,537,000	1,770,000	2,500,000
Logic Elements	16,640	24,320	38,400	54,720
Embedded System Blocks	104	152	160	228
Maximum RAM Bits	212,992	311,296	327,680	466,944
Maximum Macrocells	1,664	2,432	2,560	3,648
Maximum I/O Pins	502	624	716	858

Note to tables:

(1) For designs that require IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan testing, the built-in JTAG circuitry contributes up to 52,130 additional gates.

Table 3 explains the terminology used to describe the APEX 20K device features.

Table 3. APEX 20K Device Terminology (Part 1 of 2)

Designation	Description
Logic Elements	Logic elements are the basic logic building blocks that make up the logic array in the APEX 20K architecture. Each LE consists of a four-input LUT, a programmable flipflop, and dedicated signal paths for carry and cascade functions.
Logic Array	The logic array performs the same function as the sea-of-gates in a gate array; it is used to implement general logic such as counters, adders, state machines, and multiplexers.
Logic Array Gates	Logic array gates are the total number of usable gates available in the logic array of a device.
Logic Array Blocks (LABs)	The logic array consists of LABs. Each LAB contains 10 LEs and a local interconnect. The 10 LEs can be used to create medium-sized blocks of logic—such as 10-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks.
Embedded System Blocks (ESBs)	Embedded system blocks are used to create RAM, ROM, first-in first-out (FIFO), dual-port RAM, and content-addressable memory (CAM) functions. ESBs can also implement complex logic functions such as digital signal processing (DSP), microcontroller, wide data-path manipulation, and data transformation functions. ESBs can implement logic as either LUTs or product terms.
ESB Array Gates	ESB array gates are the total number of gates available in the embedded array.
Product Term	A product term is a wide AND gate. These AND gates are combined into macrocells when the ESB implements product-term logic.

Table 3. APEX 20K Device Terminology (Part 2 of 2)

Designation	Description
Maximum Macrocells	Maximum macrocells is the number of available macrocells when all ESBs are used entirely for product-term logic.
Maximum RAM Bits	Maximum RAM bits is the number of bits available when all ESBs are used entirely for memory functions.
Typical Gate Count	Typical gate count is the capacity metric indicating the gate array size that can be implemented in an APEX 20K device. Typical gate count assumes that a design uses the logic array and the embedded array. It also assumes that portions of the embedded array are used for both memory and logic functions.
Maximum System Gate Count	Maximum system gate count is the number of gates when 100% of the ESBs are used as memory. This measurement approximates the gate counting method used by field-programmable gate array (FPGA) vendors when determining “system gates”.

Calculating Logic Array Gates

Before calculating the total number of logic array gates, you must first determine the LE gate count. Two ways to calculate logic array gates are to compare LEs with standard gate arrays and to use empirical data for calculating the logic array gates.

For example, the APEX 20K LE gate range can be determined by using the LSI ***LCA300K Data Book*** and comparing the implementation of various functions in LEs versus the LCA300K family of standard gate arrays. To find the gate range, calculate the number of gates for a simple and a complex function. A simple function determines the lower bound, and a complex function determines the higher bound of the range. One LUT and one register are used to implement each function. See Table 4.

Table 4. Calculating LE Gates Using LCA300K Functions

Implementation	APEX 20K LUT	LSI Gates	APEX 20K Register	LSI Gates	Total
Simple LCA300K function	Two-input AND gate	1	D-type flipflop	7	8
Complex LCA300K function	Four-input XOR gate	13	D-type flipflop with clear, preset, and clock enable signals	8	21

The LE gate range is the total number of LSI gates used for simple functions and the total number of LSI gates used for complex functions. In this case, eight gates are used for simple functions and 21 gates are used for complex functions.

The APEX 20K LE gate equivalents are also calculated with empirical data. Altera compiled over 100 designs targeted towards four-input LUT technology, applying the same designs to LCA300K gate arrays using the Synopsys Design Compiler. The comparison between the LCA300K gate count usage and the LUT usage yields an average of 12 gates per LE. A device's logic array gate count can be determined by multiplying the number of gates per LE with its LE count. For example, an EP20K1000E device has 38,400 LEs; at 12 gates per LE, the EP20K1000E device has approximately 460,000 logic array gates.

Calculating Embedded Array Gates

The embedded array contains ESBs, which are extremely efficient for creating memory functions that can be configured on-the-fly. APEX 20K devices can implement up to 2 Kbits of memory in each ESB. In addition, designers can combine ESBs to achieve higher bit counts. APEX 20K ESBs have the capacity and speed to implement high-end memory blocks. Because ESBs are dedicated architectural elements, they do not require resource trade-offs. ESBs can also be used to implement logic functions as LUTs or with product-term logic.

ESB Memory Gate Count

Gate counting schemes for memory functions can vary depending on the type of RAM, vendor, and architecture. Because most memory functions use an average of four gates per memory bit, the APEX 20K family uses the same standard, allowing designers to easily compare different gate-counting schemes for different devices. The ESB array gate count can also be verified by using common LCA300K memory functions. Altera compiled various memory functions using the LSI memory compiler to determine gate counts and compare ESB implementations.

Table 5 shows the number of gates used by each memory function.

Table 5. Calculating ESB Array Gates Using LCA300K Memory Functions

Memory Function	Gates	Gates per Bit
128 × 8 single-port SRAM	4,620	4.5
128 × 16 single-port SRAM	7,980	3.9
128 × 32 single-port SRAM	14,700	3.6
128 × 16 dual-port SRAM	8,300	4.1
128 × 32 dual-port SRAM	14,910	3.6

The average number of gates per bit in Table 5 is 3.94, indicating that four gates per bit is a good metric for memory functions.

For an APEX 20K device, the maximum number of ESB array gates can be determined by multiplying the number of ESBs in the device with the number of bits per ESB and the number of gates per bit. For example, the following equation shows how to calculate the maximum embedded system gates used for memory implementations for an EP20K1000E device:

160 ESBs × 2,048 bits per ESB × 4 gates per bit = 1,310,720 gates

An EP20K1000E device has approximately 1,300,000 ESB array gates.

ESBs can implement logic as product terms or LUTs. When implementing product-term functions, the ESB becomes 16 macrocells, each of which contain two product terms and one register. The ESB can also implement LUT logic when it is preprogrammed with a bit pattern. For example, the ESB can implement a 128 × 16 ROM, which has seven address inputs and 16 data outputs. When programmed as 128 × 16 ROM, the ESB can implement logic with seven inputs and 16 outputs, effectively becoming 16 seven-input LUTs with registered inputs and outputs.

ESB Product-Term Logic Gate Count

The range of ESB gates implemented in product-term mode can be determined for simple and complex functions by adding the number of LCA300K gate equivalents for each ESB macrocell and ESB register. See Table 6.

Table 6. Calculating Embedded System Product-Term Gates Using LCA300K Functions

Implementation	16 ESB Macrocells	LSI Gates	16 ESB Registers	LSI Gates	Total
Simple LCA300K function	Two-input AND gate	16	D-type flipflop	112	128
Complex LCA300K function	Two 16-input AND gates plus two-input XOR gates	528	D-type flipflop	112	640

The product-term gate range is the total number of LSI gates used for simple functions and the total number of LSI gates used for complex functions. In this case, 128 gates are used for simple functions and 640 gates are used for complex functions.

ESB Look-Up Table Logic Gate Count

The range of ESB gates implemented in LUT logic can be determined for simple and complex functions by adding the number of ESB LUTs and ESB register gate equivalents. See Table 7.

Table 7. Calculating Embedded System LUT Gates Using LCA300K Functions

Implementation	16 ESB 7-Input LUTs	LSI Gates	23 ESB Registers	LSI Gates	Total
Simple LCA300K function	Two-input AND gate	16	D-type flipflop	161	177
Complex LCA300K function	Seven-input XOR gate	288	D-type flipflop with clear signal	184	472

The gate count of an ESB is determined by the LUT logic gate count and the product-term logic gate count. An APEX 20K ESB can implement 128 to 640 gates of logic, depending on the function and the type of logic used for the function. For estimating device gate count, the ESB is able to implement 128 gates.

For an APEX 20K device, the ESB array gate count can be determined by multiplying the number of ESBs with the number of gates per ESB. The following calculation shows how to determine the number of embedded array gates used as logic for an EP20K1000E device:

160 ESBs × 128 gates per ESB = 20,480 gates

An EP20K1000E device has approximately 20,500 embedded array gates when the ESBs are used for logic functions

Calculating System Gates

A key factor in determining gate count is the amount of memory used in the design. To determine the maximum system gate count for an EP20K1000E device, add the LE gate count to the ESB gate count. If ESBs are being used to implement both logic and memory, the percentage of ESBs that implement each function must figure into the gate count computation. Table 8 shows the system gate calculation method for an EP20K1000E device in which all ESB gates are implemented as memory.

Table 8. Calculating Maximum System Gate Count for an EP20K1000E Device

Gates	Gates × Percentage	Total Gates
LE gates	460,800 × 100%	460,800
ESB gates used as memory	1,310,720 × 100%	1,310,720
ESB gates used as logic	20,480 × 0%	0

To determine the maximum system gate count, the LE and ESB gate totals are added together.

Conclusion

The APEX 20K gate counting methodology is based on comparisons with the LSI Logic LCA300K family and on empirical data. The APEX 20K architecture contains an embedded array, which implements a variety of memory and complex logic functions, and a logic array that implements general logic functions. The combination of embedded system and logic arrays provides high performance for integrated System-on-a-Programmable-Chip applications.

Revision History

The information contained in *Application Note 110 (Gate Counting Methodology for APEX 20K Devices)* version 1.01 supersedes information published in previous versions. Version 1.01 contains the following changes:

- Updated system gate count in "Introduction" on page 1
- Added information on EP20K60E and EP20K1500E devices
- Updated Tables 1, 2, 3, and 8
- Minor textual changes throughout the document

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Customer Marketing:
(408) 544-7104
Literature Services:
(888) 3-ALTERA
lit_req@altera.com