AMERICAN MICROSYSTEMS, INC.

June 1997

## 1 Megabit (128K x8) CMOS Mask-Programmable ROM

## Features

- Fast Read Access Time - 70ns
- Low Power CMOS Operation
  – 20µA max. Standby
  – 15mA max. Active at 5MHz
- Wide Selection of JEDEC Standard Packages
  – 40-Lead 600-mil PDIP
  – 44-Pad PLCC
  – 40-Lead TSOP
  – 48-Lead TSOP
- 2.7V–3.6V Supply
- High Reliability CMOS Technology
  – 2000V ESD Protection
  – 200mA Latchup Immunity
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Full Commercial and Industrial Temperature Ranges
- Designed for Battery Supply Operation

## Description

The S63B1001 is a low-power, high performance 1,048,576 bit Mask Programmable Read Only Memory (ROM) organized 128K x 8 bits. It requires only one power supply in normal operation. Any word can be accessed in less than 70ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

The S63B1001 typically consumes 9mA. Standby mode supply current is typically less than 10µA.

The S63B1001 comes in a choice of industry standard JEDEC-approved packages including: plastic PDIP, PLCC, and TSOP. The device features two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 128K byte storage capability, the S63B1001 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media. AMI's S63B1001 has additional features to ensure high quality and efficient production use.

## Block Diagram
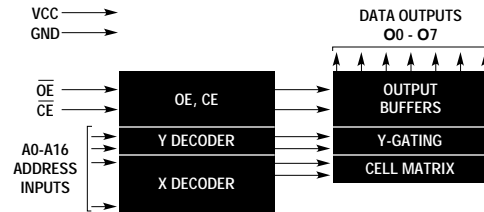


## Absolute Maximum Ratings[1]

| Temperature Under Bias | -55°C to +125°C |
|---|---|
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -2.0V to +6V[2] |

NOTE: 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent danger to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses less than 20ns. Maximum pin voltage is $V_{CC}$+0.6V DC which may overshoot to +6.0V for pulses of less than 20ns.

## Pin Configurations

| PIN NAME | FUNCTION |
|---|---|
| A0-A16 | Addresses |
| O0-O7 | Outputs |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| NC | No Connect |

## Pin Capacitance (f = 1 MHz T = 25°C)

| | TYPICAL | MAXIMUM | UNITS | CONDITIONS |
|---|---|---|---|---|
| $C_{IN}$ | 4 | 8 | pF | $V_{IN}$ = 0V |
| $C_{OUT}$ | 8 | 12 | pF | $V_{OUT}$ = 0V |

NOTE: Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

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### Operating Modes

| MODE/PIN | $\overline{CE}$ | $\overline{OE}$ | Ai | $V_{CC}$ | OUTPUTS |
|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | Ai | $V_{CC}$ | $D_{OUT}$ |
| Output Disable | X | $V_{IH}$ | X | $V_{CC}$ | High Z |
| Standby | $V_{IH}$ | X | X | $V_{CC}$ | High Z |

### DC and AC Operating Conditions

| | | S63B1001 | | |
|---|---|---|---|---|
| | | -70 | -90 | -120 |
| Operating Temperature | Commercial | 0°C - 70°C | 0°C - 70°C | 0°C - 70°C |
| | Industrial | -40°C - 85°C | -40°C - 85°C | -40°C - 85°C |
| $V_{dd}$ Power Supply | | 2.7V – 3.6V | 2.7V – 3.6V | 2.7V – 3.6V |

### DC and Operating Characteristics

#### 2.7V to 3.6V

| SYMBOL | PARAMETER | CONDITION | APP. | MIN | MAX | UNITS |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0V to $V_{CC}$ | Com., Ind. | | ±1 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0V to $V_{CC}$ | Com., Ind. | | ±5 | μA |
| $I_{SB}$ | $V_{CC}$ Standby Current | $\overline{CE}$ = $V_{CC}$ ± 0.3V | | | 20 | μA |
| $I_{CC}$ | $V_{CC}$ Active Current | f = 5MHz, $I_{OUT}$ = 0mA, $\overline{CE}$ = $V_{IL}$ ,$V_{CC}$ = 3.6V | Com. | | 15 | mA |
| | | | Ind. | | 20 | mA |
| $V_{IL}$ | Input Low Voltage | $V_{CC}$ = 3.0V to 3.6V | | | 0.8 | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | | 0.2 x $V_{CC}$ | V |
| $V_{IH}$ | Input High Voltage | $V_{CC}$ = 3.0V to 3.6V | | 2.2 | | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | 0.7 x $V_{CC}$ | | V |
| $V_{OL}$ | Output Low Voltage | 2mA | | | 0.4 | V |
| | | 100μA | | | 0.2 | V |
| | | 20μA | | | 0.1 | V |
| $V_{OH}$ | Output High Voltage | -1mA | | 2.2 | | V |
| | | -100μA | | $V_{CC}$ – 0.2 | | V |
| | | -20μA | | $V_{CC}$ – 0.1 | | V |

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## 1 Megabit (128K x8) CMOS Mask-Programmable ROM

## AC Characteristics for Read Operations

### 2.7V - 3.6V

| SYMBOL | PARAMETER | CONDITION | -70 | | -90 | | -120 | |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. |
| $t_{ACC}$[3] | Address to Output Delay | $\overline{CE}=\overline{OE}=V_{IL}$ | | 70ns | | 90ns | | 120ns |
| $t_{CE}$[2] | $\overline{CE}$ to Output Delay | $\overline{OE}=V_{IL}$ | | 70ns | | 90ns | | 120ns |
| $t_{OE}$[2,3] | $\overline{OE}$ to Output Delay | $\overline{CE}=V_{IL}$ | | 30ns | | 35ns | | 35ns |
| $t_{DF}$[4,5] | $\overline{OE}$ or $\overline{CE}$ High to Output Float | | | 25ns | | 25ns | | 30ns |
| $t_{OH}$ | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ whichever occurred first | | 0ns | | 0ns | | 0ns | |

## AC Waveforms[1]
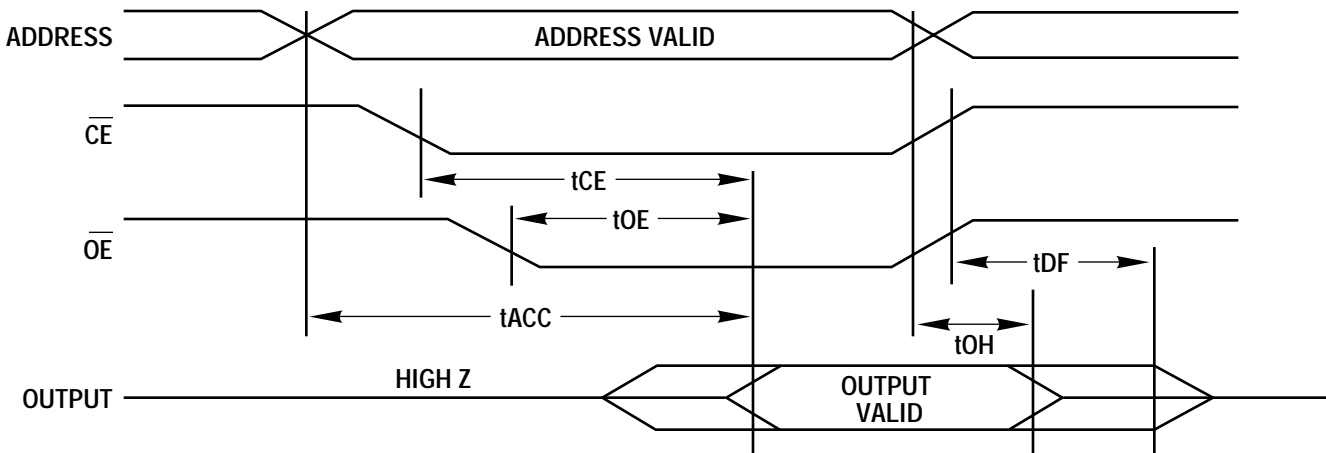


Notes: 1. Timing measurement references are 1.5V. Input AC driving levels are 0V and 2.7V.
2. $\overline{OE}$ may be delayed up to $t_{CE}$-$t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{CE}$.
3. $\overline{OE}$ may be delayed up to $t_{ACC}$-$t_{OE}$ after the address is valid without impact on $t_{ACC}$.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

## Input Test Waveforms and Measurement Levels
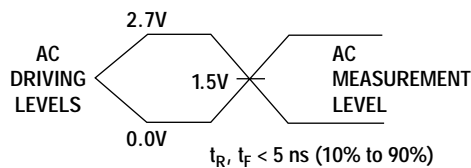


## Output Test Load
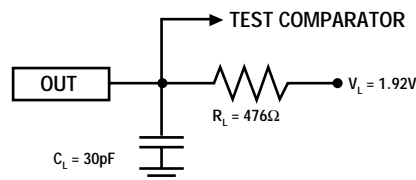
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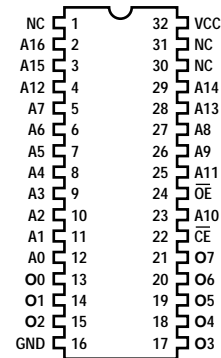# 1 Megabit (128K x8) CMOS Mask-Programmable ROM
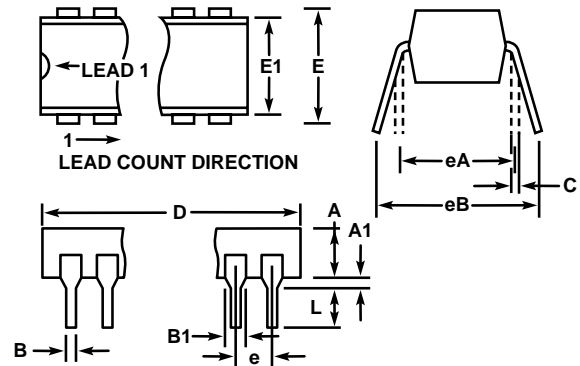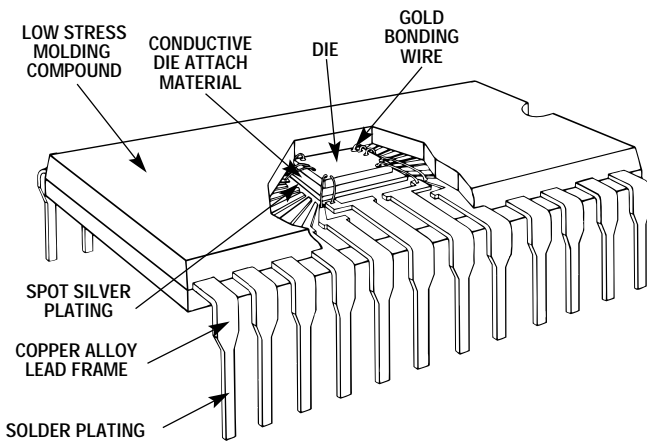
## 32-Pin PDIP Specifications

### Description

The Plastic Dual-In-Line Package (PDIP) meets widely accepted industry standard for MOS/VLSI applications. The package consists of a plastic body, transfer-molded around the leadframe and die. The leadframe is copper alloy, with external pins solder plated.

Internally, there is 125µ inch silver spot plating on the die attach pad and on each bonding fingertip. These fingers are electrically connected to the die by thermosonic gold ball bonding techniques.

## Pin Configuration

| | | | |
|---|---|---|---|
| NC | 1 | 32 | VCC |
| A16 | 2 | 31 | NC |
| A15 | 3 | 30 | NC |
| A12 | 4 | 29 | A14 |
| A7 | 5 | 28 | A13 |
| A6 | 6 | 27 | A8 |
| A5 | 7 | 26 | A9 |
| A4 | 8 | 25 | A11 |
| A3 | 9 | 24 | $\overline{OE}$ |
| A2 | 10 | 23 | A10 |
| A1 | 11 | 22 | $\overline{CE}$ |
| A0 | 12 | 21 | O7 |
| O0 | 13 | 20 | O6 |
| O1 | 14 | 19 | O5 |
| O2 | 15 | 18 | O4 |
| GND | 16 | 17 | O3 |

## Package Description and Outline Dimensions



## PDIP Specifications

| | SYMBOL | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A | A1 | B | B1 | C | D | E | E1 | e | eA | eB | L | B2 | S |
| MAX | 0.180 | - | 0.020 | 0.055 | 0.012 | 1.655 | 0.625 | 0.550 | 0.100 TYP | - | 0.686 | 0.135 | - | - |
| MIN | - | 0.015 | 0.016 | 0.045 | 0.008 | 1.645 | 0.600 | 0.530 | | 0.580 | - | 0.125 | - | - |

NOTE: 1. All measurements in inches.
2. Data is subject to change. Contact the factory for most current specifications.

# S63B1001

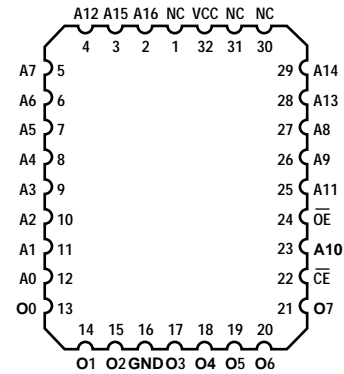## 1 Megabit (128K x8) CMOS Mask-Programmable ROM
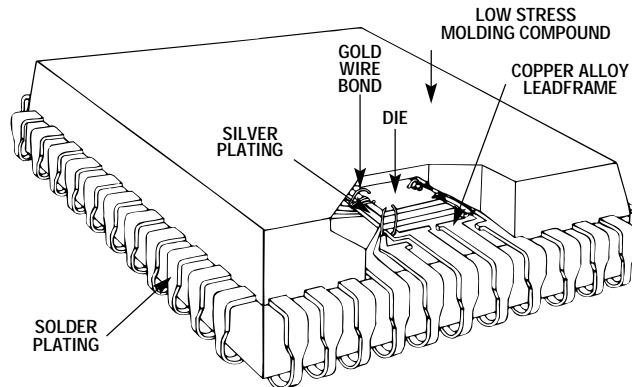
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## 32-Pin PLCC Specifications

### Description

The PLCC is transfer molded and thermosonic wire bonded. Die is mounted on a copper alloy leadframe and external leads are solder plated to provide improved solderability.
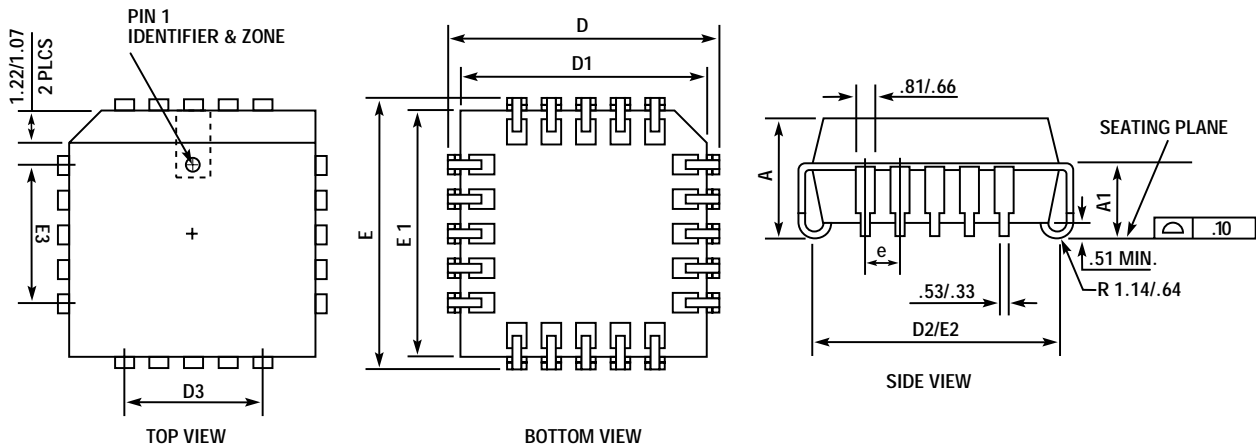
### Pin Configuration

```
        A12 A15 A16 NC VCC NC  NC
         4   3   2   1  32  31  30
   A7  5                          29  A14
   A6  6                          28  A13
   A5  7                          27  A8
   A4  8                          26  A9
   A3  9                          25  A11
   A2  10                         24  OE
   A1  11                         23  A10
   A0  12                         22  CE
   O0  13                         21  O7
        14  15  16  17  18  19  20
        O1  O2 GND O3  O4  O5  O6
```

## Package Description



LOW STRESS MOLDING COMPOUND
GOLD WIRE BOND
COPPER ALLOY LEADFRAME
DIE
SILVER PLATING
SOLDER PLATING

## Package Outline Dimensions



PIN 1 IDENTIFIER & ZONE
1.22/1.07 2 PLCS
TOP VIEW
BOTTOM VIEW
.81/.66
SEATING PLANE
.53/.33
.51 MIN.
R 1.14/.64
D2/E2
SIDE VIEW
.10

## PDIP Specifications

| | | SYMBOL | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **A** | **A1** | **D1** | **D2** | **D3** | **E1** | **E2** | **E3** | **e** | **D** | **E** |
| **MAX** | 3.56 | 2.41 | 11.51 | 10.92 | 7.62 BSC | 14.05 | 13.46 | 10.16 BSC | 1.27 BSC | 12.57 | 15.11 |
| **MIN** | 2.45 | 1.52 | 11.35 | 9.91 | | 13.89 | 12.45 | | | 12.32 | 14.86 |

NOTE: 1. All measurements in millimeters.

2. Data is subject to change. Contact the factory for most current specifications.

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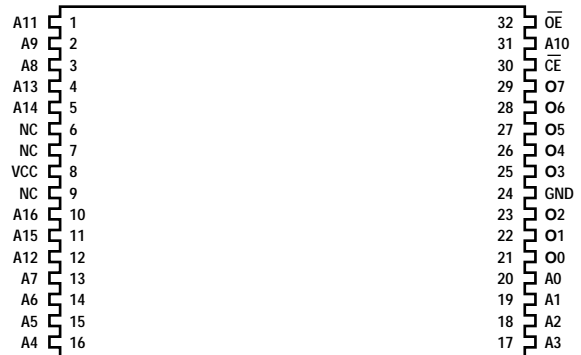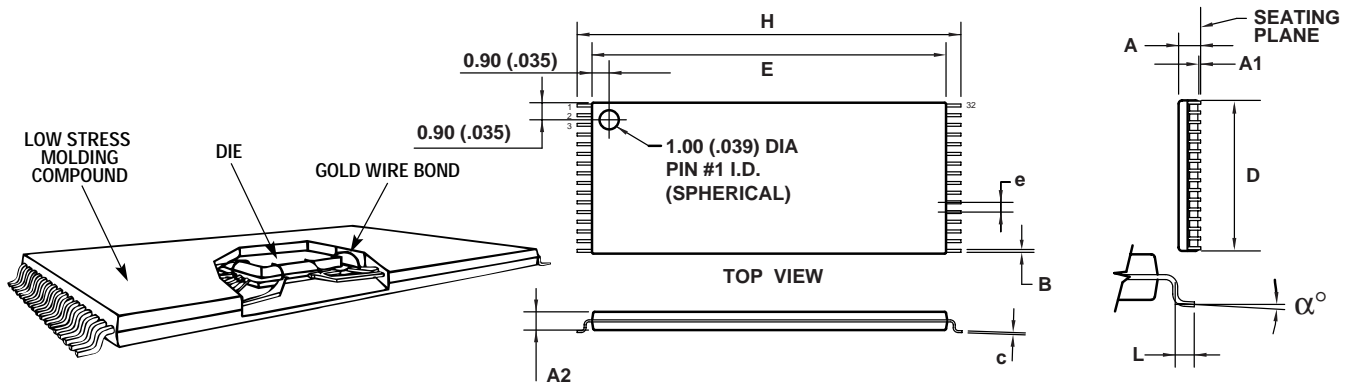## 1 Megabit (128K x8) CMOS Mask-Programmable ROM

## 32-Pin TSOP Specifications

### Pin Configuration

| | | | | |
|---|---|---|---|---|
| A11 | 1 | | 32 | $\overline{OE}$ |
| A9 | 2 | | 31 | A10 |
| A8 | 3 | | 30 | $\overline{CE}$ |
| A13 | 4 | | 29 | O7 |
| A14 | 5 | | 28 | O6 |
| NC | 6 | | 27 | O5 |
| NC | 7 | | 26 | O4 |
| VCC | 8 | | 25 | O3 |
| NC | 9 | | 24 | GND |
| A16 | 10 | | 23 | O2 |
| A15 | 11 | | 22 | O1 |
| A12 | 12 | | 21 | O0 |
| A7 | 13 | | 20 | A0 |
| A6 | 14 | | 19 | A1 |
| A5 | 15 | | 18 | A2 |
| A4 | 16 | | 17 | A3 |

### Description

The Type I Thin Small Outline Package (TSOP) is a thin, ends only package. This package is constructed using the latest low stress molding compounds and bonding technology to provide a package with total body thickness of less than 1.90mm.

This package is popular for ROM applications in memory cards and other thin card applications.

## Package Description and Outline Dimensions



## TSOP Specifications

| | A | A1 | A2 | B | D | E | H | e | c | L | α° |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **MAX** | 1.20 | 0.15 | 1.05 | 0.25 | 8.20 | 18.50 | 20.20 | 0.50 BSC | 0.20 | 0.60 | 5 |
| **MIN** | - | 0.0 | 0.95 | 0.15 | 7.80 | 18.30 | 19.80 | | 0.10 | 0.40 | 0 |

Header row above spans: **SYMBOL**

NOTE: 1. All measurements in millimeters.
   2. Data is subject to change. Contact the factory for most current specifications.

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