GOB512UV6432(A/B)-(60/70/80/10)Q-S

4MByte (512K x 64) CMOS Synchronous Graphic Module

General Description

The GOB512UV6432(A/B)-(60/70/80/10)Q-S are high performance, 4-megabyte synchronous, graphic RAM module organized as 512K words by 64 bits, in a 144-pin, small outline dual-in-line memory module (SODIMM) package.

The modules utilizes two Fujitsu MB81G163222-(60/70/80/10)TQ CMOS 512Kx32 synchronous graphic RAMs in surface mount package (TQFP) on an epoxy laminated substrate. Each device is accompanied by a decoupling capacitor for improved noise immunity.

Features

- High Density: 4MByte
- Cycle Time: 6ns (167MHz: -60), 7ns (143MHz: -70), 8ns (125MHz: -80), 10ns (100MHz: -10)
- Low Power: Active 3.2W (167MHz: -60), 2.7W (143MHz: -70), 2.4W (125MHz: -80), 2.0W (100MHz: -10)
- LVTTL-compatible inputs and outputs
- Separate power and ground planes to improve noise immunity
- Single power supply of 3.3V±0.3V
- Height: 1.150 inch

ABSOLUTE MAXIMUM RATINGS

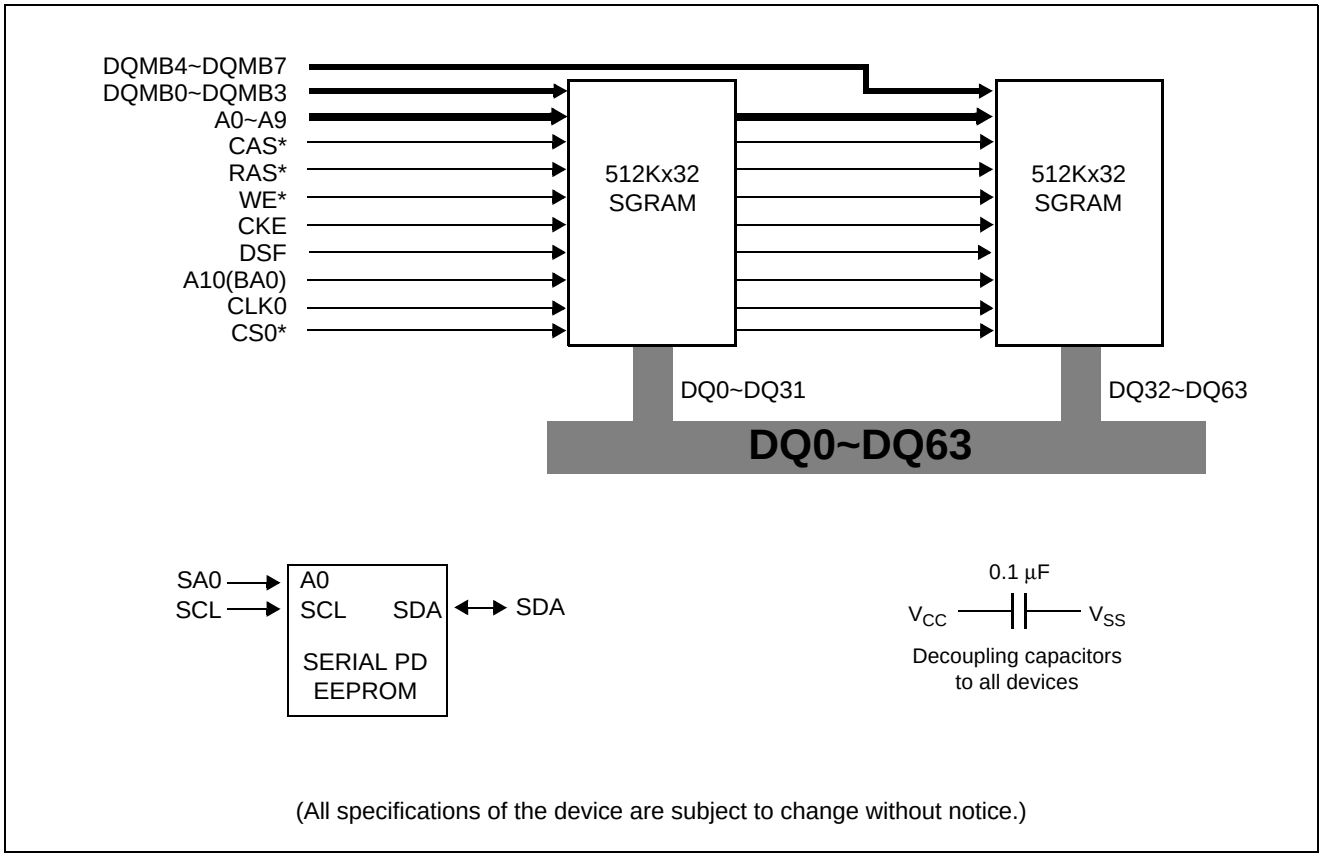
Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5 to +4.6	V
Power Dissipation	P_T	2.6	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperate	T_{stg}	-55 to +125	°C
Short Circuit Output Current	I_{OS}	±50	mA

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to +70 °C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High voltage	2.0	-	V_{CC}+0.5	V
V_{IL}	Input Low voltage	-0.5	-	0.8	V

Functional Diagram



Notes: 1. CLK,CKE,RAS*,CAS*,WE*,DSF and Address are terminated using 10Ω series resistors.

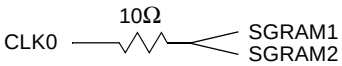
2. Data lines (DQ29~DQ31) have resistor strapping option of 4.7KΩ.

Speed Version	Cycle Time (Intel Rev.0.92)	DQ 31	DQ30	DQ29
-60 & -70	8 ns	0	1	1
-80	10 ns	0	1	0
-10	12 ns	0	0	1

0:Vss 1:Vcc

3. DQMs vs Data I/Os
DQMB0 controls DQ0 ~ DQ7
DQMB1 controls DQ8 ~ DQ15
DQMB2 controls DQ16 ~ DQ23
DQMB3 controls DQ24 ~ DQ31
DQMB4 controls DQ32 ~ DQ39
DQMB5 controls DQ40 ~ DQ47
DQMB6 controls DQ48 ~ DQ55
DQMB7 controls DQ56 ~ DQ63

4. Clock Wiring



Pin Name

A0~A9	Row Addresses	SA0	Decode Input
A0~A7	Column Addresses	CS0*	Chip Selects
A10(BA0)	Bank Select Address	WE*	Write Enable
DQ0~DQ63	Data Inputs/Outputs	SCL	Serial Clock
CLK0	Clock Inputs	SDA	Serial Data Input/Output
CKE	Clock Enable	DSF	Define Special Function
RAS*	Row Address Strobe	V_{CC}	Power Supply
CAS*	Column Address Strobe	V_{SS}	Ground
DQMB0-DQMB7	DQ Mask Enables	NC	No Connection

Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation
1	V_{SS}	2	V_{SS}	73	NC	74	CLK0
3	DQ63	4	DQ62	75	V_{CC}	76	V_{CC}
5	DQ61	6	DQ60	77	NC	78	NC
7	DQ59	8	DQ58	79	NC	80	A10(BA0)
9	DQ57	10	DQ56	81	A9	82	A8
11	V_{CC}	12	V_{CC}	83	A7	84	A6
13	DQ55	14	DQ54	85	V_{SS}	86	V_{SS}
15	DQ53	16	DQ52	87	A5	88	A4
17	DQ51	18	DQ50	89	A3	90	A2
19	DQ49	20	DQ48	91	A1	92	A0
21	V_{SS}	22	V_{SS}	93	V_{CC}	94	V_{CC}
23	DQMB7	24	DQMB6	95	DQ31	96	DQ30
25	DQMB5	26	DQMB4	97	DQ29	98	DQ28
27	V_{CC}	28	V_{CC}	99	DQ27	100	DQ26
29	DQ47	30	DQ46	101	DQ25	102	DQ24
31	DQ45	32	DQ44	103	V_{SS}	104	V_{SS}
33	DQ43	34	DQ42	105	DQ23	106	DQ22
35	DQ41	36	DQ40	107	DQ21	108	DQ20
37	V_{SS}	38	V_{SS}	109	DQ19	110	DQ18
39	DQ39	40	DQ38	111	DQ17	112	DQ16
41	DQ37	42	DQ36	113	V_{CC}	114	V_{CC}
43	DQ35	44	DQ34	115	DQMB3	116	DQMB2
45	DQ33	46	DQ32	117	DQMB1	118	DQMB0
47	V_{CC}	48	V_{CC}	119	V_{SS}	120	V_{SS}
49	NC	50	NC	121	DQ15	122	DQ14
51	NC	52	NC	123	DQ13	124	DQ12
53	NC	54	NC	125	DQ11	126	DQ10
55	V_{SS}	56	V_{SS}	127	DQ9	128	DQ8
57	DSF	58	NC	129	V_{CC}	130	V_{CC}
59	NC	60	NC	131	DQ7	132	DQ6
61	NC	62	SA0	133	DQ5	134	DQ4
63	V_{CC}	64	V_{CC}	135	DQ3	136	DQ2
65	NC	66	CS0*	137	DQ1	138	DQ0
67	RAS*	68	CAS*	139	V_{SS}	140	V_{SS}
69	WE*	70	CKE	141	SDA	142	SCL
71	V_{SS}	72	V_{SS}	143	V_{CC}	144	V_{CC}

Address Translation

SO-DIMM		512Kx32 SGRAM	
Pin No.	Pin Designation	Pin No.	Pin Designation
82	A8	51	A9
81	A9	29	A10
80	A10	30	A8

Serial PD Information

		Function Supported				Hex Value			
Byte#	**Function Described**	**167 Mhz (-60)**	**143 Mhz (-70)**	**125 Mhz (-80)**	**100 Mhz (-10)**		**143 Mhz (-70)**	**125 Mhz (-80)**	**100 Mhz (-10)**
0	# Bytes Written into serial memory at module mfr	128 bytes				80h			
1	Total # bytes of SPD memory device	256 bytes				08h			
2	Fundamental memory type	SGRAM				05h			
3	# Row Address on this assembly	10				0Ah			
4	# Column Addresses on this assembly	8				08h			
5	# Module Banks on this assembly	1				01h			
6	Data Width of this assembly	64 bits				40h			
7	Data Width of this assembly (continued)					00h			
8	Voltage interface standard of this assembly	LVTTL				01h			
9	SGRAM cycle time at CL=3 (tCLK)	6ns	7ns	8ns	10ns	60h	70h	80h	A0h
10	SGRAM Access from Clock at CL=3 (tAC)	5.5ns	6ns	7ns	7ns	55h	60h	70h	70h
11	DIMM configuration type	Non-Parity				00h			
12	Refresh Rate/Type	S/R, Normal 15.6 ms				80h			
13	SGRAM Width Primary DRAM	x32				20h			
14	ECC SGRAM Data Width	N/A				00h			
15	Min. clock delay, Back to Back Random Column Addresses (ICCD)	1CLK				01h			
16	Burst Length Supported	1, 2, 4, 8 & Full				8Fh			
17	# Banks on each SGRAM device	2				02h			
18	CAS# Latency	2, 3				06h			
19	CS# Latency	0				01h			
20	Write Latency	0				01h			
21	SGRAM Module Attribute	Non-Buffered/Registered				00h			
22	SGRAM Device Attribute	Vcc, B/R, S/W, P/A, A/P				0Eh			
23	Min Clock cycle Time at CL=2 (tCLK)	N/A	10ns	12ns	15ns	00h	A0h	C0h	F0h
24	Max. Data Access Time from clock at CL=2 (tAC)	N/A	9ns	10ns	12ns	00h	90h	A0h	C0h
25	Min Clock cycle Time at CL=1 (tCLK)	N/A				00h			
26	Max. Data Access Time from clock at CL=1 (tAC)	N/A				00h			
27	Min. Row Precharge Time (tRP)	18ns	21ns	24ns	30ns	12h	15h	18h	1Eh
28	Min. Row Active Delay (tRRD)	12ns	14ns	16ns	20ns	0Ch	0Eh	10h	14h
29	Min. RAS to CAS Delay (tRCD)	18ns	21ns	24ns	30ns	12h	15h	18h	1Eh
30	Min. RAS Pulse Width (tRAS)	36ns	42ns	48ns	60ns	24h	2Ah	30h	3Ch
31	Module Bank Density	N/A				00h			
32	Input Setup Time (tSI) for Add. & CMD	2.0ns	2.0ns	2.5ns	3.0ns	20h	20h	25h	30h
33	Input Hold Time (tHI) for Add. & CMD	1.0ns	1.0ns	1.0ns	1.0ns	10h	10h	10h	10h
34	Input Setup Time (tSI) for Data	2.0ns	2.0ns	2.5ns	3.0ns	20h	20h	25h	30h
35	Input Hold Time (tHI) for Data	1.0ns	1.0ns	1.0ns	1.0ns	10h	10h	10h	10h
36	Write Block Size	8 Columns				03h			
37-61	Superset Information					00h			
62	SPD Revision	Rev. 1.2				12h			
63	Checksum for bytes 0-62								

SERIAL PD INFORMATION (CONTINUED)

		Function Supported				Hex Value			
Byte#	Function Described	167 Mhz (-60)	143 Mhz (-70)	125 Mhz (-80)	100 Mhz (-10)	167 Mhz (-60)	143 Mhz (-70)	125 Mhz (-80)	100 Mhz (-10)
64	Manufacturers JEDEC ID code per JEP-106E	Continuation code				7Fh			
65	Manufacturers JEDEC ID code per JEP-106E	SMART's ID				94h			
66-71	Manufacturers JEDEC ID code per JEP-106E	None				FFh			
72	Manufacturing location	Mfr Specific Data							
73	Manufacturer's Part Number	G				47h			
74	Manufacturer's Part Number	O				4Fh			
75	Manufacturer's Part Number	B				42h			
76	Manufacturer's Part Number	5				35h			
77	Manufacturer's Part Number	1				31h			
78	Manufacturer's Part Number	2				32h			
79	Manufacturer's Part Number	U				55h			
80	Manufacturer's Part Number	V				56h			
81	Manufacturer's Part Number	6				36h			
82	Manufacturer's Part Number	4				34h			
83	Manufacturer's Part Number	3				33h			
84	Manufacturer's Part Number	2				32h			
85	Manufacturer's Part Number	6	7	8	1	36h	37h	38h	31h
86	Manufacturer's Part Number	0	0	0	0	30h	30h	30h	30h
87	Manufacturer's Part Number	Q	Q	Q	Q	51h	51h	51h	51h
88	Manufacturer's Part Number	S	S	S	S	53h	53h	53h	53h
89	Manufacturer's Part Number	None	None	None	None	FFh	FFh	FFh	FFh
90	Manufacturer's Part Number	None	None	None	None	FFh	FFh	FFh	FFh
91	Revision Code	Mfr Specific Data				Mfr Specific Data			
92	Revision Code	None				FFh			
93	Manufacturing Date	DATE				DATE			
94	Manufacturing Date	DATE				DATE			
95-98	Assembly Serial Number	Serial Number				S.No.			
99	Manufacturer Specific Data	S				53h			
100	Manufacturer Specific Data	M				4Dh			
101	Manufacturer Specific Data	A				41h			
102	Manufacturer Specific Data	R				52h			
103	Manufacturer Specific Data	T				54h			
104	Manufacturer Specific Data	M				4Dh			
105	Manufacturer Specific Data	o				6Fh			
106	Manufacturer Specific Data	d				64h			
107	Manufacturer Specific Data	u				75h			
108	Manufacturer Specific Data	l				6Ch			
109	Manufacturer Specific Data	a				61h			
110	Manufacturer Specific Data	r				72h			
111	Manufacturer Specific Data	T				54h			
112	Manufacturer Specific Data	e				65h			
113	Manufacturer Specific Data	c				63h			
114	Manufacturer Specific Data	h				68h			
115	Manufacturer Specific Data	n				6Eh			
116	Manufacturer Specific Data	o				6Fh			
117	Manufacturer Specific Data	l				6Ch			
118	Manufacturer Specific Data	o				6Fh			
119	Manufacturer Specific Data	g				67h			
120	Manufacturer Specific Data	i				69h			
121	Manufacturer Specific Data	e				65h			
122	Manufacturer Specific Data	s				73h			
123	Manufacturer Specific Data	None				FFh			
124	Manufacturer Specific Data	None				FFh			
125	Manufacturer Specific Data	None				FFh			
126	Intel Spec Frequency	66MHz				66h			
127	Intel Spec Detail for 100MHz	1000-1111				8Fh			
128-255	Open for CPQ Use for Read & Write	None				FFh			

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted) Notes 1,2

Parameter		Symbol	Conditions	Value		Unit
				Min.	Max.	
Output High Voltage		$V_{OH(DC)}$	I_{OH} = -2mA	2.4	-	V
Output Low Voltage		$V_{OL(DC)}$	I_{OL} = 2mA	-	0.4	V
Input Leakage Current (Any Input)		I_{LI}	0V ≤ V_{IN} ≤ V_{CC}; All other pins not under test = 0V	-20	20	µA
Output Leakage Current		I_{LO}	0V ≤ V_{IN} ≤ V_{CC} D_{out} = Disable	-10	10	µA
Operating Current (Average Power Supply Current)	-60	I_{CC1S}	Burst: Length=4, t_{RC} = min. t_{CK} = min. at each operation (*8) One bank active, Outputs open, Addresses are changed up to 3 times during t_{RC} (min), 0V ≤ V_{in} ≤ V_{CC}	-	600	mA
	-70				500	
	-80				460	
	-10				380	
Operating Current (Average Power Supply Current)	-60	I_{CC1D}	Burst: Length=4, t_{RC} = min. t_{CK} = min. at each operation (*8) Two banks active, Outputs open, Addresses are changed up to 3 times during t_{RC} (min), 0V ≤ V_{in} ≤ V_{CC}	-	900	mA
	-70				760	
	-80				680	
	-10				560	
Precharge Standby Current (Power Supply Current)		I_{CC2P}	CKE=V_{IL}, All banks idle, t_{CK}=min, Power down mode, 0V ≤ V_{in} ≤ V_{CC}	-	8	mA
		I_{CC2PS}	CKE=V_{IL}, All banks idle, CLK=V_{IH} or V_{IL}, Power down mode, 0V ≤ V_{in} ≤ V_{CC}	-	6	
Precharge Standby Current (Power Supply Current)		I_{CC2N}	CKE=V_{IH}, All banks idle, t_{CK}=min, NOP commands only, Input signals are changed one time during 3 clock cycles, 0V ≤ V_{in} ≤ V_{CC}	-	110	mA
Precharge Standby Current (Power Supply Current)		I_{CC2NS}	CKE=V_{IH}, All banks idle, CLK=V_{IH} or V_{IL}, Input signals are stable, 0V ≤ V_{in} ≤ V_{CC}	-	40	

(Continued)

Parameter		Symbol	Test Condition	Value		Unit
				Min.	Max.	
Active Standby Current (Power Supply Current)		I_{CC3P}	CKE=V_{IL}, Any bank active, t_{CK}=min, 0V ≤ V_{in} ≤ V_{CC}	-	40	mA
		I_{CC3PS}	CKE=V_{IL}, Any bank active, CLK = V_{IH} or V_{IL}, 0V ≤ V_{in} ≤ V_{CC} Input signals are stable	-	40	mA
		I_{CC3N}	CKE=V_{IH}, Any bank active, t_{CK}=min, NOP commands only, Input signals are changed one time during 3 clock cycles, 0V ≤ V_{in} ≤ V_{CC}	-	180	mA
		I_{CC3NS}	CKE=V_{IH}, Any bank active, CLK = V_{IH} or V_{IL}, 0V ≤ V_{in} ≤ V_{CC} Input signals are stable	-	60	mA
Burst mode Current (Average Power supply current)	-60	I_{CC4}	t_{CK}=min, Burst length=4, Outputs open, Multiple-banks active, Gapless data, 0V ≤ V_{in} ≤ V_{CC} Adresses are changed only one time during $t_{CK\ (min.)}$	-	680	mA
	-70				580	
	-80				520	
	-10				440	
Refresh Current #1 (Average Power Supply Current)	-60	I_{CC5}	Auto-refresh; t_{CK}=min, t_{RC}=min, 0V ≤ V_{in} ≤ V_{CC}	-	560	mA
	-70				480	
	-80				420	
	-10				360	
Refresh Current #2 (Average Power Supply Current)		I_{CC6}	Self-refresh; t_{CK}=min, CKE ≤ 0.2V, 0V ≤ V_{in} ≤ V_{CC}	-	8	mA
Block Write Current (Average Power Supply Current)	-60	I_{CC7}	Block Write; t_{CK}=min, t_{BWC}=min, 0V ≤ V_{in} ≤ V_{CC}	-	640	mA
	-70				540	
	-80				480	
	-10				420	

†CL = CAS* Latency

Notes: 1. I_{CC} depends on the output termination or load conditions, clock cycle rate, and signal clocking rate; The specified values are obtained with the output open and no termination register.

2. An initial pause (DESL or NOP) of 200 μs is required after power-up followed by a minimum of eight Auto-refresh cycles.

CAPACITANCE

(TA =+25°C, VCC = 3.3V±0.3V)

Parameter	Symbol	Max.	Unit	Note
Input Capacitance (Address, WE*, CKE, RAS*, CAS*)	C_{I1}	15	pF	1
Input Capacitance (DQMBs)	C_{I2}	10	pF	1
Input Capacitance (CS0*)	C_{I3}	15	pF	1
Input Capacitance (CLK0)	C_{I4}	15	pF	1
Input/Output Capacitance (DQ0~DQ63)	$C_{I/O}$	12	pF	1, 2

Notes: 1. Capacitance is measured with Boonton Meter or effective capacitance method.
2. CAS* - V_{IH} to disable D_{out}.

AC CHARACTERISTICS (MB81G163222)

(At recommended operation conditions unless otherwise noted)

Parameter		Symbol	Unit	MB81G163222-60		MB81G163222-70		MB81G163222-80		MB81G163222-10		Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Period	CL=2	t_{CK}	ns	-	-	10	-	12	-	15	-	2,3,4
	CL=3			6		7		8		10	-	
Clock High Time		t_{CH}	ns	2.5	-	2.5	-	3	-	3.5	-	2,3,4
Clock Low Time		t_{CL}	ns	2.5	-	2.5	-	3	-	3.5	-	2,3,4
Data Input Setup Time		t_{DS}	ns	2	-	2	-	2.5	-	3	-	2,3,4
Data Input Hold Time		t_{DH}	ns	1	-	1	-	1	-	1	-	2,3,4
Address Setup Time		t_{AS}	ns	2	-	2	-	2.5	-	3	-	2,3,4
Address Hold Time		t_{AH}	ns	1	-	1	-	1	-	1	-	2,3,4
CKE Setup Time		t_{CKS}	ns	2	-	2	-	2.5	-	3	-	2,3,4
CKE Hold Time		t_{CKH}	ns	1	-	1	-	1	-	1	-	2,3,4
Command Setup Time (CS, RAS, CAS, WE, DSF, DQM)		t_{CMS}	ns	2	-	2	-	2.5	-	3	-	2,3,4
Command Hold Time (CS, RAS, CAS, WE, DSF, DQM)		t_{CMH}	ns	1	-	1	-	1	-	1	-	2,3,4
Access Time from Clock (t_{CK}=min.)	CL=2	t_{AC}	ns	-	-	-	9	-	10	-	12	2,3,4
	CL=3			-	5.5	-	6	-	7	-	7	
Output In Low-Z		t_{LZ}	ns	0	-	0	-	0	-	0	-	2,3,4
Output in High-Z	CL=2	t_{HZ}	ns	-	-	2	9	2	10	2	12	2,3,4,5
	CL=3			2	5.5	2	6	2	7	2	7	
Output Hold Time		t_{OH}	ns	2	-	2	-	2	-	2	-	2,3,4
Time between Refresh		t_{REF}	ms	-	32.8	-	32.8	-	32.8	-	32.8	2,3,4
Transition Time		t_T	ns	0.5	2	0.5	2	0.5	2	0.5	2	2,3,4
Power-down Exit Time		t_{PDE}	ns	2.5	-	3	-	3.5	-	4	-	2,3,4

AC CHARCTERISTICS (CONTINUED)

BASE VALUES FOR CLOCK COUNT/LATENCY

Parameter	Symbol	Unit	MB81G163222-60		MB81G163222-70		MB81G163222-80		MB81G163222-10		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{RAS}$ Cycle Time	t_{RC}	ns	54	-	63	-	72	-	90	-	2,3,4,6
$\overline{RAS}$ Precharge Time	t_{RP}	ns	181	-	21	-	24	-	30	-	2,3,4
$\overline{RAS}$ Active Time	t_{RAS}	ns	36	100000	42	100000	48	100000	60	100000	2,3,4
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	ns	18	-	21	-	24	-	30	-	2,3,4
Write Recovery Time	t_{WR}	ns	6	-	7	-	8	-	10	-	2,3,4
Data-in to Precharge Lead Time	t_{DPL}	ns	6	-	7	-	8	-	10	-	2,3,4
Data-in to Active/Refresh Command Period	t_{DAL}	ns	1 cyc + tRP	-	1 cyc + tRP	-	1 cyc + tRP	-	1 cyc + tRP	-	2,3,4
Block Write Data-in to Precharge Lead Time	t_{BPL}	ns	14	-	14	-	16	-	20	-	2,3,4
RAS to RAS Bank Active Delay Time	t_{RRD}	ns	12	-	14	-	16	-	20	-	2,3,4
Block Write Cycle Time	t_{BWC}	ns	12	-	14	-	16	-	20	-	2,3,4
Mode and Special Mode Register Cycle Time	t_{RSC}	ns	12	-	14	-	16	-	20	-	2,3,4
Mode and Special Mode Register Cycle Time	t_{RSC}	ns	2 cyc + tRP	-	2 cyc + tRP	-	2 cyc + tRP	-	2 cyc + tRP	-	2,3,4

CLOCK COUNT FORMULA

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \quad \text{(Round off a whole number)}$$

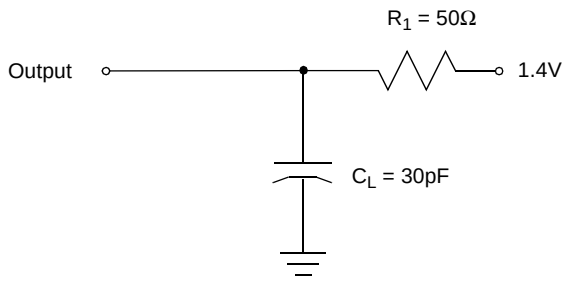
LATENCY-FIXED VALUES: MB81G163222

(The latency values on these parameters are fixed regardless of clock period)

Parameter		Symbol	Unit	MB81G163222-60	MB81G163222-70	MB81G163222-80	MB81G163222-10
CKE to Clock Disable		l_{CKE}	cycle	1	1	1	1
DQM to Output in High-Z		l_{DQZ}	cycle	2	2	2	2
DQM to Input Data Delay		l_{DQD}	cycle	0	0	0	0
Last Output to Write Command Delay		l_{OWD}	cycle	2	2	2	2
Write Command to Input Data Delay		l_{DWD}	cycle	0	0	0	0
Precharge to Output in High-Z Delay	CL = 2	l_{ROH}	cycle	-	2	2	2
	CL = 3			3	3	3	3
Burst Stop Command to Output in High-Z Delay	CL = 2	l_{BSH}	cycle	-	2	2	2
	CL = 3			3	3	3	3
$\overline{CAS}$ to $\overline{CAS}$ Delay (min.)		l_{CCD}	cycle	1	1	1	1
$\overline{CAS}$ Bank Delay (min.)		l_{CBD}	cycle	1	1	1	1

Notes:
1. I_{CC} depends on the output termination or load conditions, clock cycle rate, and signal clocking rate; The specified values are obtained with the output open and no termination register.
2. An initial pause (DESL or NOP) of 200µs is required after power-up followed by a minimum of eight Auto-refresh cycles.
3. AC characteristics assume t_T = 1 ns and 30 pF of capacitive load.
4. 1.4 V is the reference level for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max).
5. Specified where output buffer is no longer driven.

Fig. 1 - EXAMPLE OF AC TEST LOAD CIRCUIT

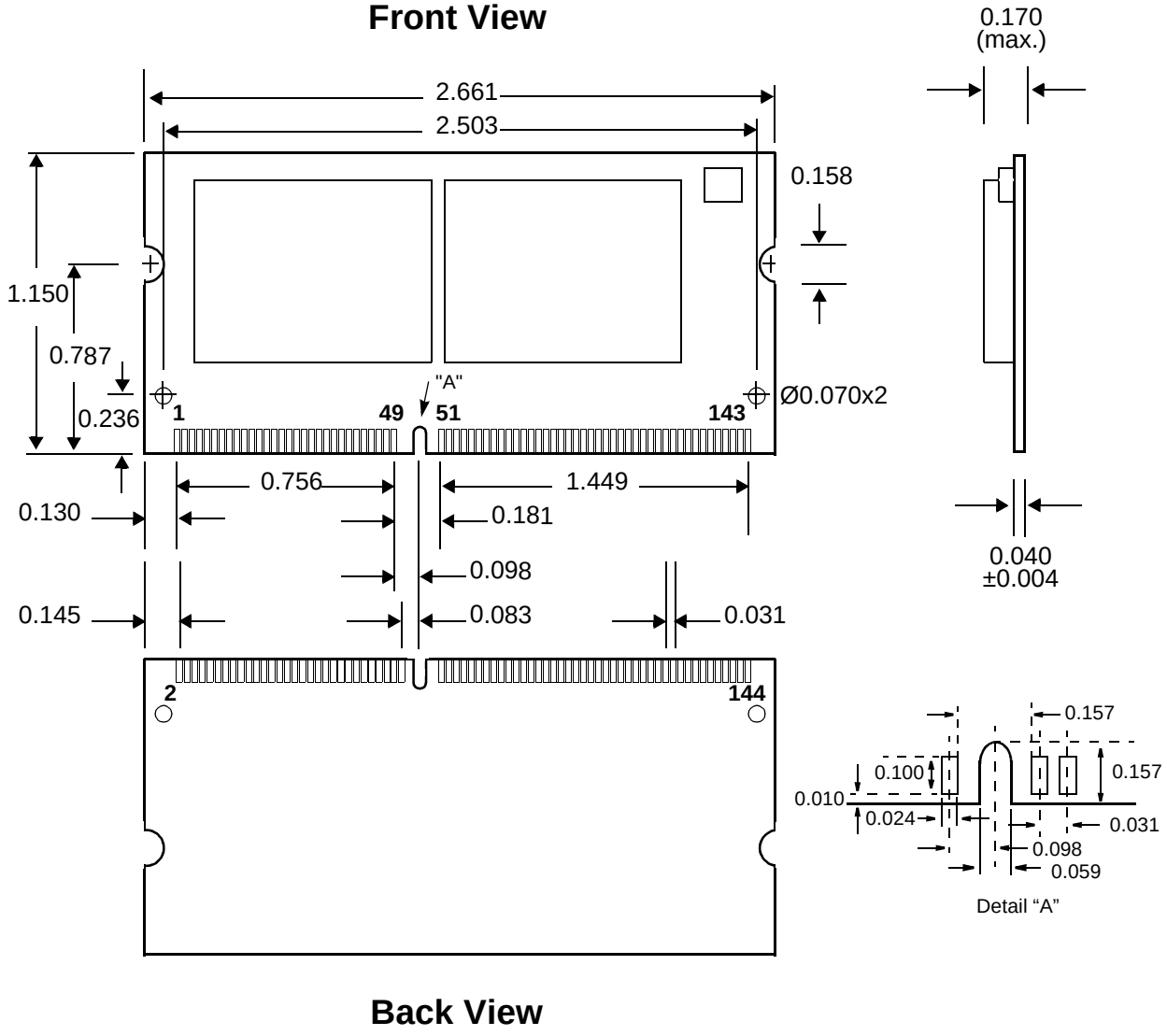


LVTTL

Note: AC characteristics are measured in this condition. This load circuits are not applicable for V_{OH} and V_{OL}.

Physical Dimensions

144-pin (72x2) DIMM



Back View

(All dimensions are in inches with 0.005" tolerance unless otherwise specified. Drawing not to scale.)

Ordering Information

G O B 512 U V 64 3 2 A - 60 Q - S

(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11) (12) (13)

(1) **Memory Type**
S : SDRAM
G : SGRAM

(2) **Module Shape**
S : SIMM
D : DIMM
O : Small Outline DIMM

(3) **Module Pin Count**
A : 72-pin
B : 144-pin
C : 168-pin
D : 184-pin
E : 200-pin

(4) **Word Depth**
1 : 1M
2 : 2M
4 : 4M
8 : 8M
256 : 256K
512 : 512K

(5) **Buffer Type**
B : Buffered
U : Unbuffered

(6) **Operating Voltage & Power Consumption**
V : 3.3V & LVTTL & Standard Power
L : 3.3V & LVTTL & Low Power
S : 3.3V & SSTL & Standard Power

(7) **Data Width**
(ex. 64=x64, 72=x72 etc.)

(8) **Device Configuration**
4 : x4
8 : x8
1 : x16
3 : x32

(9) **Refresh**
1 : 1kR
2 : 2kR

(10) **Module Revision / Applied "Standard" *1**
Blank : Rev. 0
A : Rev. 1
B : Rev. 2 (etc.)

*1 When DRAM device or PCB is revised, the revision is changed

(11) **Clock Frequency**
70 : 143Mhz
80 : 125Mhz
10 : 100Mhz

(12) **Package of Component**
J : SOJ
T : TSOP
Q : QFP/TQFP

(13) **Assembly & Test Site**
S : Smart Modular Technologies

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Memory Marketing Dept.
4-1-1, Kamikodanaka Nakahara-ku,
Kawasaki 211-88, Japan
Tel: +81-44-754-3767
Fax: +81-44-754-3343

Internet: http://www.fujitsu.co.jp/

North and South America

FUJITSU MICROELECTRONICS, INC.
3545 North First Street
San Jose, CA 95134-1804, USA.
Tel: +1-408-922-9000
Fax: +1-408-922-9179

Customer Response Center (Mon-Fri: 7am-5pm (PST))
Tel: +1-800-866-8608
Fax: +1-408-922-9179

Internet: http://www.fujitsumicro.com/

Europe

FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
63303 Dreieich–Buchschlag
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

Internet: http://www.fujitsu-ede.com/

Asia

FUJITSU MICROELECTRONICS ASIA PTE LIMITED
#05-08, 151 Lorong Chuan
NewTechPark
Singapore 556741
Tel: +65-281-0770
Fax: +65-281-0220

Internet: http://www.fmap.com.sg/

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