TOSHIBA

32-Bit TX System RISC

TX39 Family

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The TX39 high-performance RISC microprocessor family, designed for incorporation into systems, is a family of 32-bit original Toshiba processors based on the R3000A architecture designed by MIPS Technologies, Inc. Using the high-speed TX39/H version of the TX39 Core as the CPU core in gate arrays and cell-based ICs yields highly integrated systems.

High-performance core based on RISC technology

- R3000A architecture
- TX39/H processing performance: 74 MIPS (at 70 MHz)
  TX39 processing performance: 52 MIPS (at 50 MHz)
  Equivalent to Dhrystone 2.1 VAX-11/780
- Built-in cache memory
  Separate instruction and data caches
- Non-blocking load function
  During cache refill instructions which follow are executed.
- DSP functions
  Executes 32-bit sum-of-products arithmetic operations in a single clock cycle.

Improved software development environment

- C/C++ compiler and assembly language tools
- Real-time debugger system connection
  Enables real-time debugging when cache ON specified.
- Supports a wide range of real-time OSs.
- Standard board for evaluation and user applications

Functions optimized for embedded systems

- Code size reduced, performance improved
  Branch-Likely instruction supported
  Hardware interlock mechanism
- Improved real-time operation
  Cache-lock function
- Range of middleware supplied:
  e.g. JPEG, MH/MR/MMR, SoftModem

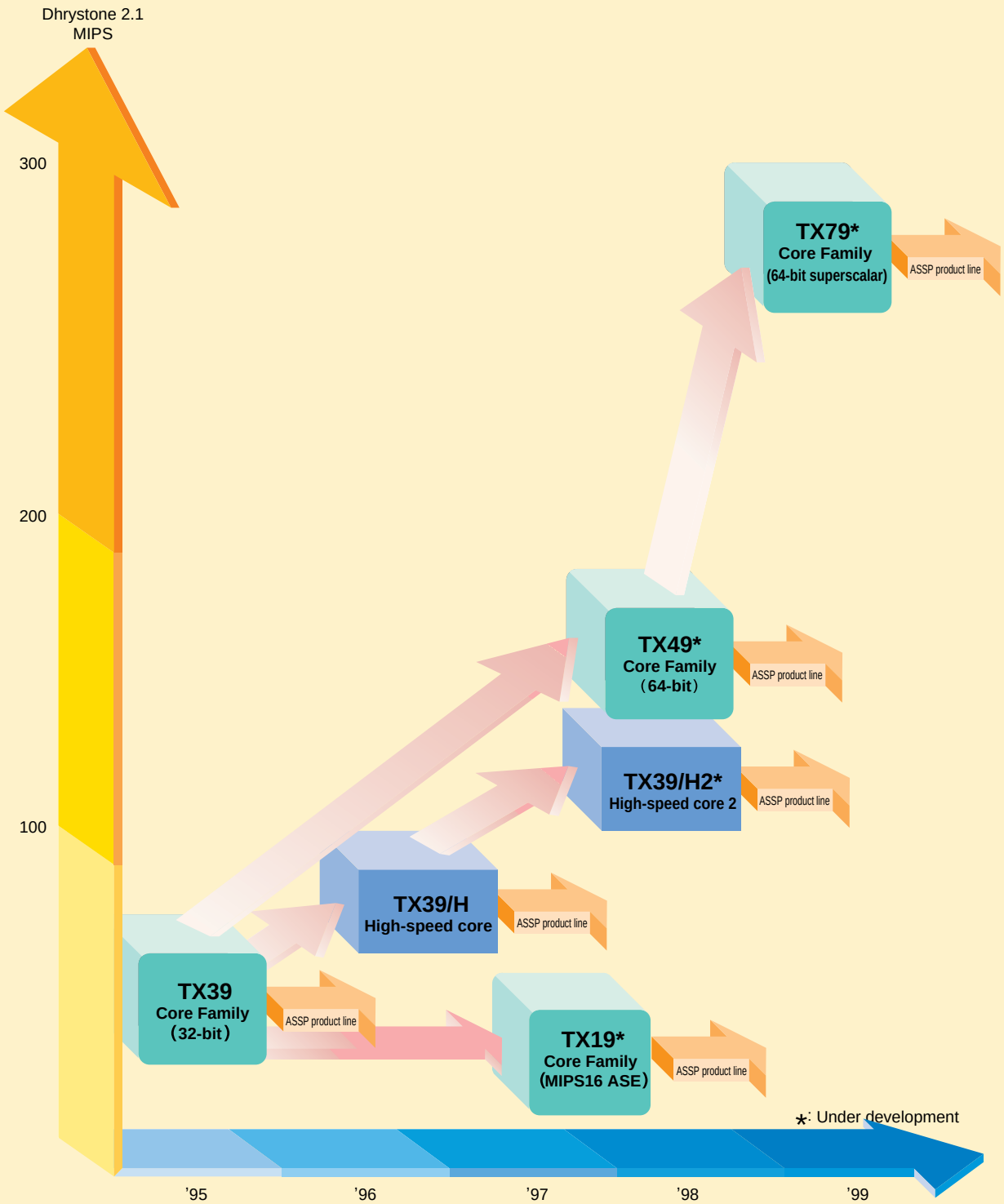
Low power dissipation

- Low power dissipation modes
- Clock can be stopped.

Can be used as ASIC CPU core

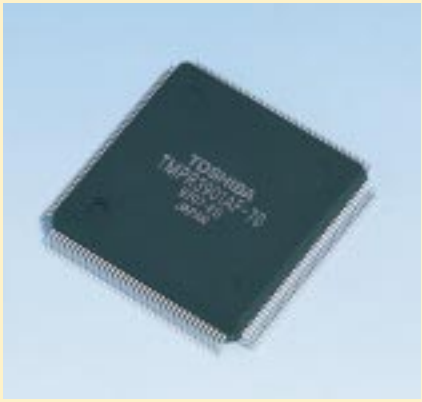
- TX39 Core RTL model supplied
- Megacell peripheral circuits supported
- TX39/H: TC220C-equivalent performance
  TX39: TC200C-equivalent performance

TX System RISC Road Map



TMPR3901AF-70

The TMPR3901AF is a member of the TX39 Family. Designed for incorporation into systems and devices, the TX39 Family is made up of a range of 32-bit RISC processors which use the original TX39 microprocessor core developed by Toshiba, based on the MIPS Group's R3000A architecture.
The TMPR3901AF uses the TX39/H core, which can operate at low voltage and which minimizes power consumption.



Functions specially designed for embedded use and high performance

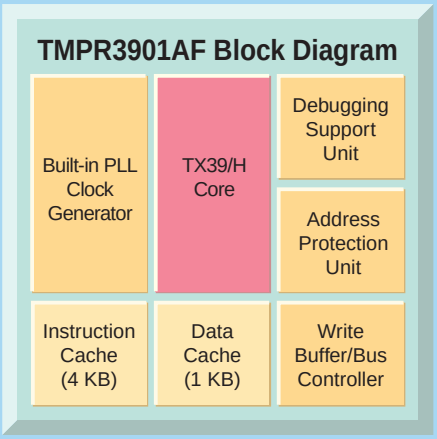
- 74 MIPS @70 MHz
  Equivalent to Dhrystone 2.1 VAX-11/780
- MIPS RISC architecture
  Developed by Toshiba based on the R3000A
- DSP functions
  Executes 32-bit sum-of-products arithmetic operations in a single clock cycle.
- Half-Speed Bus Mode
  Bus frequency can be halved.

Low power dissipation design suitable for portable equipment

- Supply voltage 3.3 V, 600 mW @70 MHz
- Low power dissipation modes
  Doze and Halt Modes to reduce power dissipation when idle;
  RF function to reduce operating frequency
- Clock can be stopped.

Configuration

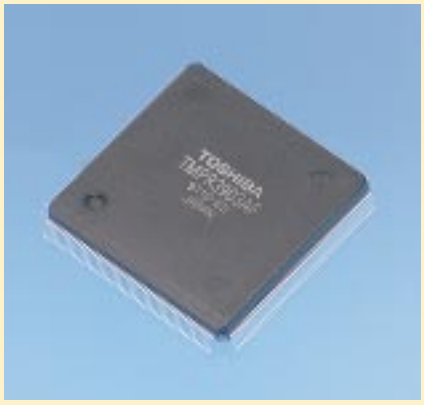
- 32-bit RISC core: TX39/H core
- Instruction cache: 4 KB
- Data cache: 1 KB
- Internal 8× PLL clock generator
- Debugging support unit
- Address protection unit (2 channels)
- Four-stage write buffer



TMPR3903AF

Based on the TX39 processor core, the TMPR3903AF is a high-performance 32-bit single-chip RISC ASSP whose features include a memory controller and graphic control functions suitable for car navigation systems.

The TMPR3903AF is designed to speed up car navigation systems while reducing their size and cost. Because of its built-in graphic control functions, the TMPR3903AF can also be used in the display panels of personal digital assistants (PDAs), electronic musical instruments, karaoke machines, factory automation equipment and any other similar devices which require miniature color display functions.



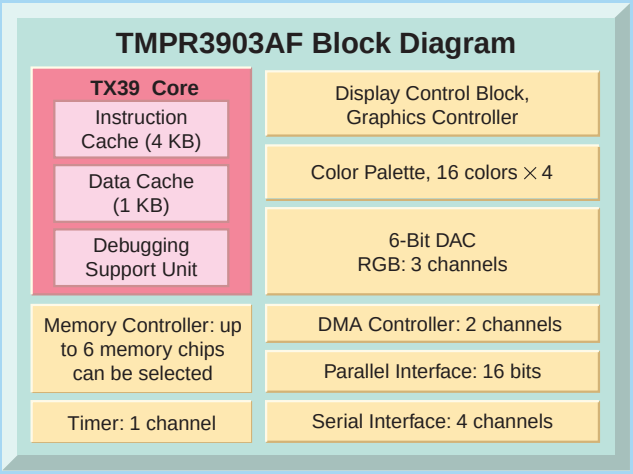
Features

- Based on the TX39 32-bit RISC core
- Instruction cache: 4 KB; Data cache: 1 KB
- Sum-of-products arithmetic operations: executed in a single clock cycle
- Operating frequency: 40 MHz (external 10 MHz)
- Package: 208-pin QFP
- Supply voltage: 3.3 V ± 0.3 V
- Maximum power dissipation: 800 mW
- Operating temperature: -40° to 85°C

■ Graphic control functions

- Supports DRAM frame buffer structure.
  - Unified memory architecture
  - Generates RAS/CAS signal.
  - High-speed Hyper Page Mode for reading display data
  - 32-dot internal buffer
- Four-plane overlay hardware processing
  - A level: 16 out of 65,536 colors or natural picture (16 bits per pixel)
  - B to D levels: 16 out of 65,536 colors (including one transparent color)
  - Colors can be individually set for each level (A to D).
- Sync display signal generation (HSYNC, VSYNC, CSYNC)
- Internal color palette and video DAC: 3 channels

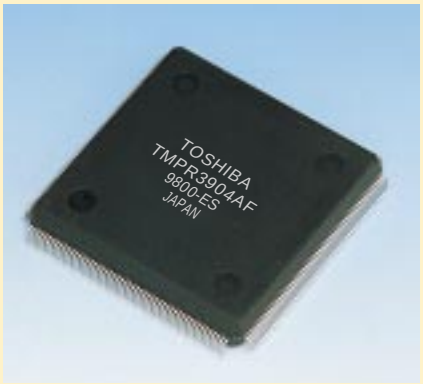
TMPR3903AF Block Diagram



TMPR3904AF-66

New Product

Based on the TX39/H processor core, the TMPR3904AF is a 32-bit, single-chip RISC microcontroller with general-purpose peripherals. Incorporating such peripherals as a memory controller, DMAC, UART and timers, the TMPR3904AF requires few external components for its application circuits. The ROM and DRAM controllers support both 16-bit and 32-bit width memory and enable the TMPR3904AF to meet performance and cost requirements flexibly. The TMPR3904AF is ideal for high-speed processing applications such as digital copiers and set-top boxes.



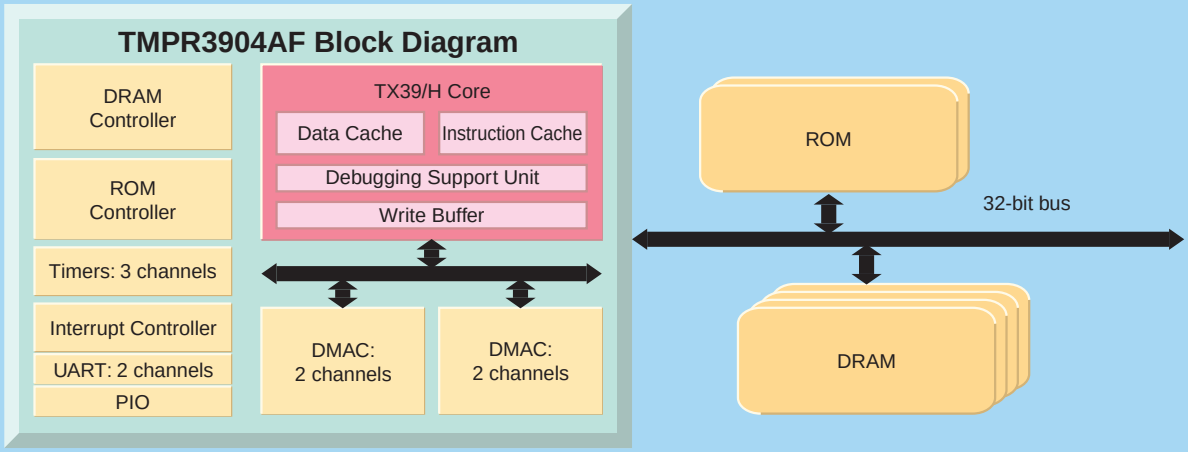
Features

■Built-in peripherals

- ROM controller
  Supports 16-bit width settings and Page Mode reading.
- RAM controller
  Supports 16-bit width settings, High-Speed Page Mode and Hyper Page Mode (EDO).
- Built-in DMA controller: 4 channels
  Memory-to-memory transfer, memory-to-I/O transfer
- Interrupt controller
  External interrupts: 8; Internal interrupts: 9
- Built-in timers: 3 channels
- Built-in UART: 2 channels
- PIO: 8 bits x 3 ports

■Additional features

- Instruction cache: 4 KB built in
- Data cache: 1 KB built in
- Maximum operating frequency: 66 MHz
- Supply voltage: 3.3 V
- 5-V tolerant buffer input
- Package: 208-pin QFP



*: Under development

TMPR3907F-66

New Product

Based on the TX39/H processor core, the TMPR3907F is a 32-bit single-chip RISC microcontroller with general-purpose peripherals. In addition to such peripherals as a memory controller, UART and timers, the TMPR3907F incorporates a PCI controller to facilitate connection of a wide range of peripheral circuits. The ROM controller supports interleaved connection of ROMs for high-performance systems.

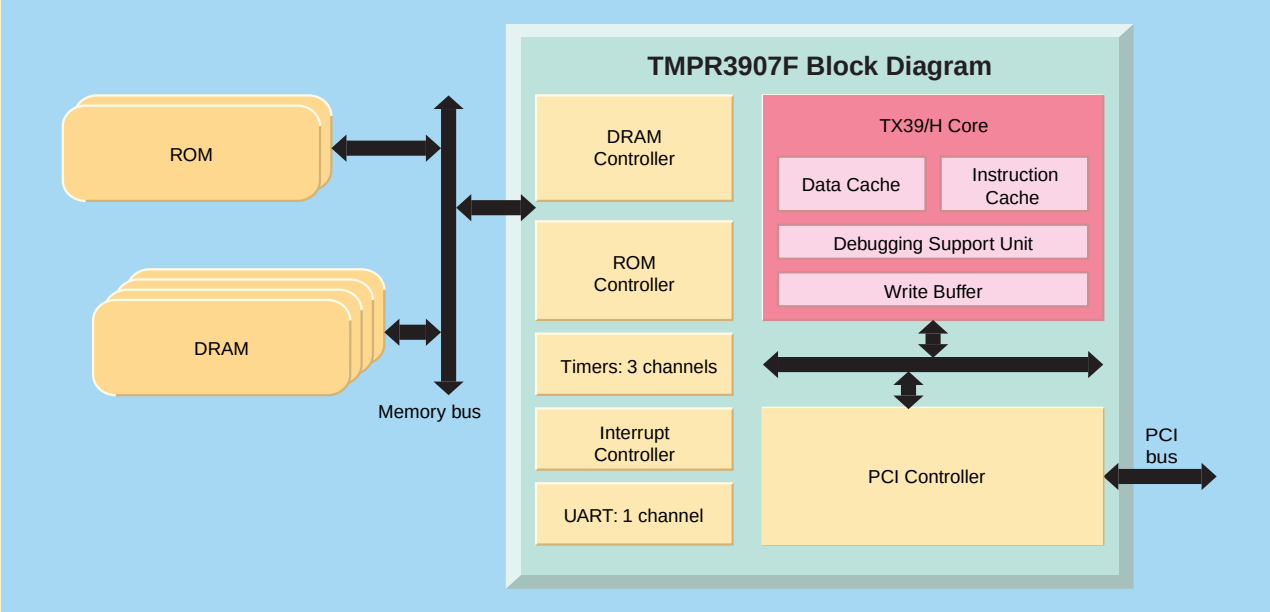
Features

■ Built-in peripherals

- ROM controller
  Supports 16-bit width settings and interleaved connection.
- DRAM controller
  Supports 16-bit width settings, High-Speed Page Mode and Hyper Page Mode (EDO).
- PCI controller: based on PCI 2.1
  Supports three slots.
  33-MHz operation, 3.3-V bus
- Interrupt controller
  External interrupts: 3; Internal interrupts: 8
- Built-in timers: 3 channels
- Built-in UART: 1 channel

■ Additional features

- Instruction cache: 4 KB built in
- Data cache: 1 KB built in
- Maximum operating frequency: 66 MHz
- Supply voltage: 3.3 V
- Package: 208-pin QFP



TMPR3912AU
TMPR3912AU-92*
TMPR3912XB-92*

New Product

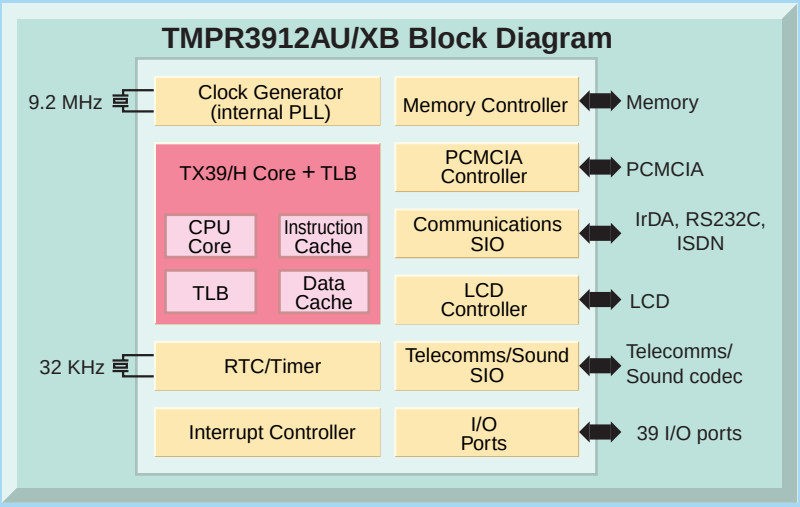
Based on the TX39/H processor core, the TMPR3912AU/XB incorporates into a single chip all the peripheral functions required by a portable information controller (PIC). The TMPR3912AU/XB built-in peripheral functions and its advanced power management capabilities make it an ideal choice as an ASSP for PICs.

The TMPR3912AU/XB is designed to improve the performance of portable information terminal systems while reducing their size and cost.

Features

- Instruction cache: 4 KB built in
- Data cache: 1 KB built in
- Memory management unit (TLB): 32 entries, 4 KB/page
- Memory controller: Supports DRAM (EDO), SDRAM, SRAM, ROM and flash memory.
- Communications interfaces: RS232C, IrDA (rev 1.0) and ISDN
- PCMCIA interface
- LCD interface: Supports monochrome and color, up to 1024 × 1024 pixels.
- Timers: 2 channels (RTC and/or watchdog timer)
- I/O ports: 39 bits
- Low power dissipation modes:
  Sleep Mode (only RTC operates.)
  Doze Mode (low-frequency operation)
- Maximum operating frequency:
  75 MHz (TMPR3912AU)
  92 MHz (TMPR3912AU-92/XB-92)
- Supply voltage: 3.3 V
- Package: 208-pin LQFP TMPR3912AU
  (1.4 mm thick)
  217-pin FBGA TMPR3912XB

TMPR3912AU/XB Block Diagram



*: Under development

TMPR3922AU
TMPR3922XB*

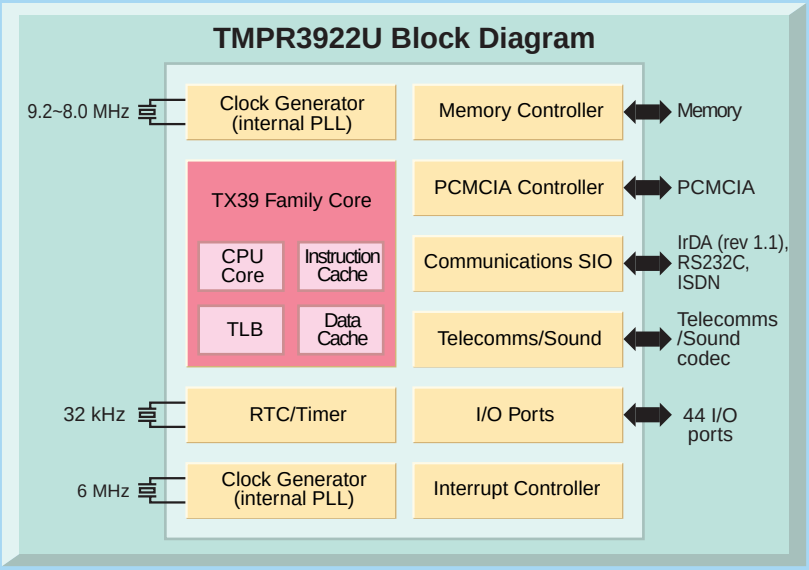
New Product

Based on the TX39 Family processor core, the TMPR3922AU/XB incorporates all the peripheral functions required by a portable information controller (PIC) on a single chip. The TMPR3922AU/XB built-in peripheral functions and its advanced power management capabilities make it an ideal choice as an ASSP for PICs.
The TMPR3922AU/XB is designed to improve the performance of portable information terminal systems while reducing their size and cost.

Features

- Instruction cache: 16 KB built-in (two-way set-associative)
- Data cache: 8 KB built-in (two-way set-associative)
- Memory management unit (TLB): 64 entries, 4 KB / 16 KB / 64 KB / 256 KB / 1 MB / 4 MB per page
- Memory controller: Supports DRAM (EDO), SDRAM, SRAM, ROM and flash memory.
- Communications interfaces: RS232C, IrDA (rev 1.1) and ISDN
- PCMCIA interface
- Timers: 2 channels (RTC and/or watchdog timer)
- I/O ports: 48 bits
- Low power dissipation modes:
  Sleep Mode (only RTC operates)
  Doze Mode (low-frequency operation)
- Maximum operating frequency:
  148* MHz / 129 MHz
- Supply voltage: 3.3 V for I/O, 2.7 V for internal use
- Package: 208-pin LQFP TMPR3922AU (1.4 mm thick)
  217-pin FBGA TMPR3922XB

TMPR3922U Block Diagram



*: Under development

TX39 Family Development Tools

Language processing tools for efficient application program development

■TX39 C/C++ compiler (supplied by Green Hills Software, Inc.)

- C compiler based on ANSI standard C, K&R C support
- C++ compiler: Support for Vers. 2.0, 2.1 and 3.0
- Powerful optimization functions
  e.g. register relocation, pipeline scheduling, loop optimization
- Compiler functions make use of the features of the TX39 processor architecture.
- Supports EWS (Sun) and PC (IBM PC) host systems.

■TX39 GNU C/C++ compiler (supplied by Cygnus Solutions, Inc.)

- C compiler based on ANSI standard C.
- C++ compiler complies with the latest ANSI C++ standards.
- Reliable technical support
- This compiler is optimized for the TX39 architecture.
- Source code and binary code supplied free of charge
- Supports Sun (Solaris) and PC (Windows 95/Windows NT) host systems.

Real-time debugging environment for high-speed systems

■TX39 simulator/Multi debugger (supplied by Green Hills Software, Inc.)

- C/C++/Assembly language source-level debugger
- Supports a wide range of debugging modes.
  Supports a cross-debugging environment on the host system when connected to the simulator.
  Supports real-time and cross-debugging environments when connected to the processor probe.
- Supports advanced user interfaces in Windows environments.
- Support for real-time OSs
  μITRON specification OS
  VxWorks (*1)/pSOS (*2)
  *1 VxWorks is a trademark of Wind River Systems, Inc.
  *2 pSOS is a trademark of Integrated Systems, Inc.

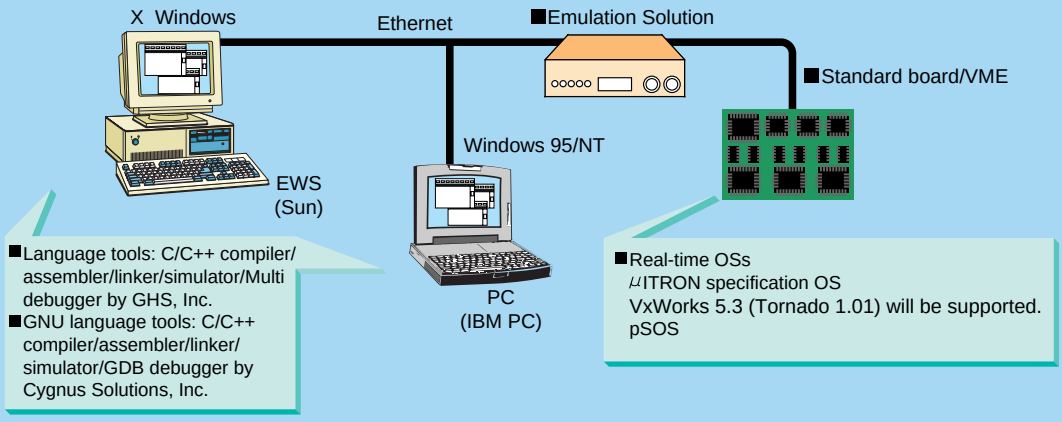
■GNU TX39 simulator/GDB debugger (supplied by Cygnus Solutions, Inc.)

- C/C++/Assembly language source-level debugger
- Supports easy-to-use GUIs.
- Connects to peripherals such as a GNU simulator or a debugging monitor.
- Source code and binary code supplied free of charge

■Emulation Solution (supplied by Hewlett-Packard Japan, Ltd.)

- Execution control
  Control includes program Run/Stop and display of memory/register contents.
- Program Counter trace
  A real-time trace of the Program Counter value and the instruction currently being executed are displayed.

Emulation Solution/ROM Emulator Connection Diagram



*: Under development

TX39 Family Development Tools

Real-time OSs

- TX39-dedicated real-time OS based on μITRON specification 3.0
  Provides the same system calls that are used in Toshiba's original TLCS-900/9000 Series microprocessors.
- VxWorks 5.3 (Tornado 1.01) supplied by Wind River Systems, Inc., will be supported.
- pSOS (supplied by Integrated Systems, Inc.)

TX39 standard board (supplied by Densan, Inc.)

- VME bus interface board
  TX39 internal operating frequency: 50/70 MHz
  Bus operating frequency: 25 MHz
  ROM: 1 MB; RAM: 16 MB
  RS-232C serial interface
  SCSI-2 interface
  Ethernet interface

- TMPR3904F board
  TMP3904F internal operating frequency: 50 MHz
  Bus operating frequency: 25 MHz
  ROM: 1 MB; RAM: 16 MB
  RS-232C serial interface
  SCSI-2 interface
  Ethernet interface

Documents

TX39 Family Architecture	**TMPR3922 Databook**
TX39 Family Hardware	**TMPR3901 Technical**
TX39/H2 Processor Core	**TMPR3904 Technical**
TMPR3903AF Databook	**TMPR3907 Technical**
TMPR3904 Databook	**TMPR3912 Technical**
TMPR3907 Databook	**TMPR3922 Technical**
TMPR3905/12 User's Manual	

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