Features

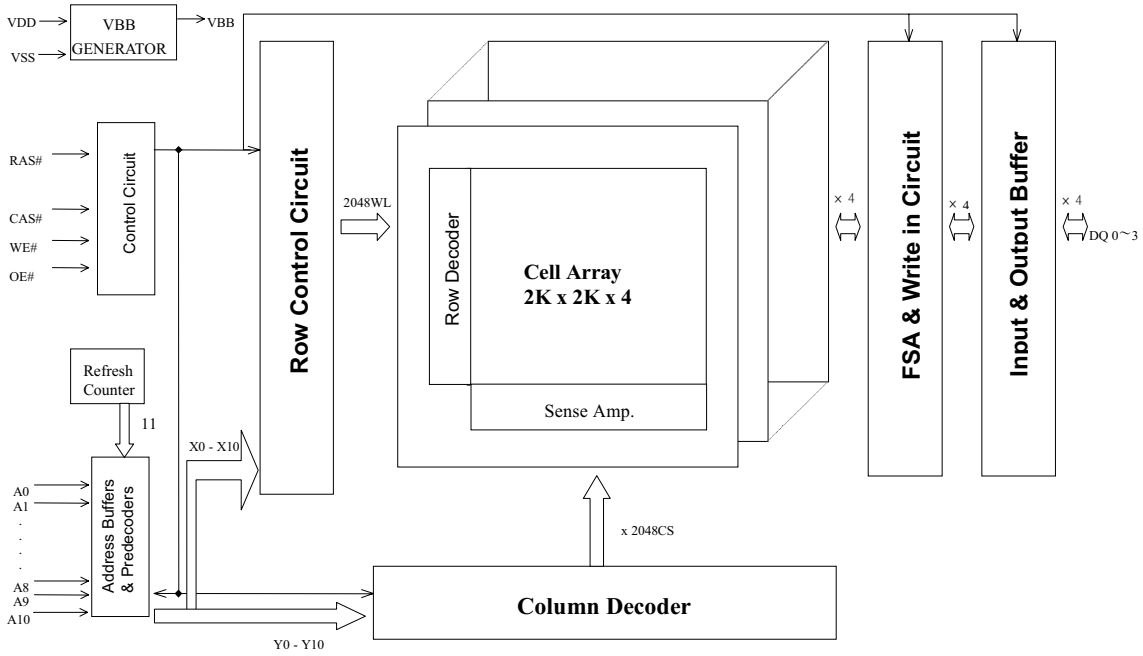
- Part identification—
  UT51C416(5V 1K Ref)
  UT51L416(3.3V 1K Ref)
- Extended Data Out operation
- RAS# access time: 60, 70, 80
- CAS# - before – RAS# refresh capability
- RAS – only and Hidden refresh capability
- Early write or output enable controlled write
- Available in 24/26 pin 300mil SOJ packages
- Single +5V±10% power supply
  --UT51C416
- Single +3.3V ± 10% power supply
  --UT51L416
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- 2K refresh cycles /32ms

Speed	-60	-70	-80
t_{RC}	105ns	125ns	145ns
t_{RAC}	60ns	70ns	80ns
t_{CAA}	30ns	35ns	35ns
t_{PC}	25ns	30ns	35ns
t_{CAC}	17ns	20ns	20ns
t_{CAS}	12ns	15ns	20ns

General Description

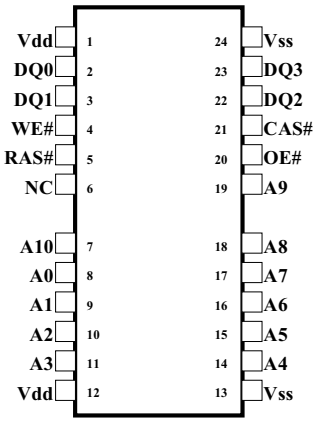
The UT51C416/UT51L416 is high speed 5 Volt/3.3Volt EDO DRAMs organized as 4M bit X 4 I/O and fabricated with the CMOS process. The UT51C416/UT51L416 offers a combination of unique features including: EDO Page Mode operation for higher bandwidth with Page Mode cycle time as short as 25ns. All inputs are TTL /LVTTLcompatible. Input and output capacitance is significantly lowered to increase performance and minimize loading. These features make the UT51C416/UT51L416 suited for wide variety of high performance computer systems and peripheral applications.

Block Diagram



Pin Assignment

UT51C416/UT51L416
24/26-pin SOJ package



PIN DESCRIPTION

A0-A10	Address Inputs
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write enable
OE#	Output enable
DQ0-DQ3	Data Input, Data Output
Vdd	Power Supply
Vss	0V Supply
NC	No Connect

Electrical Characteristic

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
Voltage on any pin relative to Vss	V_T	-1.0 to +7V	V	
Supply voltage relative to V_{SS}	V_{DD}	-1.0 to +7V	V	
Short circuit output current	Iout	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to + 70	ºC	
Storage temperature	Tstg	-55 to +125	ºC	

Notes: Permanent device damage may occur if absolute maximum ratings are exceed.

Recommended DC Operating Conditions (Ta = 0 to +70ºC)

Parameter	Symbol	3.3V			5V			Notes
		Min	Max	Unit	Min	Max	Unit	
Supply voltage	Vdd	3.0	3.6	V	4.5	5.5	V	1
	Vss	0	0	V	0	0	V	
Input high voltage	V_{IH}	2.1	V_{DD}+1V	V	2.4	V_{DD}+1V	V	1,2
Input low voltage	V_{IL}	-0.3	0.8	V	-0.3	0.8	V	1,3

Notes: 1. All Voltage referred to Vss

Capacitance(TA = 25ºC, 5V device：5V±10%, 3.3V device：3.3V±0.3V, f=1MHz)

	Symbol	Typ	Max	Unit
Input capacitance(A0-A10)	Cin1	3	4	pF
Input Capacitance (RAS#, UCAS# , LCAS# ,WE# , OE#)	Cin2	4	7	pF
Output capacitance(DQ0-DQ15)	Cdq	5	7	pF

DC Characteristics (Ta = 0 to 70ºC, 5V device：V_{DD}=5.0V±0.5V, Vss = 0 V)
DC Characteristics (Ta = 0 to 70ºC,3.3V device：V_{DD}=3.3V±0.3V, Vss = 0 V)

Symbol	Parameter	Speed (t_{RAC})	UT51C416		UT51L416		unit	Test condition
			Min	Max	Min	Max		
I_{DD1}	Operating current, Vdd supply	-60		90		80	mA	t_{RC} = t_{RC} (min.)
		-70		80		70		
		-80		70		70		
I_{DD2}	Standby current (TTL input)			3		2	mA	RAS# = UCAS# = LCAS# = V_{IH}
I_{DD3}	RAS-only refresh current	-60		90		80	mA	t_{RC} = t_{RC} (min.)
		-70		80		70		
		-80		70		70		
I_{DD4}	EDO page mode current	-60		180		160	mA	t_{PC} = t_{PC} (min.)
		-70		170		150		
		-80		160		150		
I_{DD5}	CBR refresh current	-60		90			mA	t_{RC} = t_{RC} (min.)
		-70		80				
		-80		70				
I_{DD6}	Standby current (CMOS input)			2		2	mA	RAS# ≧ VDD-0.2V CAS# ≧ VDD-0.2V All other inputs>= VSS
VDD	Power Supply		4.5	5.5	3.0	3.6	V	
I_{LI}	Input Leakage Current		-10	10	-10	10	uA	VSS≦ Vin ≦Vdd
I_{LO}	Output Leakage Current		-10	10	-10	10	uA	VSS≦ V_{OUT} ≦Vdd RAS# = CAS# = V_{IH}
V_{IL}	Input Low Voltage		-0.3	0.8	-0.3	0.8	V	
V_{IH}	Input High Voltage		2.4	Vdd+1	2.1	Vdd+1	V	
V_{OL}	Output Low Voltage			0.4		0.4	V	Iol =2mA
V_{OH}	Output High Voltage		2.4		2.2		V	Ioh = 2mA

Notes: I_{DD1}, I_{DD3}, I_{DD4}, I_{DD5} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{DD} is specified as an average current. In I_{DD1}, I_{DD3}, and I_{DD5} address can be changed maximum once while RAS#=Vil. In I_{DD4}, address can be changed maximum once within one EDO page cycle time, t_{PC}.

AC Characteristics (Ta = 0 to 70°C, Vdd = 5V ± 10%, Vss = 0 V)
Test condition: V_{DD} = 5.0V±10%, Vih/Vil=3V/0V, Voh/Vol=2.0/0.8)
Test condition: V_{DD} = 3.3V±0.3V, Vih/Vil=2.4V/0.4V, Voh/Vol=2.0/0.8)

	Symbol	Parameter	60		70		80		unit	
			Min.	Max	Min.	Max	Min.	Max		
1	t_{RAS}	RAS# Pulse Width	60	10K	70	10K	80	10K	ns	
2	t_{RC}	Read or Write Cycle Time	105		125		145		ns	
3	t_{RP}	RAS# Precharge Time	40		50		60		ns	
4	t_{CSH}	CAS# Hold Time	55		60		70		ns	
5	t_{CAS}	CAS# Pulse Width	12		15		20		ns	
6	t_{RCD}	RAS# to CAS# Delay	20	43	20	50	20	60	ns	
7	t_{RCS}	Read Command Setup Time	0		0		0		ns	*1
8	t_{ASR}	Row Address Setup Time	0		0		0		Ns	
9	t_{RAH}	Row Address hold Time	10		10		10		ns	
10	t_{ASC}	Column Address Setup Time	0		0		0		ns	
11	t_{CAH}	Column Address Hold Time	10		10		10		ns	
12	t_{RSH}	RAS# to CAS# Hold Time	17		20		20		ns	
13	t_{CRP}	CAS# to RAS# Precharge Time	5		5		5		ns	
14	t_{RCH}	Read Command Hold Time Reference CAS#	0		0		0		ns	*2
15	t_{RRH}	Read Command Hold Time Reference RAS#	0		0		0		ns	*2
16	t_{ROH}	RAS# Hold Time Referenced to OE#	10		15		15		ns	
17	t_{OAC}	Access Time from OE#		17		20		20	ns	*9
18	t_{CAC}	Access Time from CAS#		17		20		20	ns	*3,4,11
19	t_{RAC}	Access Time from RAS#		60		70		80	ns	*3,5,6
20	t_{CAA}	Access Time From Column Address		30		35		35	ns	*3,4,7
21	t_{LZ}	OE# or CAS# to Low-Z Output	0		0		0		ns	*13
22	t_{HZ}	OE# or CAS# to High-Z Output	0	10	0	15	0	15	ns	*13
23	t_{AR}	Column Address Hold Time from RAS#	45		50		60		ns	
24	t_{RAD}	RAS# to Column Address Delay Time	15	30	15	35	15	40	ns	*8
25	t_{T}	Transition Time	2	50	2	50	2	50	ns	*12
26	t_{CWL}	Write Command to CAS# Lead Time	10		15		20		ns	
27	t_{WCS}	Write Command Setup Time	0		0		0		ns	*9,10
28	t_{WCH}	Write Command Hold time	10		15		15		ns	

AC Characteristics (Ta = 0 to 70°C)

	Symbol	Parameter	60		70		80		unit	
			Min.	Max	Min.	Max	Min.	Max		
29	t_{WP}	Write Pulse Width	10		15		15		ns	
30	t_{WCR}	Write Command Hold Time from RAS#	45		50		60		ns	
31	t_{RWL}	Write Command to RAS# Lead Time	15		20		20		ns	
32	t_{DS}	Data in Setup Time	0		0		0		ns	*11
33	t_{DH}	Data in Hold Time	10		15		15		ns	*11
34	t_{WOH}	Write to OE# Hold time	10		15		15		ns	*11
35	t_{OED}	OE# to Data Delay Time	15		20		20		ns	*11
36	t_{RWC}	Read-Modify-Write Cycle Time	140		170		190		Ns	
37	t_{RRW}	Read-Modify-Write Cycle Time RAS# Pulse Width	95		115		135		ns	
38	t_{CWD}	CAS# to WE# Delay in Read-Modify-Write Cycle	35		40		40		ns	*9
39	t_{RWD}	RAS# to WE# Delay in Read-Modify-Write Cycle	80		95		105		ns	*9
40	t_{CRW}	CAS# pulse Width in RMW	65		75		85		ns	
41	t_{AWD}	Column Address to WE# Delay Time	60		65		70		ns	*9
42	t_{PC}	EDO Page Mode Read or Write Cycle Time	25		30		35		ns	
43	t_{CP}	CAS# Precharge Time	10		10		10		ns	
44	t_{CAR}	Column Address to RAS# Setup Time	30		35		35		ns	
45	t_{CPA}	Access Time from Column Precharge		35		40		40	ns	*4
46	t_{DHR}	Data in Hold Time Referenced to RAS#	45		50		60		ns	
47	t_{CSR}	CAS# Setup Time in CBR Refresh	5		10		10		ns	
48	t_{RPC}	RAS# to CAS# Precharge Time	5		5		5		ns	
49	t_{CHR}	CAS# Hold Time in CBR Refresh	10		10		10		ns	
50	t_{PCM}	EDO Page Mode Cycle Time in RMW	55		70		80		ns	
51	t_{COH}	Output Hold After CAS# Low	3		3		3		ns	
52	t_{OES}	OE# Low to CAS# High Setup Time	5		5		5		ns	
53	t_{OEH}	OE# Hold Time from WE# in RMW Cycle	12		12		12		ns	
54	t_{OEP}	OE# Pulse Width	10		10		10		ns	
55	t_{REF}	Refresh Interval (2K Cycles)		32		32		32	ms	*14

Notes:

1. TRCD (Max.) is specified for reference only. Operation within t_{raced} (Max.) limits insures that t_{race} (Max.) and T_{CP} (Max.) can be met. If t_{raced} is greater than the specified t_{raced} (Max.), the access time is controlled by T_{CP} and $T_{eac.}$

2. Either $t_{r.}$ or t_{roche} must be satisfied for Read Cycle to occur.
3. Measured with a load equivalent to one TTL input and 50pF.
4. Access time is determined by the longest of t_{CAA} , t_{CAC} and t_{CAP} .
5. Assumes that $t_{RAD} \leqq t_{RAD}$ (Max.). If t_{RCD} is greater than t_{RCD} (Max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (Max.)
6. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If t_{RCD} is greater than t_{RCD} (Max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (Max.)
7. Assumes that $t_{RAD} \geqq t_{RAD}$ (Max.).
8. Operation within the t_{RAD} (Max.) limits ensures that t_{RA} can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.), the access time is controlled by t_{CAA} and $t_{CAC.}$
9. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters.
10. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
11. t_{DS} and t_{DH} are referenced to the latter occurrence of CAS# or WE#.
12. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 3Ns.
13. Assumes a tri-state test load (5pF and a 500Ohm Thevenin equivalent).
14. An initial pause of 200us is required after power-up followed by any 8 CBR or ROR cycles before device operation is achieved.

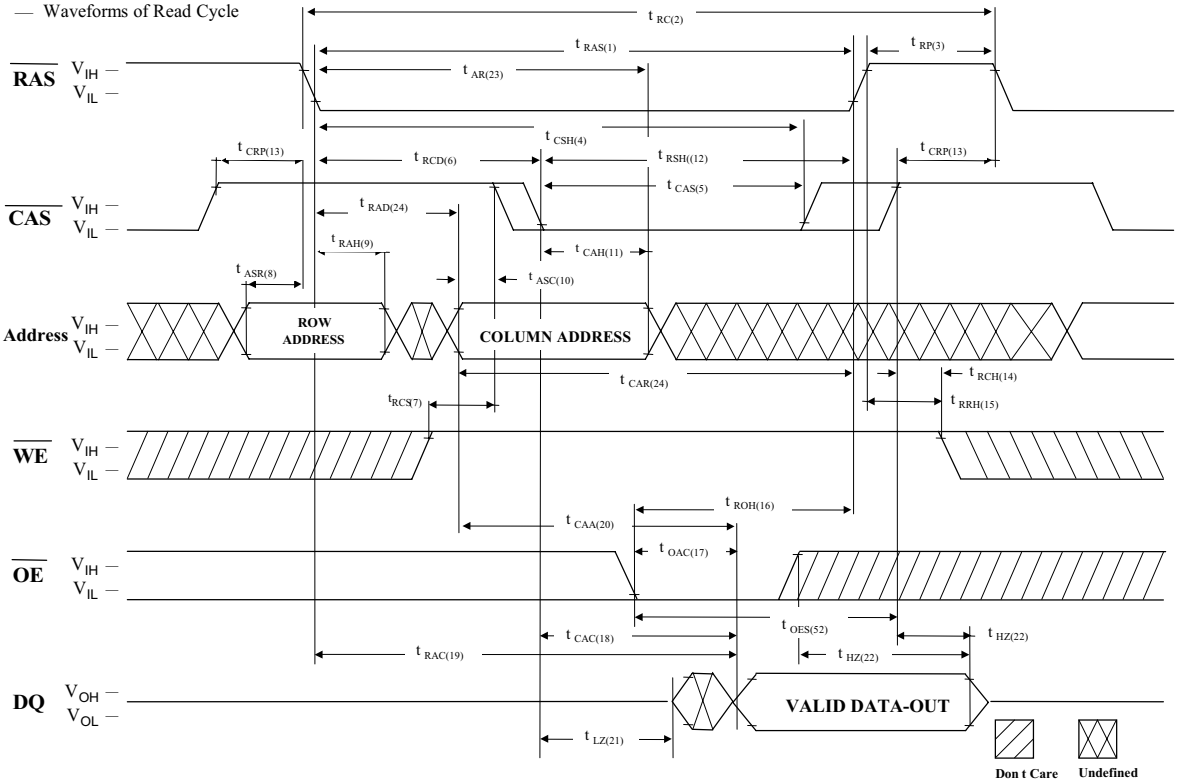
Truth Table

Function	RAS#	CAS#	WE#	OE#	ADDRESS	DQ0-3
Standby	H	H	X	X	X	High-Z
Read:Word	L	L	H	L	ROW/COL	DQ-OUT
Write: Word (Early-Write)	L	L	L	X	ROW/COL	DQ-IN
Read-Write	L	L	H→L	L→H	ROW/COL	DQ-OUT,DQ-IN
EDO Page-Mode Read	L	H→L	H	L	COL	DQ-OUT
EDO Page-Mode Write	L	H→L	L	X	COL	DQ-IN
EDO Page –Mode Read-Write	L	H→L	H→L	L→H	COL	DQ-OUT,DQ-IN
Hidden Refresh Read	L→H→L	L	H	L	ROW/COL	DQ-OUT
Ras#-Only Refresh	L	H	X	X	ROW	High-Z
CBR Refresh	H→L	L	X	X	X	High-Z

Timing Diagram

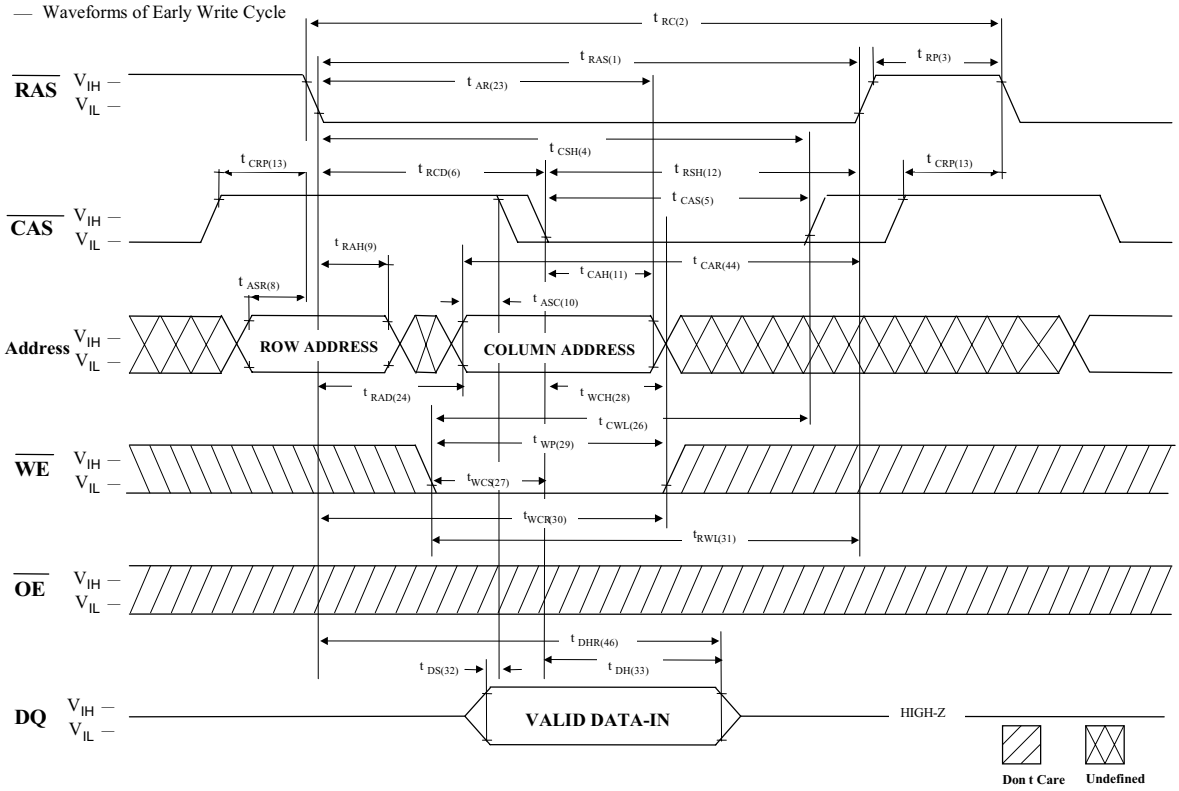
UTRON EDO Mode, X4 / X8 Device Timing Diagram

— Waveforms of Read Cycle



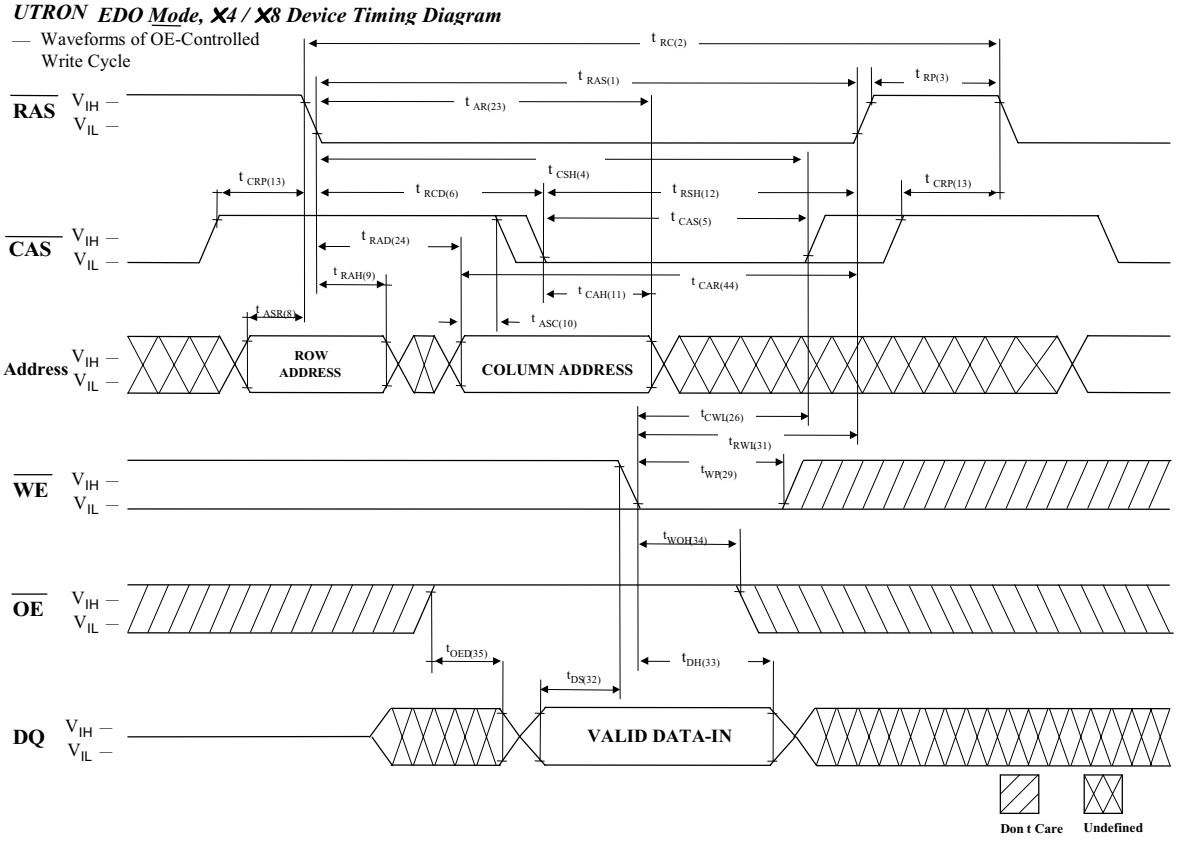
UTRON EDO Mode, X4 /X8 Device Timing Diagram

— Waveforms of Early Write Cycle



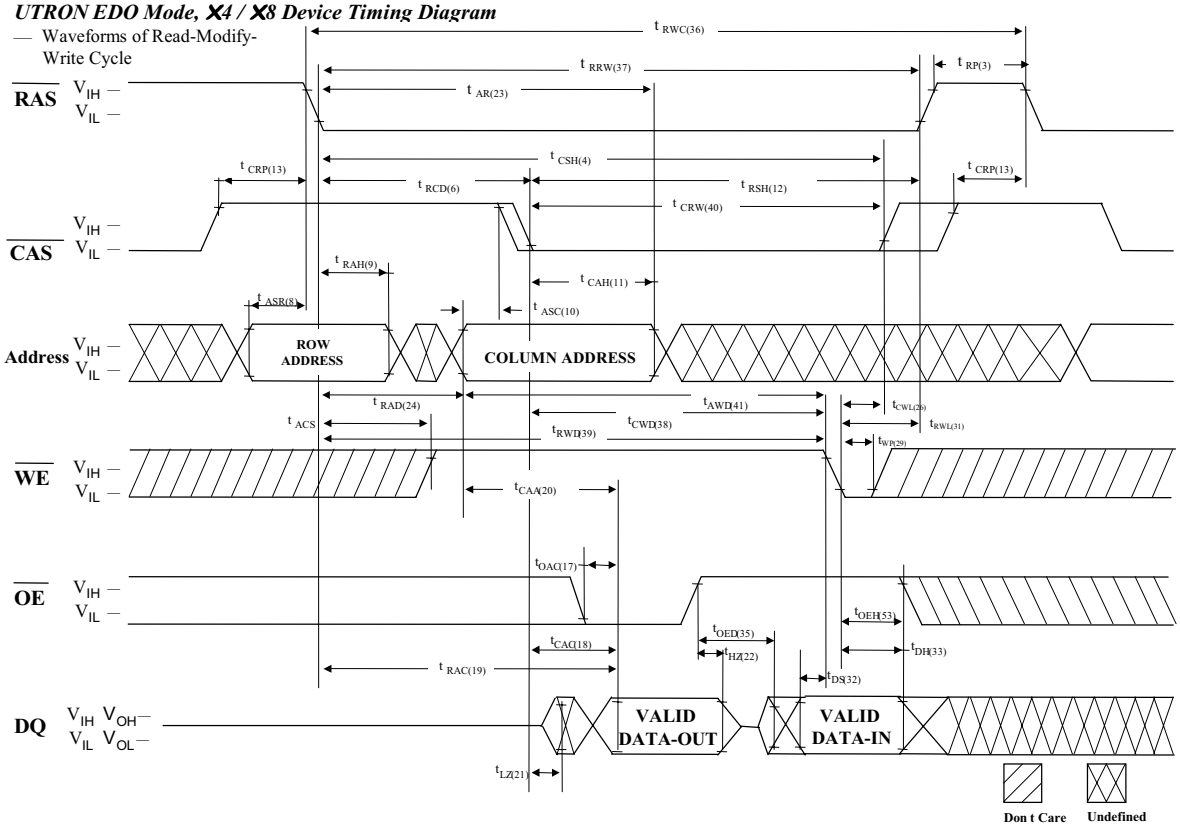
UTRON EDO Mode, X4 / X8 Device Timing Diagram

— Waveforms of OE-Controlled Write Cycle



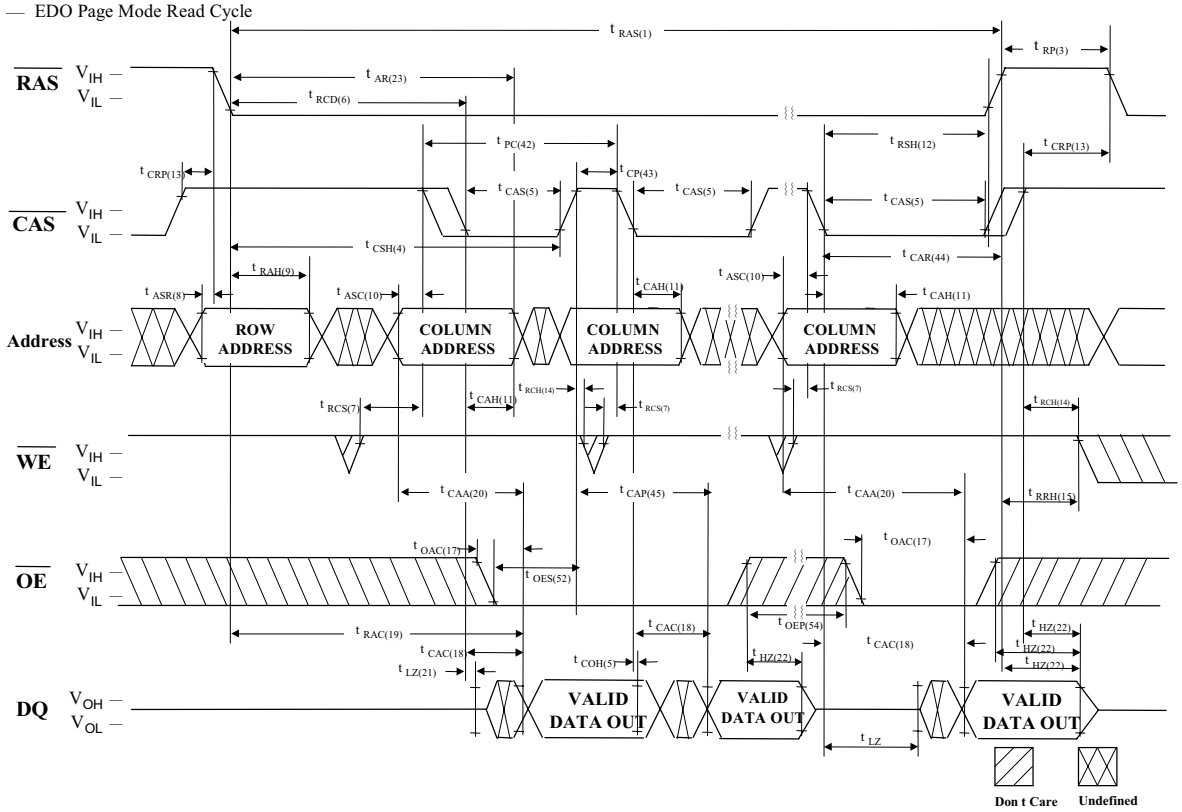
UTRON EDO Mode, X4 / X8 Device Timing Diagram

— Waveforms of Read-Modify-Write Cycle



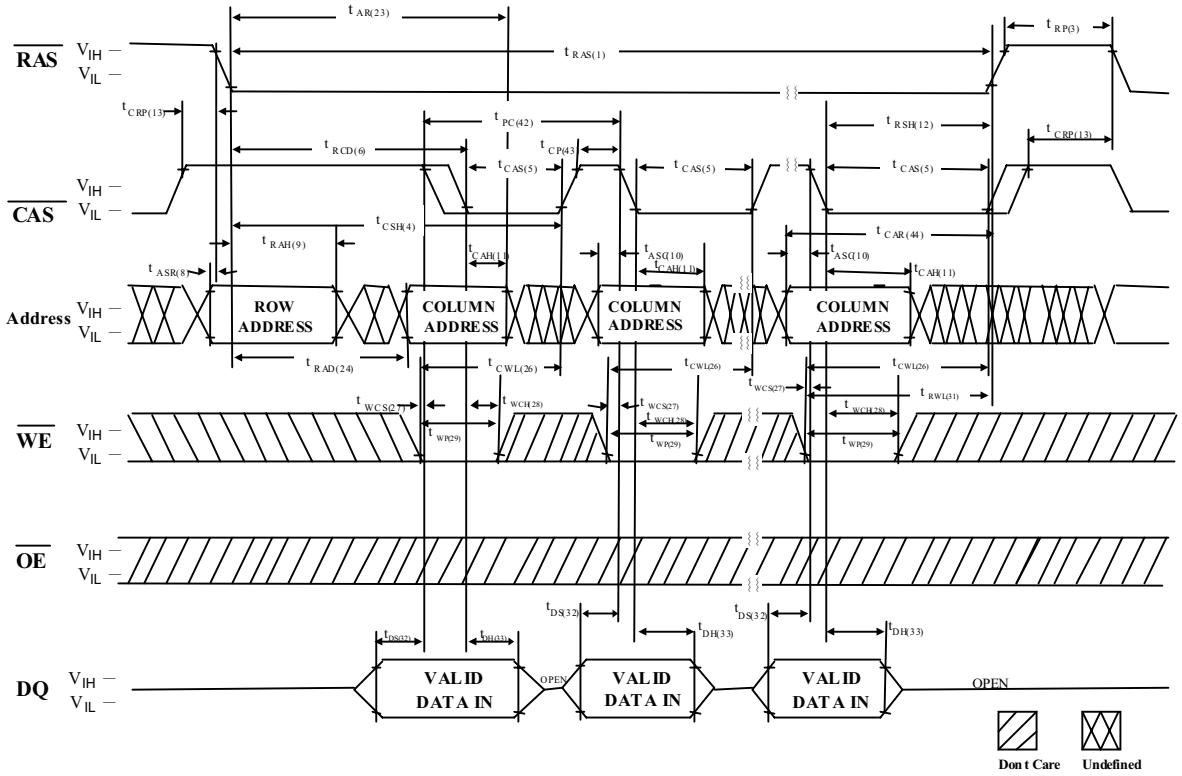
UTRON EDO Mode, X4 / X8 Device Timing Diagram

— EDO Page Mode Read Cycle



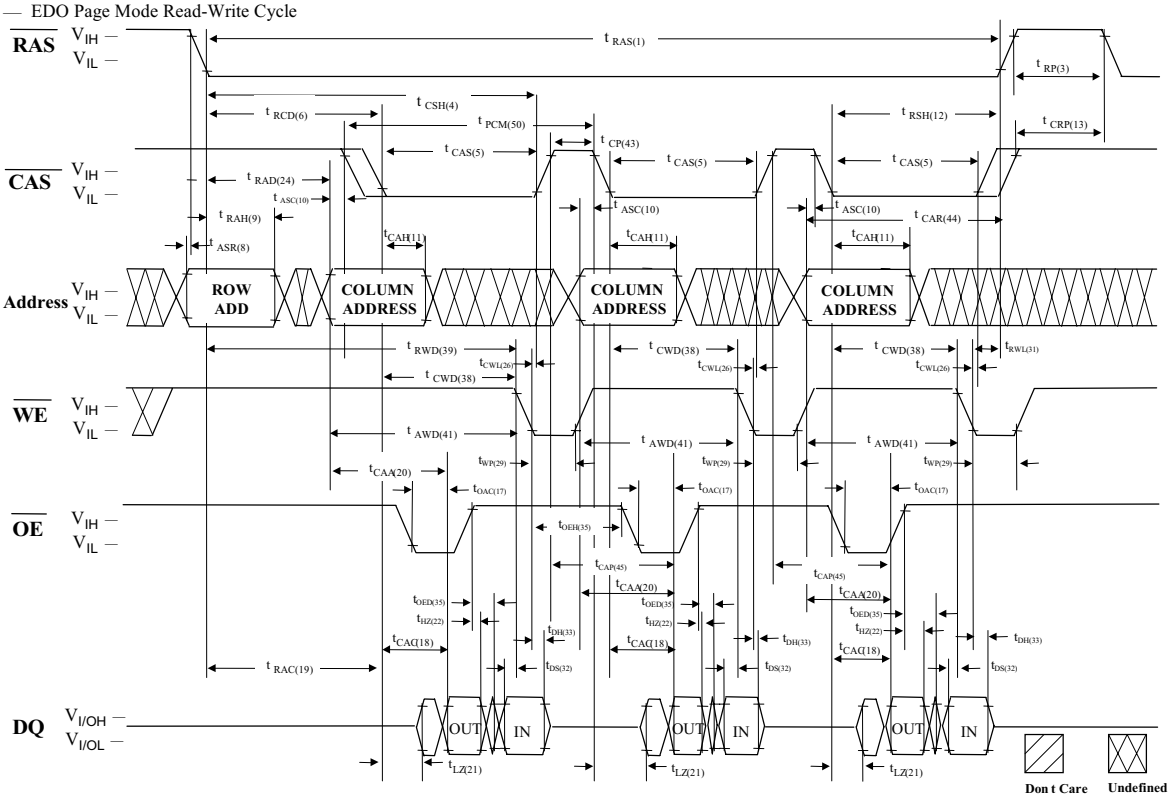
UTRON EDO Mode, ×4 / × 8 Device Timing Diagram

— EDO Page Mode Write Cycle



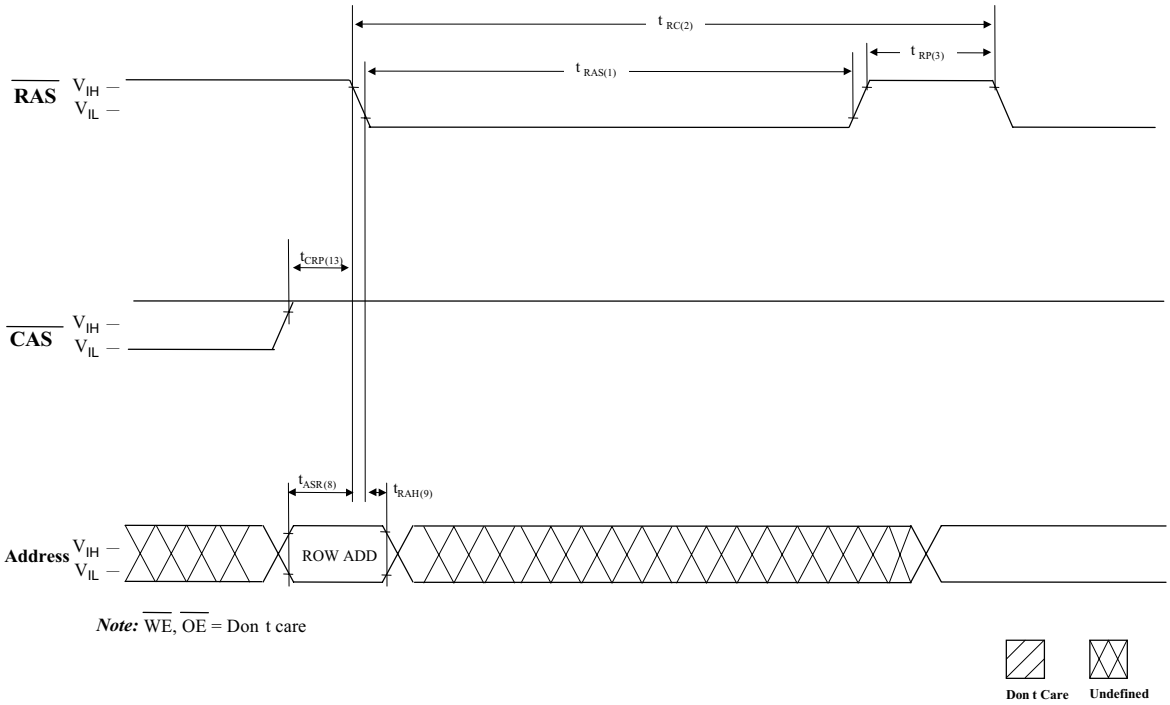
UTRON EDO Mode, X4 / X 8 Device Timing Diagram

— EDO Page Mode Read-Write Cycle



UTRON EDO Mode, ×4 / ×8 Device Timing Diagram

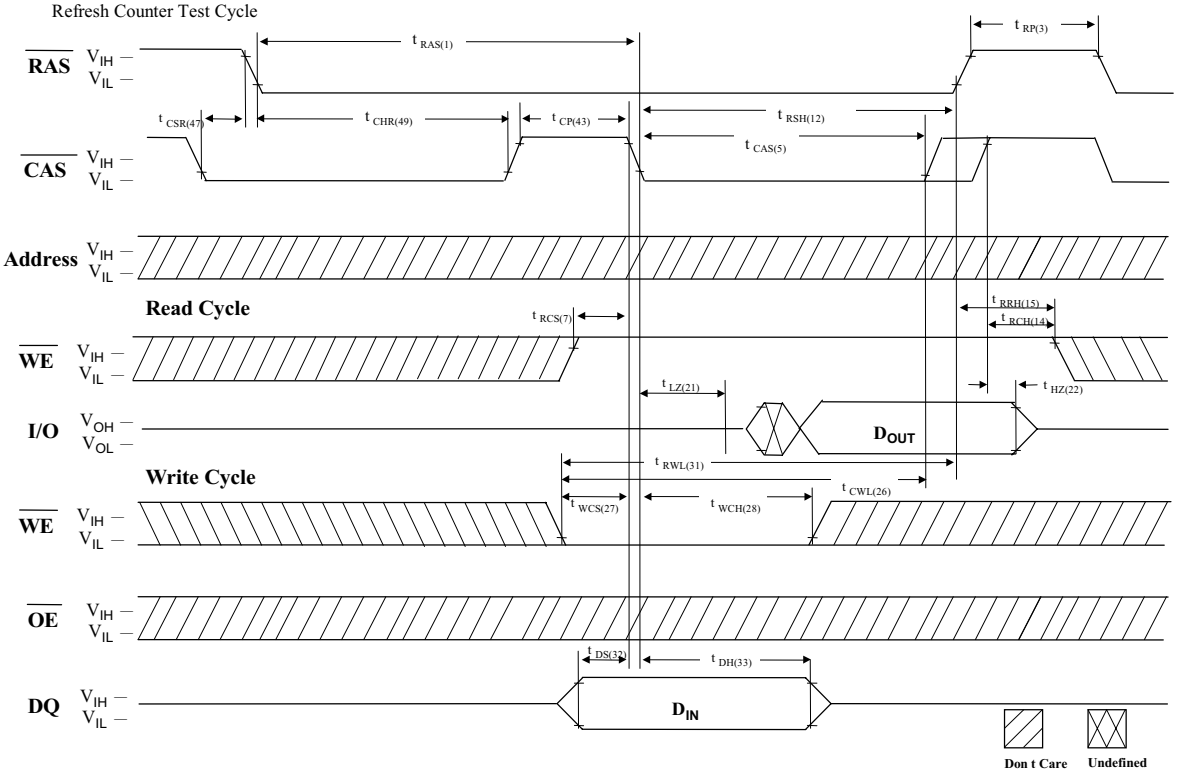
— Waveforms of $\overline{RAS}$-Only Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$ = Don t care

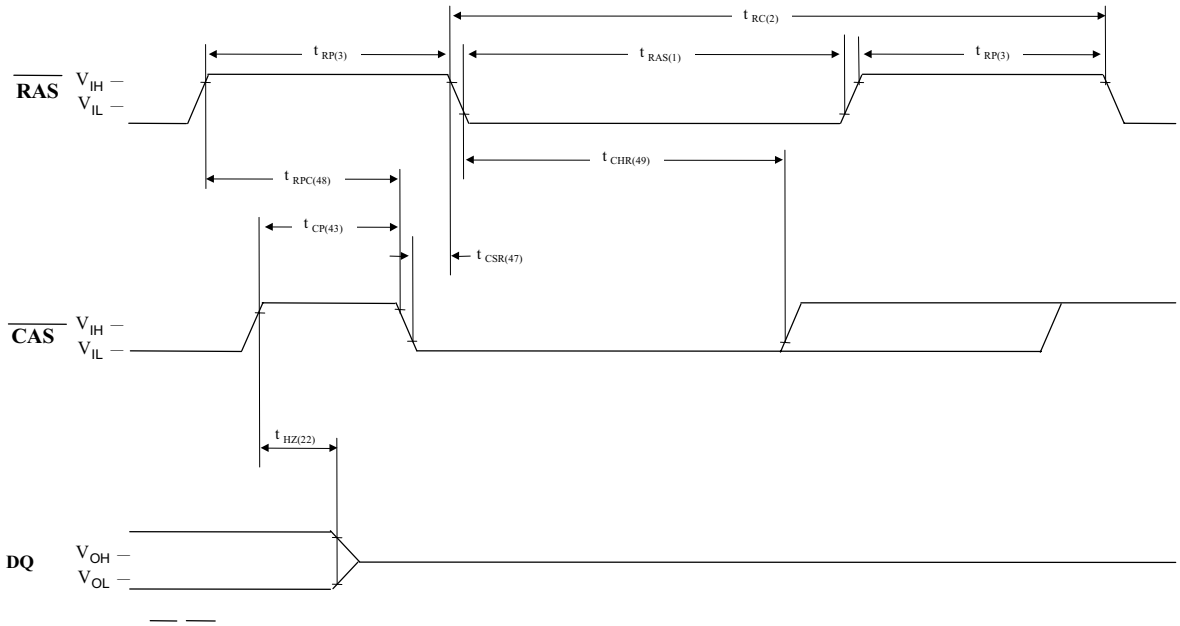
UTRON EDO Mode, X4 / X8 Device Timing Diagram

— Waveforms of CAS-before-RAS
Refresh Counter Test Cycle



UTRON EDO Mode, X4 / X8 Device Timing Diagram

— Waveforms of CAS-before-RAS
Refresh Cycle

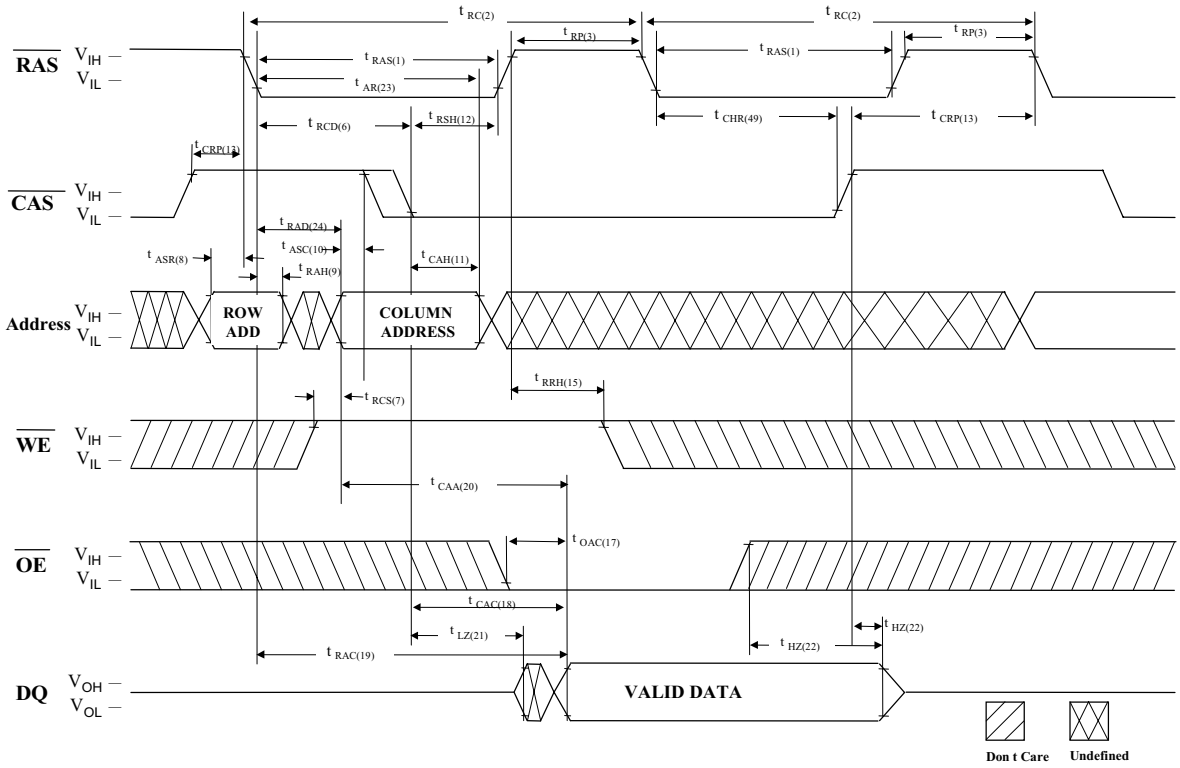


Note: WE, OE = A_0 - A_8 = Don t care

Don t Care Undefined

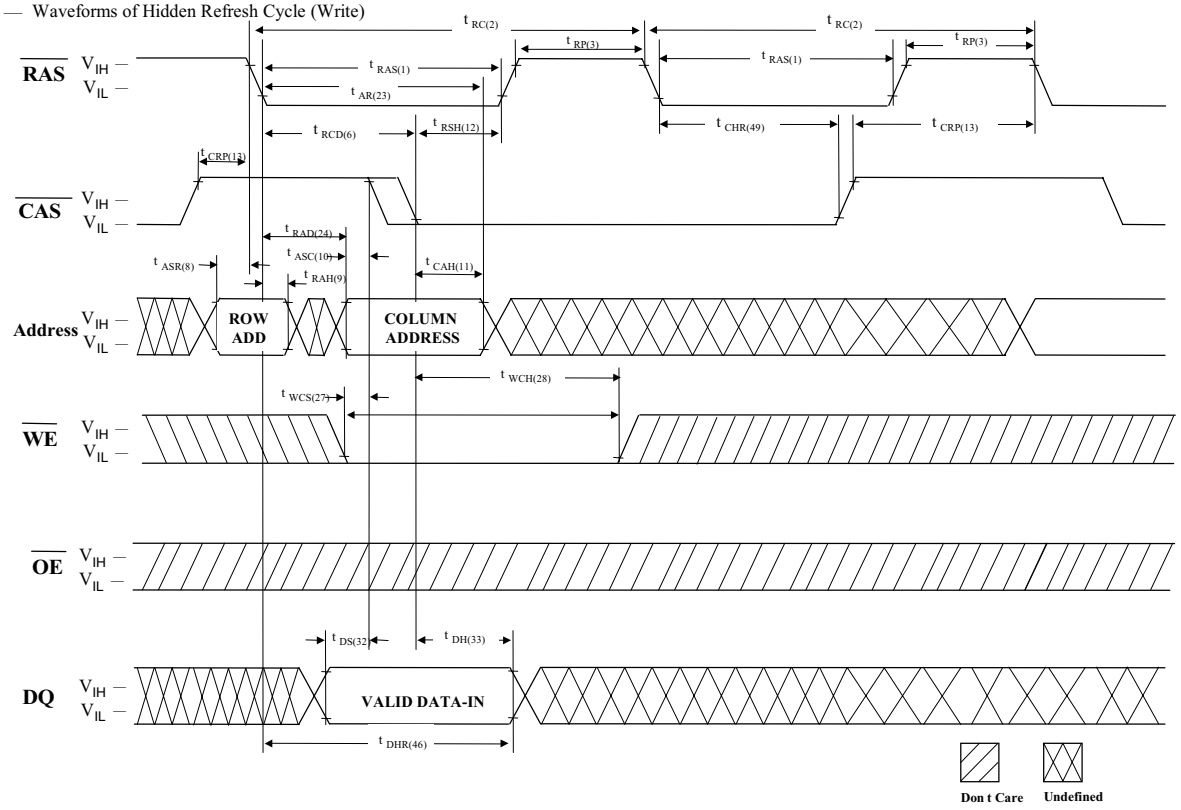
UTRON EDO Mode, X4 / X8 Device Timing Diagram

— Waveforms of Hidden Refresh Cycle (Read)



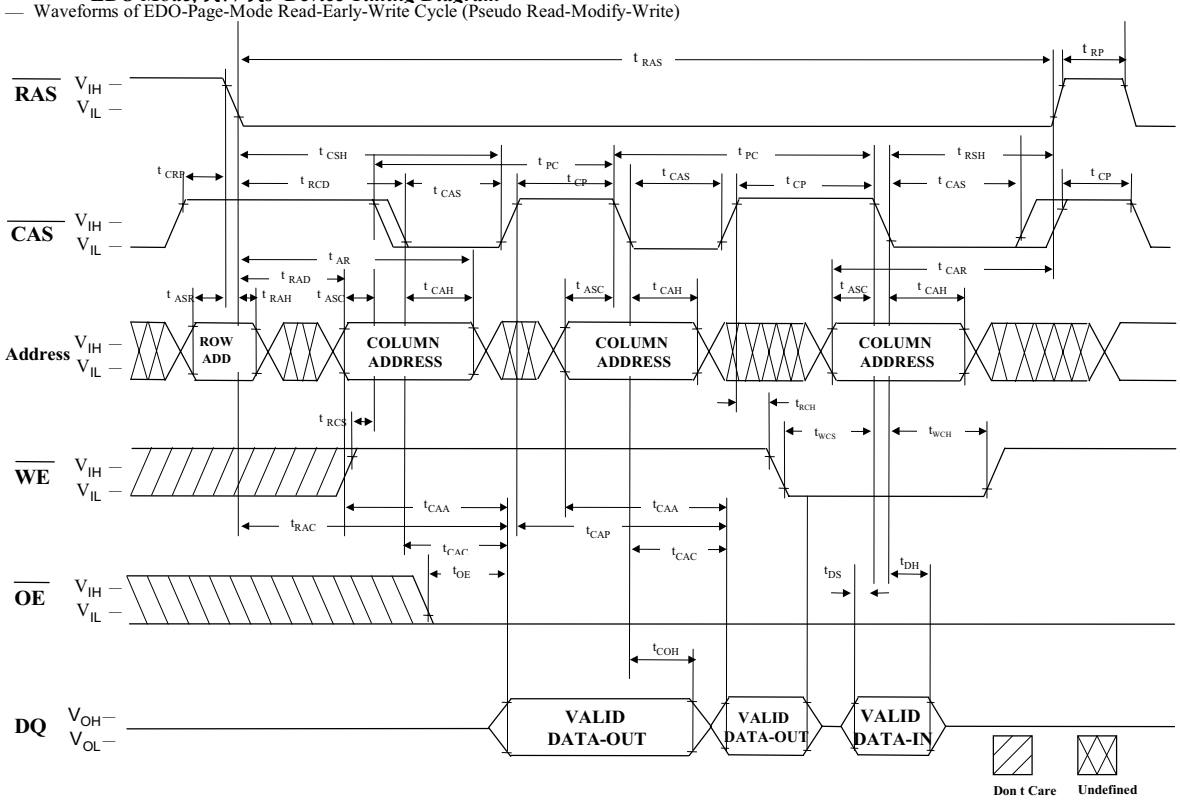
UTRON EDO Mode, X4 / X8 Device Timing Diagram

— Waveforms of Hidden Refresh Cycle (Write)



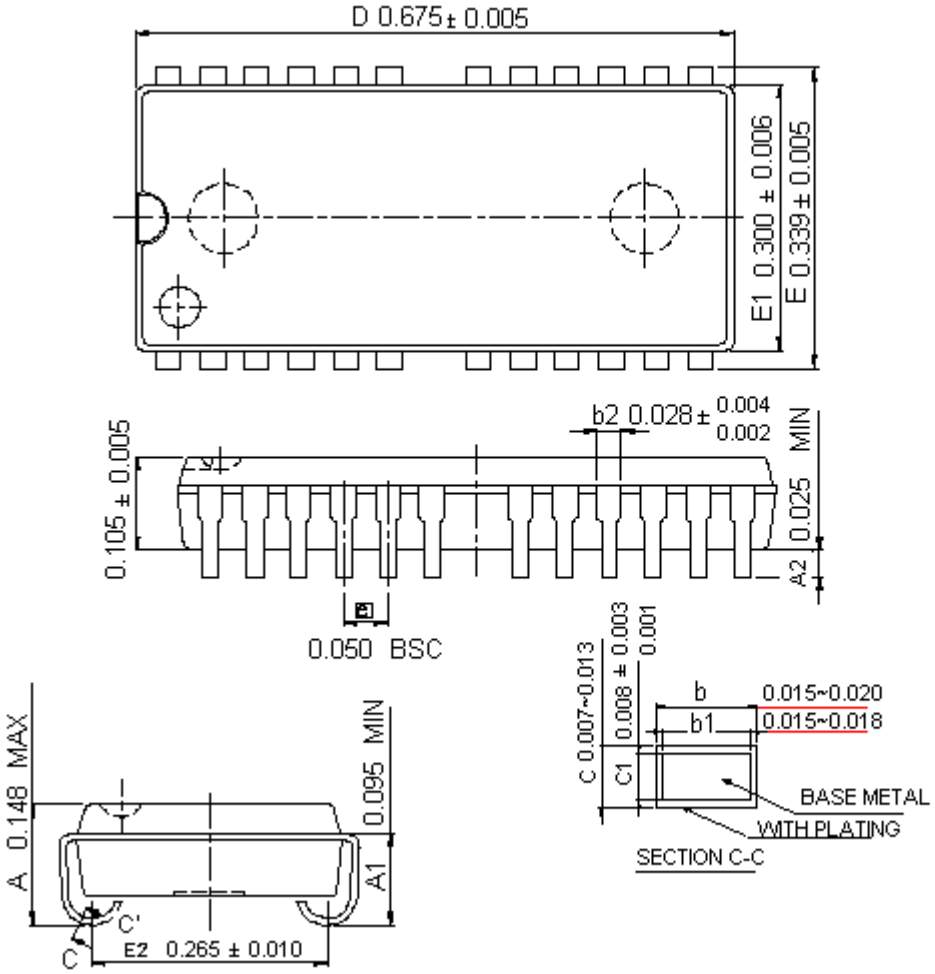
UTRON EDO Mode, X4 / X8 Device Timing Diagram

— Waveforms of EDO-Page-Mode Read-Early-Write Cycle (Pseudo Read-Modify-Write)



Package Outline Dimension

24 /26 pin 300mil SOJ Package Outline Dimension



NOTE:
1. DIMENSION D&E DOES NOT INCLUDE FLASH.
2. LEAD COPLANARITY 4 MIL MAX.
3. SOLDER PLATED THICK 300～800 uM.

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	PACKAGE
UT51C416JC-60	60	24/26 PIN SOJ
UT51C416JC-70	70	24/26 PIN SOJ
UT51C416JC-80	80	24/26 PIN SOJ
UT51L416JC-60	60	24/26 PIN SOJ
UT51L416JC-70	70	24/26 PIN SOJ
UT51L416JC-80	80	24/26 PIN SOJ

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