NIPPON PRECISION CIRCUITS INC.

# SM5866AS

## D/A Converter for DSD and PCM

## OVERVIEW

The SM5866AS is a D/A converter compatible with both the DSD SACD signal format and the PCM CD/DVD-Audio and similar formats. DSD employs a 1-bit data stream, from a high-order ΔΣ conversion at 64fs (fs = 44.1kHz), that contains high-level quantization noise in the high-frequency band above 20kHz. The SM5866AS, in DSD reproduction, has a DSD-dedicated FIR digital filter that attenuates the DSD quantization noise in the digital domain, and the resulting multi-level signal is D/A converted. In PCM reproduction, an oversampled PCM signal input, provided using a SM5847AF or similar digital filter, is converted to a multi-level signal by the 3rd-order noise shaper and then the multi-level signal is D/A converted.

## FEATURES

- Mono-channel multi-level D/A converter
- High performance analog characteristics
  - DSD mode (typical values)
    - THD + N: –109dB (0.00036%)
    - D.R: 115dB
  - PCM mode (typical values)
    - THD+N: –106dB (0.00050%)
    - D.R: 112dB
- 2 selectable DSD digital filters
- PCM input mode
  - 24-bit, MSB-first, right-justified
  - 8-times or 4-times oversampling of fs = 16k to 192kHz
- System clock (CKI)
  Maximum operating frequency: $f_{CKI}$ (max)
  - 37.0MHz (note 1)
  - 45.4MHz (note 2)
- DSD mode fs = $f_{CKI}$/512
  - typ. fs = 44.1kHz
  - max. fs = 52.7kHz (note 1)
  - max. fs = 88.7kHz (note 2)
- PCM mode system clock
  - 192/256/384/512/768fs
- Operating voltage: 4.5 to 5.5V
- Operating temperature: –40 to 85°C
- Package: 28-pin SOP
- Molybdenum-gate CMOS process

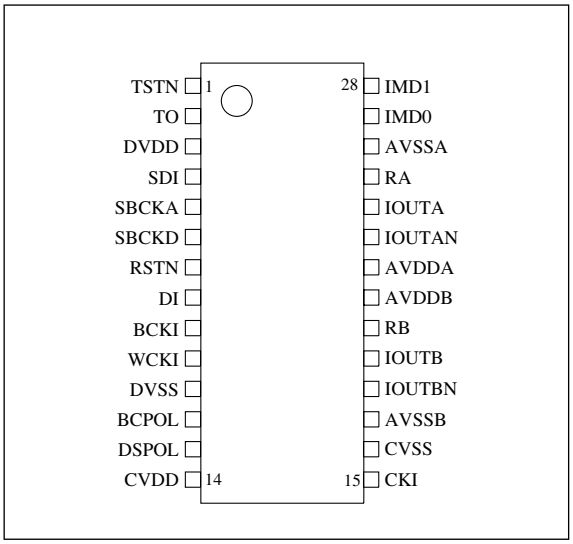
(note 1) Under the operating conditions 1: 4.5 to 5.5V, –40 to 85°C
(note 2) Under the operating conditions 2: 4.75 to 5.25V, –40 to 70°C

## ORDERING INFORMATION

| Device | Package |
|---|---|
| SM5866AS | 28-pin SOP |

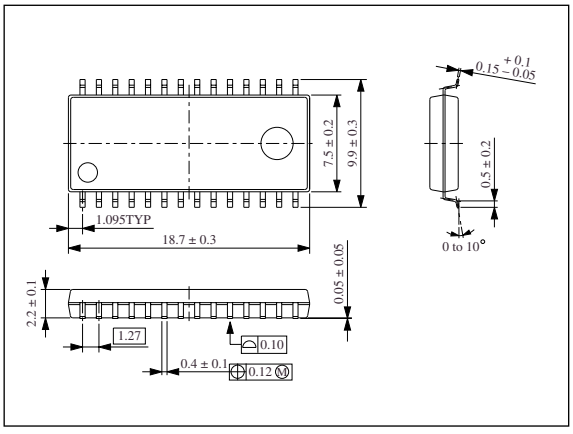
## PINOUT

(Top view)

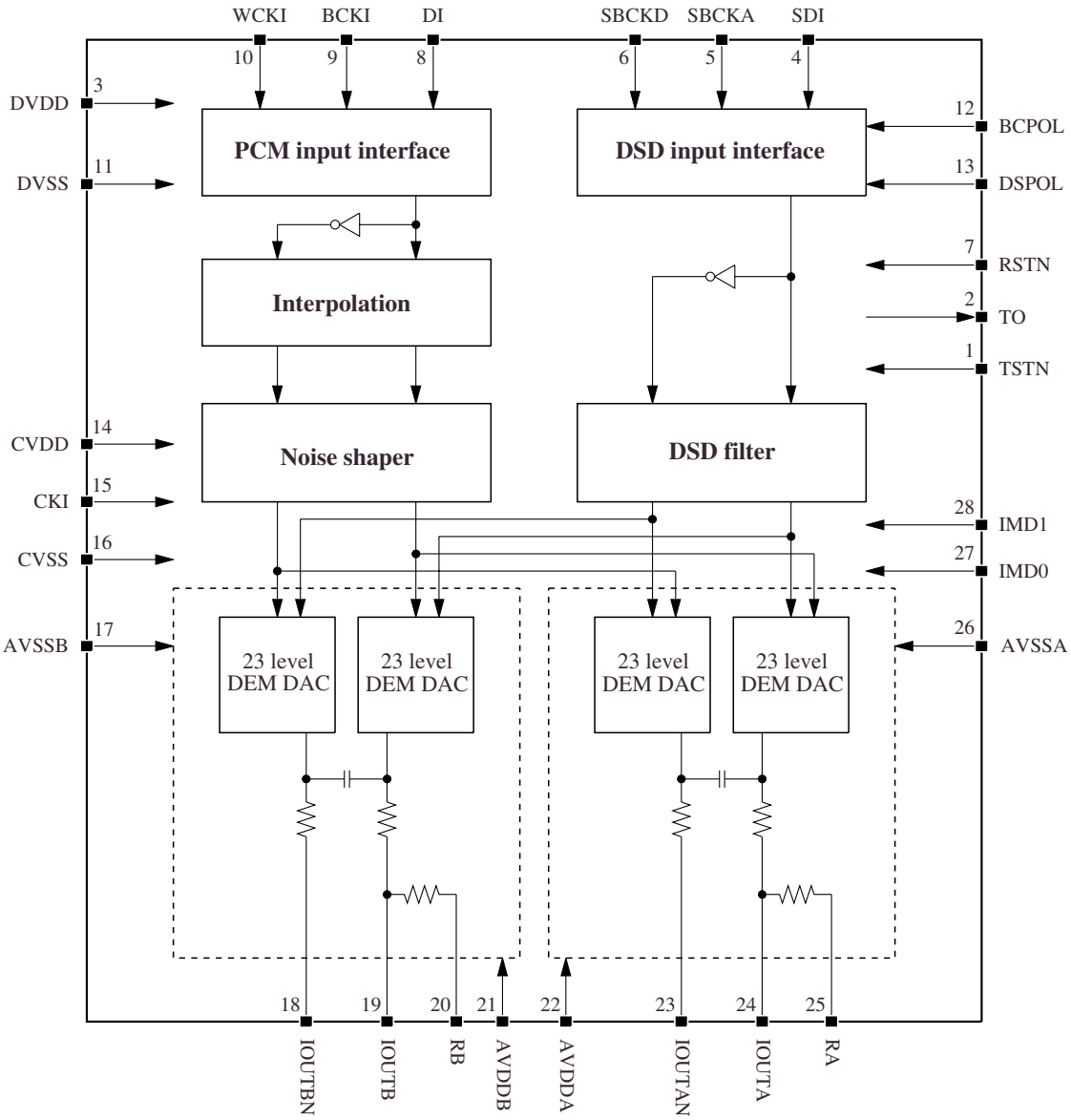



## PACKAGE DIMENSIONS

(Unit: mm)
Weight: 0.60g



## BLOCK DIAGRAM



## PIN DESCRIPTION

| Number | Name | I/O[1] | Description |
|---|---|---|---|
| 1 | TSTN | Ip | Test mode use only (tie HIGH or leave open for normal operation) |
| 2 | TO | O | Test mode use only (leave open for normal operation) |
| 3 | DVDD | – | Digital supply VDD |
| 4 | SDI | Ip | DSD data input |
| 5 | SBCKA | Ip | DSD bit clock input |
| 6 | SBCKD | Ip | DSD bit clock input (tie LOW for DSD normal input mode) |
| 7 | RSTN | Ip | System reset (active LOW) |
| 8 | DI | Ip | PCM data input |
| 9 | BCKI | Ip | PCM bit clock input |
| 10 | WCKI | Ip | PCM word clock input |
| 11 | DVSS | – | Digital ground VSS |
| 12 | BCPOL | Ip | DSD mode bit clock polarity select |
| 13 | DSPOL | Ip | DSD mode data polarity select |
| 14 | CVDD | – | System clock supply VDD |
| 15 | CKI | I | System clock |
| 16 | CVSS | – | System clock ground VSS |
| 17 | AVSSB | – | B-channel analog ground VSS |
| 18 | IOUTBN | O | B-channel analog output (inverse-phase) |
| 19 | IOUTB | O | B-channel analog output (in-phase) |
| 20 | RB | I | B-channel built-in resistor connection |
| 21 | AVDDB | – | B-channel analog supply VDD |
| 22 | AVDDA | – | A-channel analog supply VDD |
| 23 | IOUTAN | O | A-channel analog output (inverse-phase) |
| 24 | IOUTA | O | A-channel analog output (in-phase) |
| 25 | RA | I | A-channel built-in resistor connection |
| 26 | AVSSA | – | A-channel analog ground VSS |
| 27 | IMD0 | Ip | Input mode select |
| 28 | IMD1 | Ip | Input mode select |

1. Ip = input pin with built-in pull-up resistor

# SPECIFICATIONS

## Absolute Maximum Ratings

DVSS = CVSS = AVSSA = AVSSB = 0 V, DVDD = CVDD = AVDDA = AVDDB

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage range | DVDD, CVDD, AVDDA, AVDDB | –0.3 to 7.0 | V |
| Input voltage range[1] | $V_{IN1}$ | DVSS – 0.3 to DVDD + 0.3 | V |
| Storage temperature range | $T_{STG}$ | –55 to 125 | °C |
| Power dissipation | $P_D$ | 250 | mW |

1. Pins TSTN, SDI, SBCKA, SBCKD, RSTN, DI, BCKI, WCKI, BCPOL, DSPOL, IMD0, IMD1.
Note: Rating applies at power-ON and power-OFF.

## Recommended Operating Conditions

DVSS = CVSS = AVSSA = AVSSB = 0 V, DVDD = CVDD = AVDDA = AVDDB

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage range | DVDD, CVDD, AVDDA, AVDDB | 4.5 to 5.5 | V |
| Supply voltage differential | DVDD – CVDD, DVDD – AVDDA, DVDD – AVDDB, CVDD – AVDDA, CVDD – AVDDB, AVDDA – AVDDB, DVSS – CVSS, DVSS – AVSSA, DVSS – AVSSB, CVSS – AVSSA, CVSS – AVSSB, AVSSA – AVSSB | ±0.1 | V |
| Operating temperature range | $T_{OPR}$ | –40 to 85 | °C |

Note: DVDD, CVDD, AVDDA, AVDDB are connected on the LSI substrate, and so the same potential should be applied to these inputs.

## DC Electrical Characteristics

Recommended operating conditions apply unless otherwise noted.

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| DVDD, CVDD, AVDDA, AVDDB current consumption[1] | $I_{DD}$ | $f_{CKI}$ = 22.5792 MHz | – | 13 | 18 | mA |
| | | $f_{CKI}$ = 45.1584 MHz | – | 25 | 32 | mA |
| CKI HIGH-level input voltage | $V_{IHC}$ | | 0.7 × DVDD | – | – | V |
| CKI LOW-level input voltage | $V_{ILC}$ | | – | – | 0.3 × DVDD | V |
| CKI input voltage | $V_{INAC}$ | AC coupling | 1.0 | – | – | Vp-p |
| HIGH-level input voltage[2] | $V_{IH}$ | | 2.4 | – | – | V |
| LOW-level input voltage[2] | $V_{IL}$ | | – | – | 0.5 | V |
| HIGH-level output voltage[3] | $V_{OH}$ | $I_{OH}$ = –1 mA | DVDD – 0.4 | – | – | V |
| LOW-level output voltage[3] | $V_{OL}$ | $I_{OL}$ = 1 mA | – | – | 0.4 | V |
| CKI HIGH-level input current | $I_{IHC}$ | $V_{IN}$ = DVDD | 20 | 60 | 120 | µA |
| CKI LOW-level input current | $I_{ILC}$ | $V_{IN}$ = 0 V | 20 | 60 | 120 | µA |
| LOW-level input current[2] | $I_{IL1}$ | $V_{IN}$ = 0 V | – | 9 | 18 | µA |
| HIGH-level input leakage current[2] | $I_{IH1}$ | $V_{IN}$ = DVDD | – | – | 1.0 | µA |

1. all outputs have no load. Input data is an NPC test pattern.
2. Pins TSTN, SDI, SBCKA, SBCKD, RSTN, DI, BCKI, WCKI, BCPOL, DSPOL, IMD0, IMD1.
3. Pin TO.

## Switching Characteristics

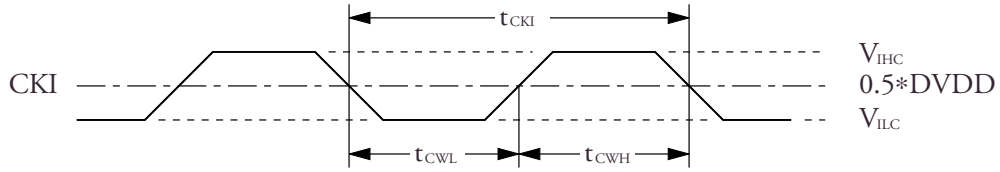
### System clock (CKI)

Operating conditions 1: $V_{DD}$ = 4.5 to 5.5V, $T_{OPR}$ = –40 to 85°C

| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| HIGH-level clock pulsewidth | $t_{CWH}$ | 7 | – | 100 | ns |
| LOW-level clock pulsewidth | $t_{CWL}$ | 7 | – | 100 | ns |
| Clock pulse cycle | $t_{CKI}$ | 27 | – | 200 | ns |

Operating conditions 2: $V_{DD}$ = 4.75 to 5.25V, $T_{OPR}$ = –40 to 70°C

| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| HIGH-level clock pulsewidth | $t_{CWH}$ | 7 | – | 100 | ns |
| LOW-level clock pulsewidth | $t_{CWL}$ | 7 | – | 100 | ns |
| Clock pulse cycle | $t_{CKI}$ | 22 | – | 200 | ns |

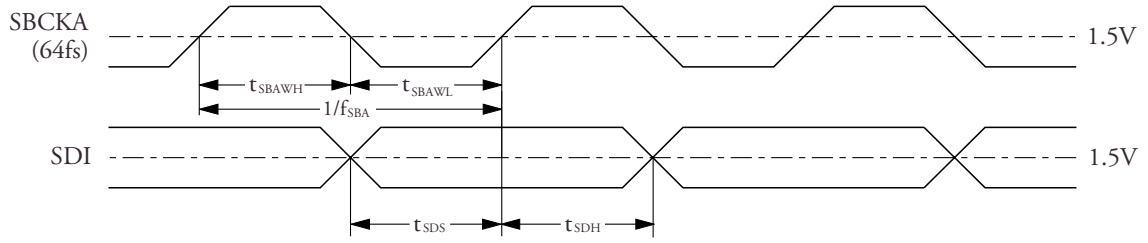



### Reset input (RSTN)

| Parameter | Symbol | Conditions | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| RSTN pulsewidth (active LOW) | $t_{RSTN}$ | At power-ON | 1 | – | – | µs |
| | | After power-ON | 100 | – | – | ns |

## DSD normal input mode (SDI, SBCKA)

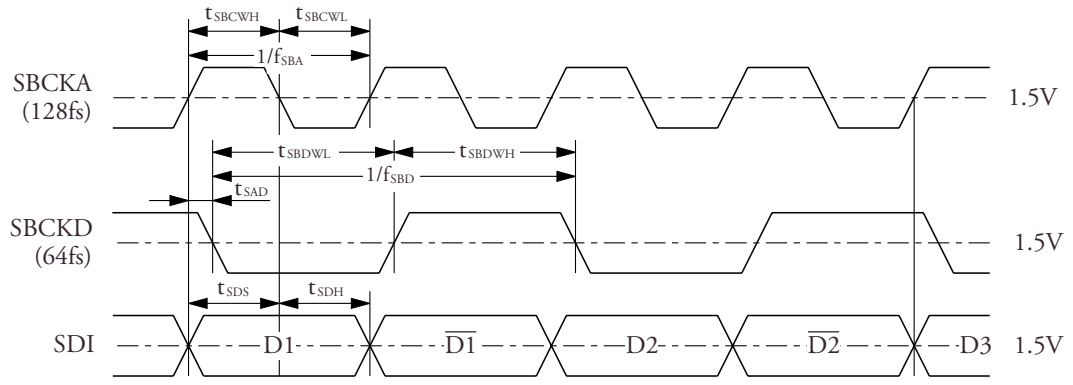
| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| SBCKA frequency | $f_{SBA}$ | – | 2.8224 | – | MHz |
| SBCKA HIGH-level pulsewidth | $t_{SBAWH}$ | 40 | – | – | ns |
| SBCKA LOW-level pulsewidth | $t_{SBAWL}$ | 40 | – | – | ns |
| SDI setup time | $t_{SDS}$ | 10 | – | – | ns |
| SDI hold time | $t_{SDH}$ | 10 | – | – | ns |




SBCKD = LOW
This figure applies when BCPOL = LOW (SBCKA rising edge read-in).
When BCPOL = HIGH, SBCKA has opposite phase.

## DSD phase-modulated input mode (SDI, SBCKA, SBCKD)

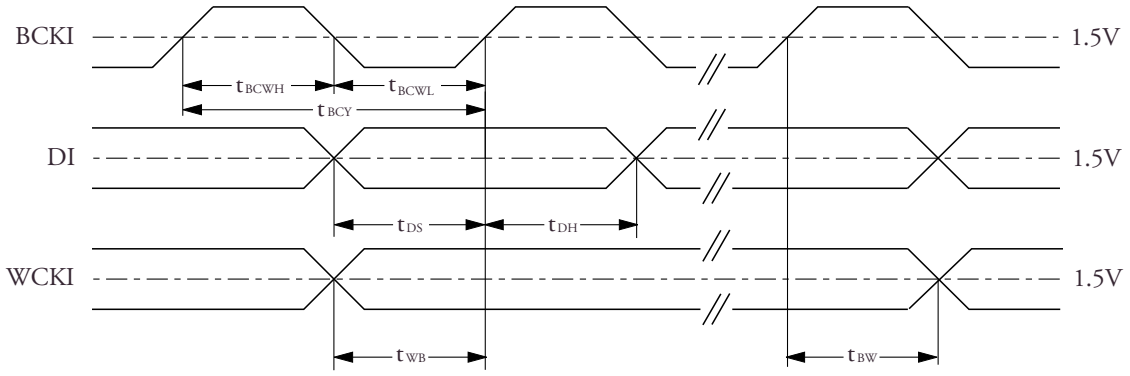
| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| SBCKA frequency | $f_{SBA}$ | – | 5.6448 | – | MHz |
| SBCKA HIGH-level pulsewidth | $t_{SBAWH}$ | 20 | – | – | ns |
| SBCKA LOW-level pulsewidth | $t_{SBAWL}$ | 20 | – | – | ns |
| SBCKD frequency | $f_{SBD}$ | – | 2.8224 | – | MHz |
| SBCKD HIGH-level pulsewidth | $t_{SBDWH}$ | 40 | – | – | ns |
| SBCKD LOW-level pulsewidth | $t_{SBDWL}$ | 40 | – | – | ns |
| SDI setup time | $t_{SDS}$ | 10 | – | – | ns |
| SDI hold time | $t_{SDH}$ | 10 | – | – | ns |
| SBCKA rising edge → SBCKD falling edge | $t_{SAD}$ | – 20 | – | 20 | ns |




BCPOL = LOW

## PCM mode data input (DI, BCKI, WCKI)

| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| BCKI HIGH-level pulsewidth | $t_{BCWH}$ | 7 | – | – | ns |
| BCKI LOW-level pulsewidth | $t_{BCWL}$ | 7 | – | – | ns |
| BCKI pulse cycle | $t_{BCY}$ | 22 | – | – | ns |
| DI setup time | $t_{DS}$ | 5 | – | – | ns |
| DI hold time | $t_{DH}$ | 5 | – | – | ns |
| WCKI edge → first BCKI rising edge | $t_{WB}$ | 10 | – | – | ns |
| Last BCKI rising edge → WCKI edge | $t_{BW}$ | 10 | – | – | ns |



## DSD Mode Analog Characteristics

### Measurement Conditions

| | | | |
|---|---|---|---|
| Op-amp | | : | JRC NJM5534D |
| Supply voltage | SM5866AS | : | DVDD = CVDD = AVDDA = AVDDB = 5V,<br>DVSS = CVSS = AVSSA = AVSSB = 0V |
| | NJM5534D | : | ± 15V |
| Mode setting | | : | H-Mode (uses H-Filter) |
| Measurement temperature | | : | 25°C |
| Input data | | : | SUPER AUDIO CD DAC Test Disc (PHILIPS, 3122-783-00632) |
| System clock | | : | 22.5792MHz |
| Measurement equipment | | : | Audio Precision System Two (RMS mode) |
| Filter conditions | | : | THD + N 22Hz HPF, 20kHz LPF (FLP-A20K), Unweighted |
| | | | D.R 22Hz HPF, 20kHz LPF (AES17), A-weighted (FIL-AWT) |
| | | | S/N 22Hz HPF, 20kHz LPF (AES17), A-weighted (FIL-AWT) |
| Measurement circuit | | : | Refer to “Measurement circuit”. |

### Analog Characteristics

| Parameter | | Symbol | Conditions | Rating | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | min | typ | max | |
| LSI output level[1] | | $V_{out1}$ | 1 kHz, 0 dB | 0.92 | 0.97 | 1.02 | Vrms |
| Evaluation board output level | | $V_{out2}$ | 1 kHz, 0 dB | – | 5.7 | – | Vrms |
| Total harmonic distortion | 0dB | THD + N | 1 kHz, 0 dB | – | –109 (0.00036%) | –105 (0.00056%) | dB |
| | –20dB | | 1 kHz, –20 dB | – | –92 | –88 | dB |
| | –60dB | | 1 kHz, –60 dB | – | –52 | –48 | dB |
| Dynamic range | | D.R | 1 kHz, –60 dB | 111 | 115 | – | dB |
| Signal-to-noise ratio | | S/N | 1 kHz, 0 dB/–∞ | 112 | 116 | – | dB |

1. Input stage I/V op-amp, U101 output level (when R101 = 0Ω)

## PCM Mode Analog Characteristics

### Measurement Conditions

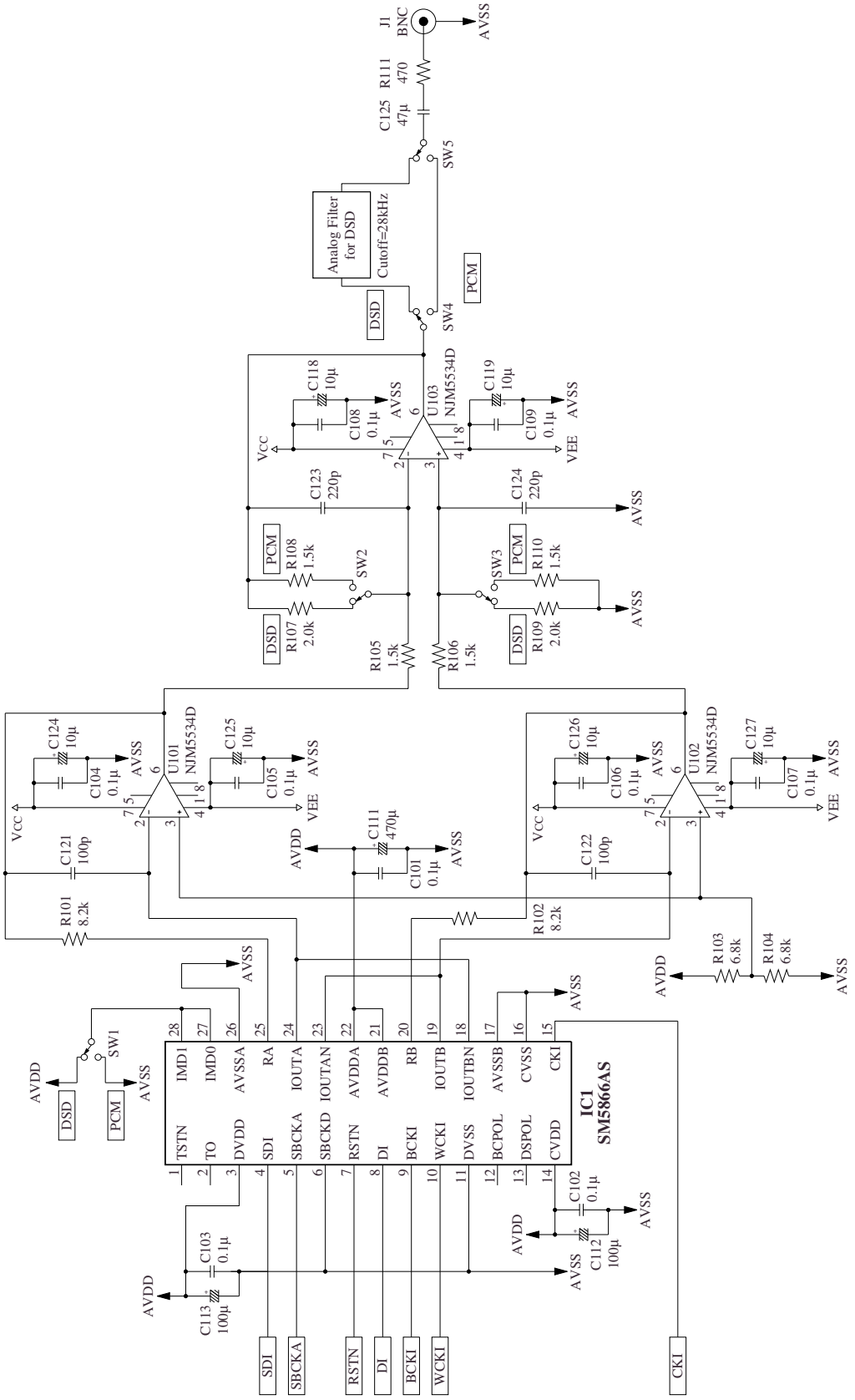
| | | | |
|---|---|---|---|
| Digital filter | | : | NPC SM5847AF |
| Op-amp | | : | JRC NJM5534D |
| Supply voltage | SM5866AS | : | DVDD = CVDD = AVDDA = AVDDB = 5V,<br>DVSS = CVSS = AVSSA = AVSSB = 0V |
| | SM5847AF | : | + 3.3V |
| | NJM5534D | : | ± 15V |
| Mode settings | | : | D-Mode |
| Measurement temperature | | : | 25°C |
| Input data | | : | 44.1kHz sampling, 24-bit data, no dither |
| System clock | | : | 22.5792MHz (512fs), 64fs operation |
| Measurement equipment | | : | Audio Precision System Two (RMS mode) |
| Filter conditions | | : | THD + N 22Hz HPF, 20kHz LPF (FLP-A20K) Unweighted |
| | | | D.R 22Hz HPF, 22kHz LPF, A-weight (FIL-AWT) |
| | | | S/N 22Hz HPF, 22kHz LPF, A-weight (FIL-AWT) |
| Measurement circuit | | : | Refer to “Measurement circuit”. |

### Analog Characteristics

| Parameter | Symbol | Conditions | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| LSI output level[1] | $V_{out1}$ | 1 kHz, 0 dB | 1.23 | 1.28 | 1.33 | Vrms |
| Evaluation board output level | $V_{out2}$ | 1 kHz, 0 dB | – | 5.7 | – | Vrms |
| Total harmonic distortion | THD + N | 1 kHz, 0 dB | – | 0.0005<br>(–106dB) | 0.0010<br>(–100dB) | % |
| Dynamic range | D.R | 1 kHz, –60 dB | 106 | 112 | – | dB |
| Signal-to-noise ratio | S/N | 1 kHz, 0 dB/–∞ | 117 | 120 | – | dB |

1. Input stage I/V op-amp, U101 output level (when R101 = 0Ω)

## Measurement circuit



# FUNCTIONAL DESCRIPTION

## Analog Pins

### Current output pins (IOUTA, IOUTAN, IOUTB, IOUTBN)

The SM5866AS generates current output A differential outputs, formed by input data in-phase signal processed by noise shaper A and then 23-level D/A conversion, and current output B differential outputs, formed by input data inverse-phase signal processed by noise shaper B and then 23-level D/A conversion. A and B differential outputs each have a in-phase output and inverse-phase output: A in-phase output on IOUTA, A inverse-phase output on IOUTAN, B in-phase output on IOUTB, and B inverse-phase output on IOUTBN.

Using external circuits, outputs IOUTA and IOUTAN are added and I/V converted, and IOUTB and IOUTBN are added and I/V converted. Then, the converted signals are input to an op-amp stage to obtain the final output analog signal.

### Feedback resistor connection pins (RA, RB)

There are internal built-in resistors connected between IOUTA and RA and between IOUTB and RB, which can be used as op-amp feedback resistors. These resistors have a resistance of approximately 6.8kΩ. An external resistor can be connected to the internal resistor, in serial or parallel, in order to adjust the analog output level. Note, however, that the internal resistance can vary by as much as ± 20% between individual LSI devices, and thus the output level may change with the difference in the ratio of internal resistance to external resistance.

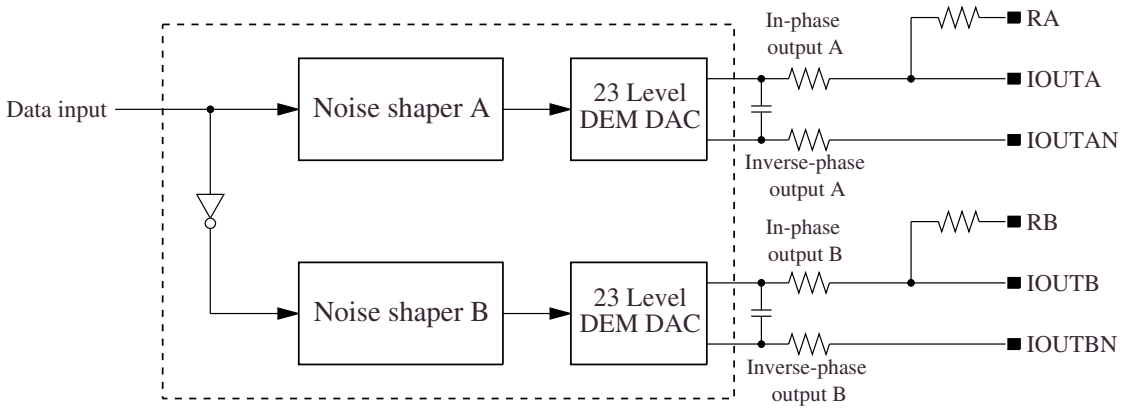



Figure 1. Analog outputs

## Input Mode Settings (IMD0, IMD1)

IMD0 and IMD1 pin settings switch between the DSD and PCM operating modes. In DSD mode, the DSD signal high-frequency components can be removed using one of DSD filters (H-Filter and G-Filter), or the signal can be left unfiltered.

Table 1. Input mode setting

| IMD0 | IMD1 | Mode name | Input format | DSD FIR filter |
|---|---|---|---|---|
| H | H | H | 1bit, 64fs, DSD | H-Filter |
| H | L | G | 1bit, 64fs, DSD | G-Filter |
| L | H | A | 1bit, 64fs, DSD | None |
| L | L | D | 24bit, 8fs, PCM | None |

## DSD Filter Characteristics

### H-Filter frequency response

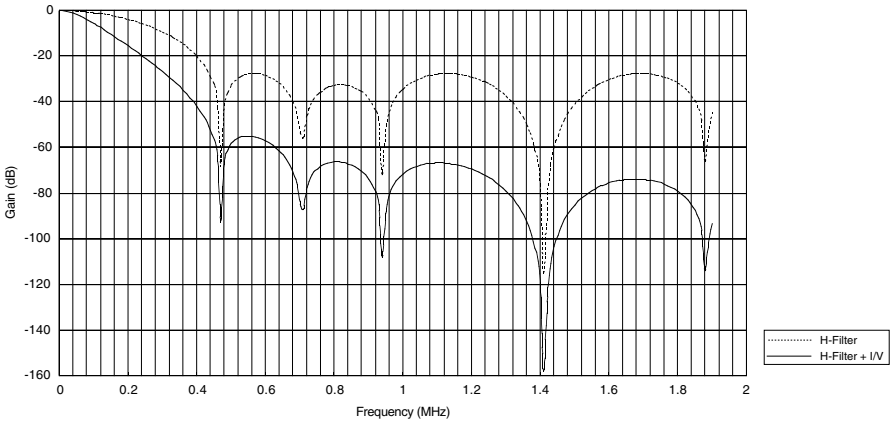



Figure 2. SM5866AS H-Filter + I/V Halfband Characteristics

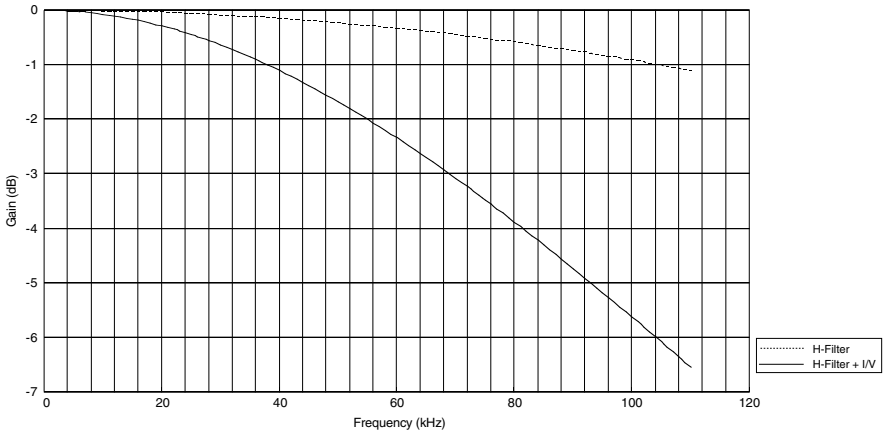



Figure 3. SM5866AS H-Filter + I/V Passband Characteristics

## G-Filter frequency response

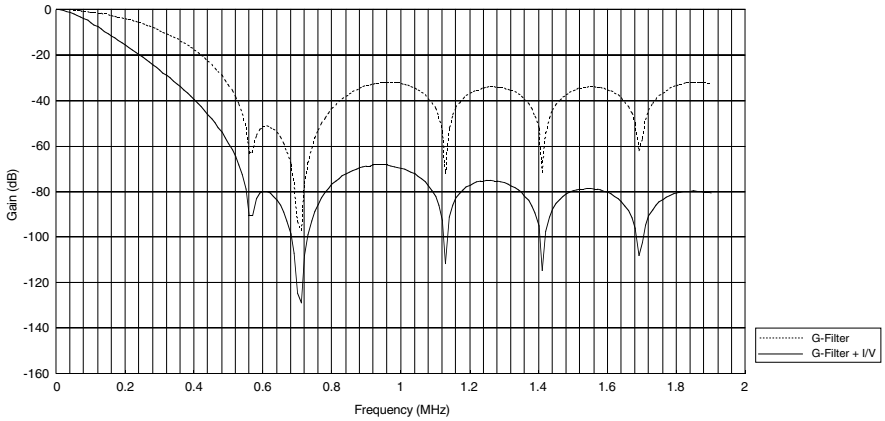



Figure 4. SM5866AS G-Filter + I/V Halfband Characteristics

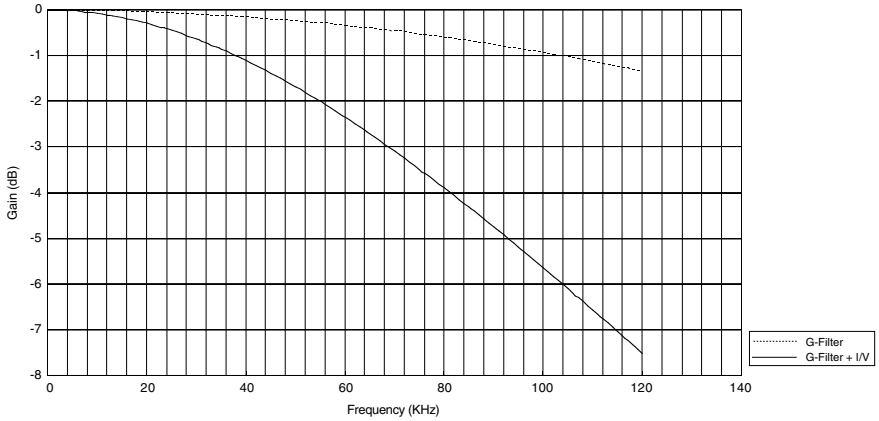



Figure 5. SM5866AS G-Filter + I/V Passband Characteristics

## DSD Mode Data Input Pins (SDI, SBCKA, SBCKD)

In DSD mode, the following 2 data input formats are supported.

(1) Normal input format (refer to "DSD normal input mode")

A 64fs clock is input on SBCKA, and 64fs rate DSD data in sync with the clock is input on SDI. SBCKD is tied LOW.

(2) Phase-modulated format (refer to "DSD phase-modulated input mode")

A 128fs clock is input on SBCKA, a 64fs clock is input on SBCKD, and 128fs rate phase-modulated DSD data in sync with both clocks is input on SDI.
The DSD data phase modulation depends on the clock interval. When the 64fs rate DSD data is "1", SDI = HIGH if SKCKD = LOW or SDI = LOW if SBCKD = HIGH. When the DSD data is "0", SDI = LOW if SKCKD = LOW or SDI = HIGH if SBCKD = HIGH.

## DSD Mode Bit Clock Polarity Select (BCPOL)

When BCPOL = LOW, data on SDI is read in on the rising edge of SBCKA. When BCPOL = HIGH, data on SDI is read in on the falling edge of SBCKA.

## DSD Mode Analog Output Polarity Select (DSPOL)

When DSPOL = HIGH, the analog output has in-phase polarity relative to the SDI input data. When DSPOL = LOW, the analog output has inverse-phase polarity relative to the SDI input data.

## PCM Mode Data Inputs (DI, BCKI, WCKI)

- Input data format

  Data is in MSB-first, 24-bit serial, 2s-complement format.

- Jitter-free function

  The SM5866AS reads serial input data on DI into the first-stage register in sync with the word clock on WCKI, while processed data is read into the last-stage register in sync with a clock derived by frequency division of the system clock. The word clock and the system clock continually undergo phase comparison and if a phase difference is detected, the system clock timing is corrected. Accordingly, if large jitter occurs in the word clock or the data sampling rate between input/output varies, the internal computational operation is not affected.

## System Reset (RSTN)

The SM5866AS must be reset under the following conditions:

- At power-ON
- When the CKI system clock stops or other similar occurrences

A reset occurs when RSTN goes LOW.

## PCM Mode Theoretical Quantization Noise

During PCM operation (D-Mode), residual quantization noise in the audio signal band to the high-frequency band, caused by the operation of the 3rd-order 23-level quantizer noise shaper, is greatly reduced. Figure 6 shows the theoretical quantization noise component for 16fs to 96fs operation.

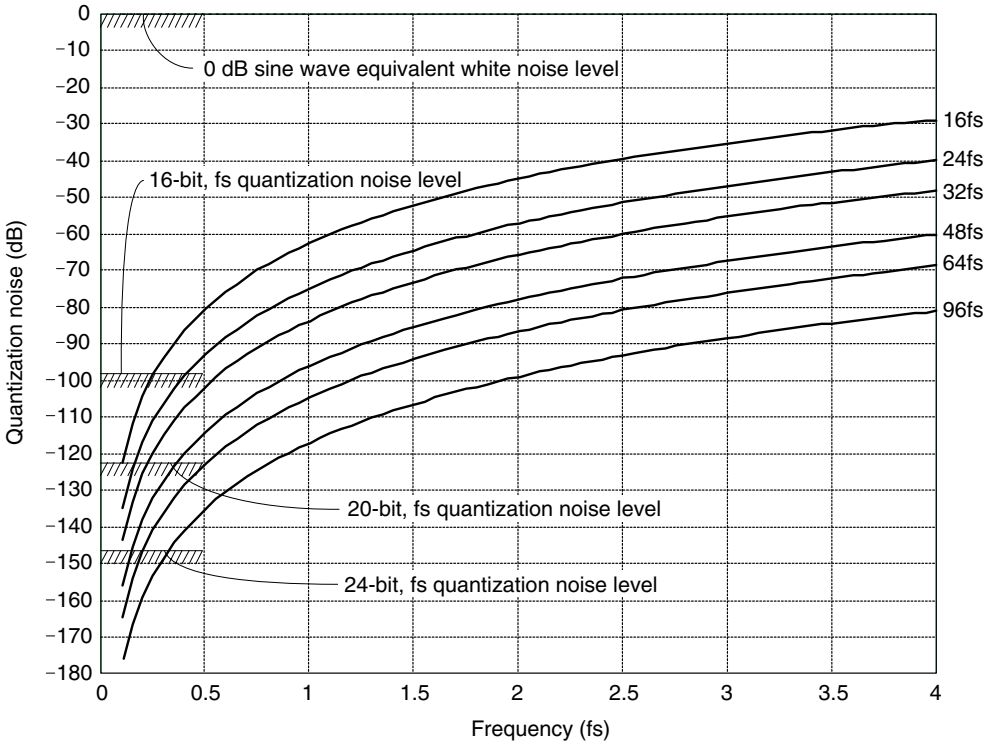



Figure 6. Quantization noise level

## PCM Mode Oversampling Operation

The SM5866AS receives signal output from either a 8-times or 4-times oversampling digital filter. Internally, this data is further oversampled up to the noise shaper operating rate. The internal oversampling ratio is determined automatically by the system clock frequency and the input sampling frequency. This internal oversampling ratio must be an integer, and therefore must satisfy the conditions shown in table 2.

Table 2. Internal oversampling conditions

| | |
|---|---|
| $f_{WCKI}$ and $f_{CKI}$ conditions[1] | $f_{CKI} = f_{WCKI} \times 8 \times n$ where n = 1, 2, 3, ... |
| Noise shaper operating frequency | $f_{ns} = f_{WCKI} \times n = \frac{f_{CKI}}{8}$ |

1. $f_{WCKI}$ = word clock frequency, $f_{CKI}$ = input system clock frequency, n = internal oversampling ratio

## PCM Mode System Clock Frequency Example

With the circuit structure shown in figure 7, the oversampling rate for various sampling frequencies is given in table 3.

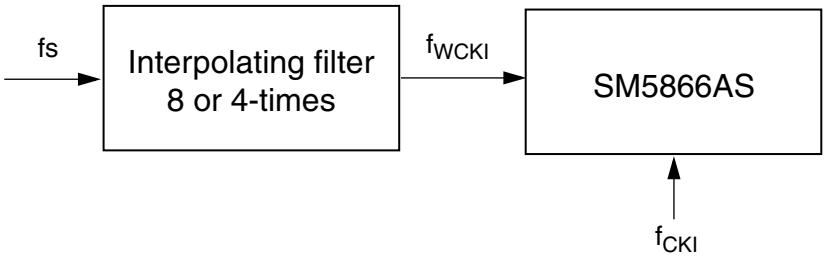



Figure 7. Circuit structure

Table 3. System clock frequency table

| fs | $f_{CKI}$ system clock frequency | Noise shaper operating rate | Internal ratio (8fs input) | Internal ratio (4fs input) |
|---|---|---|---|---|
| 16kHz | 6.144MHz (384fs) | 48fs | 6 | 12 |
| 16kHz | 8.192MHz (512fs) | 64fs | 8 | 16 |
| 16kHz | 12.288MHz (768fs) | 96fs | 12 | 24 |
| 32kHz | 6.144MHz (192fs) | 24fs | 3 | 6 |
| 32kHz | 8.192MHz (256fs) | 32fs | 4 | 8 |
| 32kHz | 12.288MHz (384fs) | 48fs | 6 | 12 |
| 32kHz | 16.384MHz (512fs) | 64fs | 8 | 16 |
| 32kHz | 24.576MHz (768fs) | 96fs | 12 | 24 |
| 44.1kHz | 8.4672MHz (192fs) | 24fs | 3 | 6 |
| 44.1kHz | 11.2896MHz (256fs) | 32fs | 4 | 8 |
| 44.1kHz | 16.9344MHz (384fs) | 48fs | 6 | 12 |
| 44.1kHz | 22.5792MHz (512fs) | 64fs | 8 | 16 |
| 44.1kHz | 33.8688MHz (768fs) | 96fs | 12 | 24 |
| 48kHz | 9.216MHz (192fs) | 24fs | 3 | 6 |
| 48kHz | 12.288MHz (256fs) | 32fs | 4 | 8 |
| 48kHz | 18.432MHz (384fs) | 48fs | 6 | 12 |
| 48kHz | 24.576MHz (512fs) | 64fs | 8 | 16 |
| 48kHz | 36.864MHz (768fs) | 96fs | 12 | 24 |
| 88.2kHz | 16.9344MHz (192fs) | 24fs | 3 | 6 |
| 88.2kHz | 22.5792MHz (256fs) | 32fs | 4 | 8 |
| 88.2kHz | 33.8688MHz (384fs) | 48fs | 6 | 12 |
| 88.2kHz | 45.1584MHz (512fs) | 64fs | 8 | 16 |
| 96kHz | 18.432MHz (192fs) | 24fs | 3 | 6 |
| 96kHz | 24.576MHz (256fs) | 32fs | 4 | 8 |
| 96kHz | 36.864MHz (384fs) | 48fs | 6 | 12 |
| 176.4kHz | 33.8688MHz (192fs) | 24fs | 3 | 6 |
| 176.4kHz | 45.1584MHz (256fs) | 32fs | 4 | 8 |
| 192kHz | 36.864MHz (192fs) | 24fs | 3 | 6 |

## PCM MODE INPUT TIMING EXAMPLE

PCM mode input data in 24-bit word length, MSB-first, right-justified format

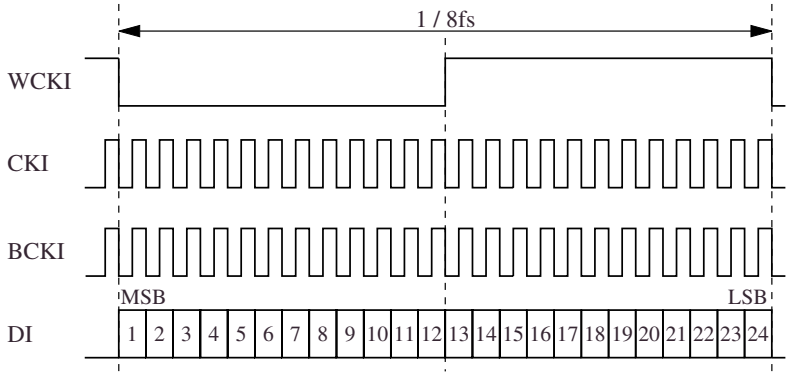



Figure 8. 192fs system clock input

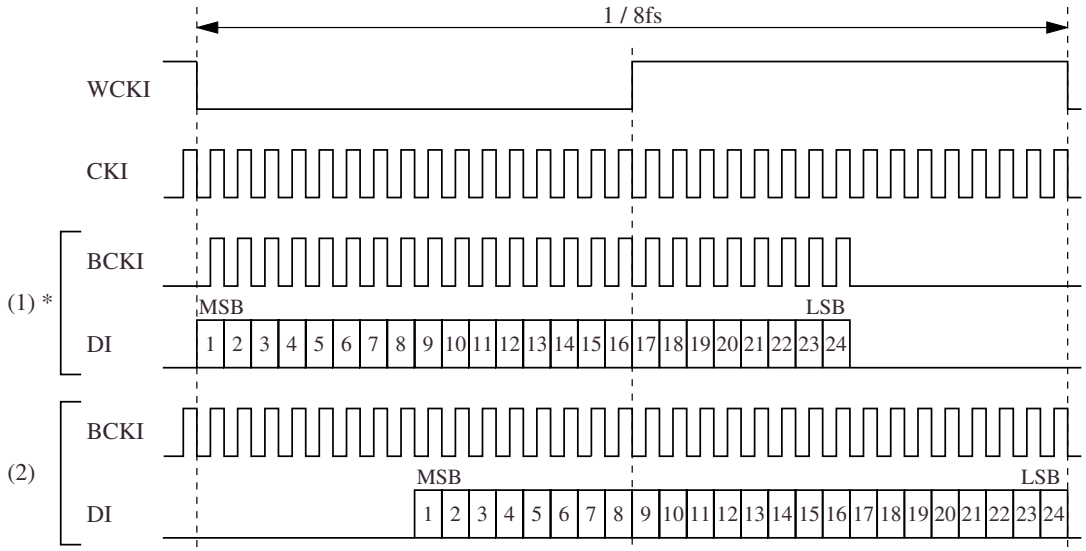



Figure 9. 256fs system clock input

*: When the input data fits within the word clock cycle, the input data position (left/right) can be changed.

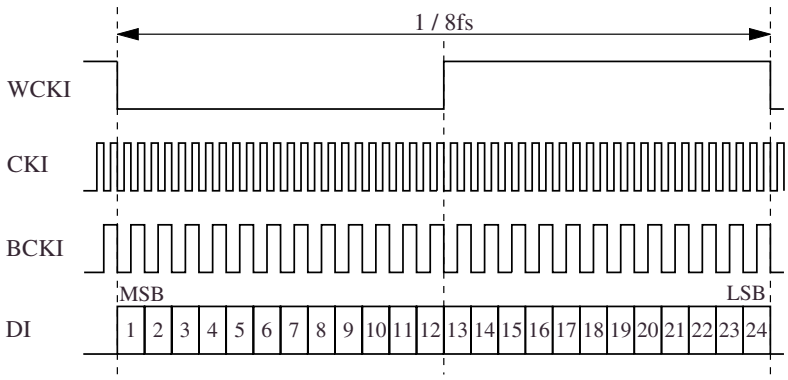



Figure 10. 384fs system clock input

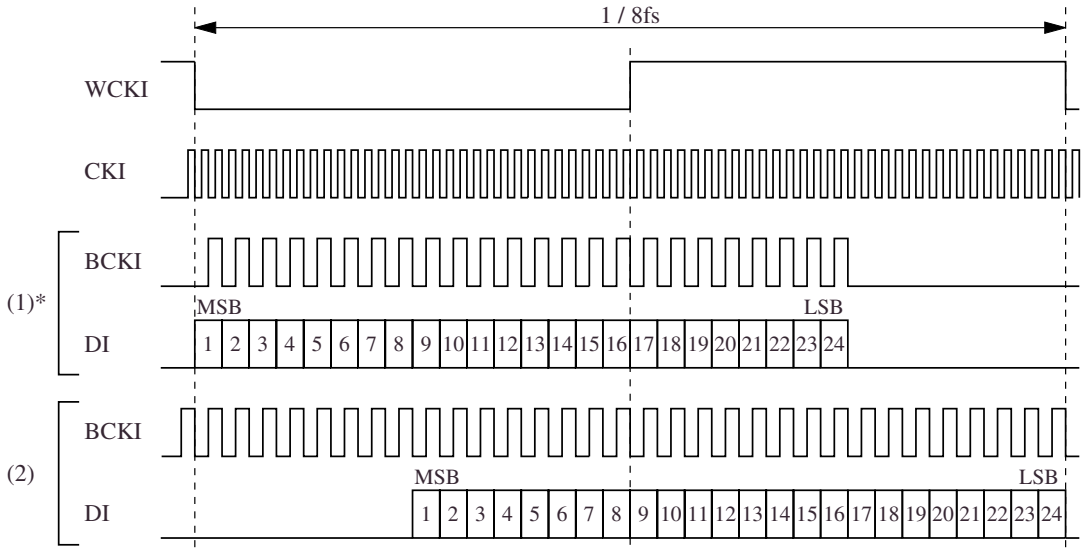



Figure 11. 512fs system clock input

*: When the input data fits within the word clock cycle, the input data position (left/right) can be changed.

# TYPICAL CIRCUIT DIAGRAM

## DSD Mode Input Interface Connection Example

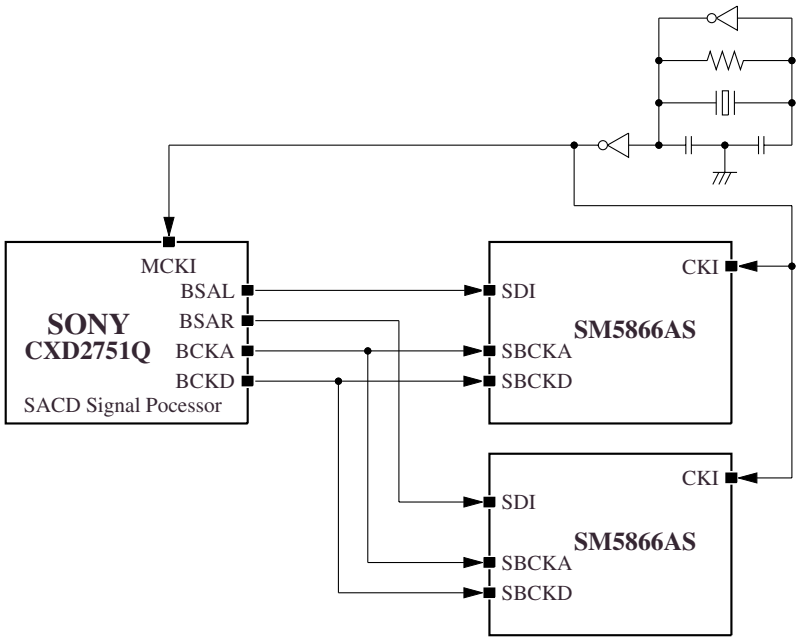



Figure 12. DSD Mode input interface connection example

## PCM Mode Input Interface Connection Example

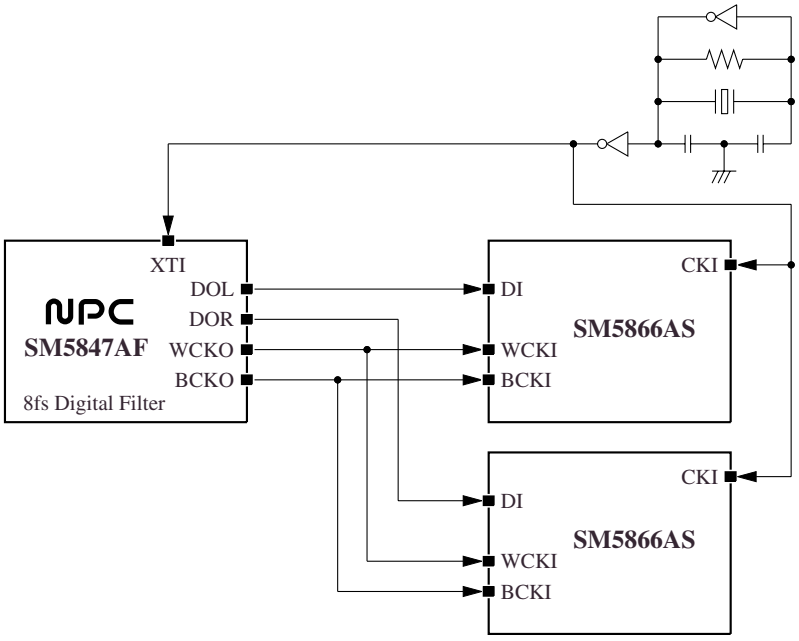



Figure 13. PCM Mode input interface connection example

## Analog Output Connection Example

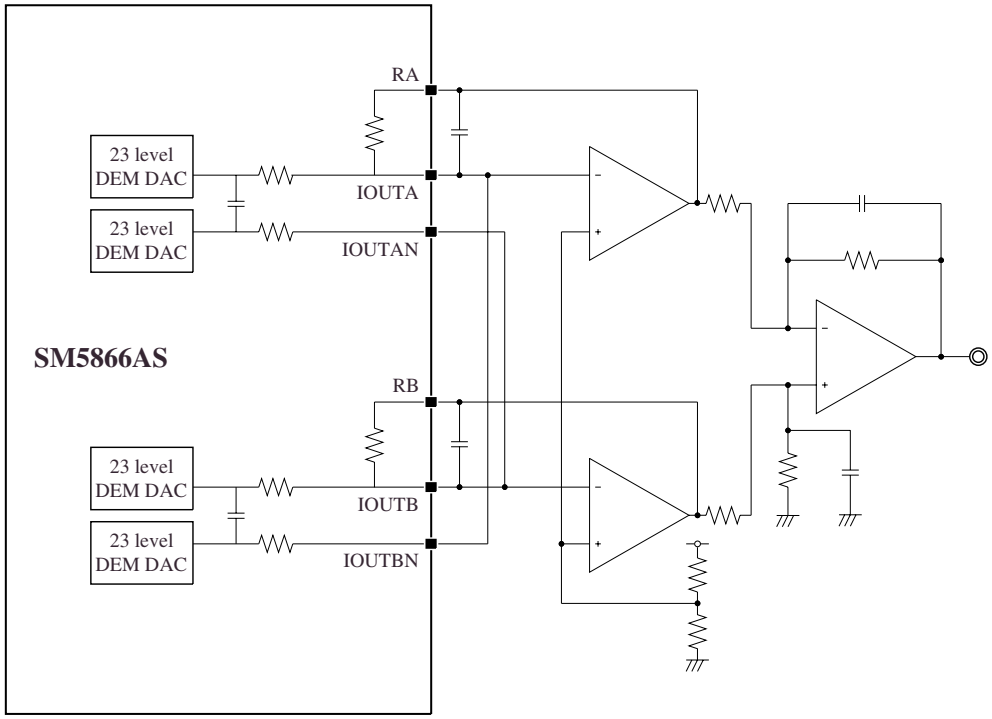



Figure 14. Connection example 1

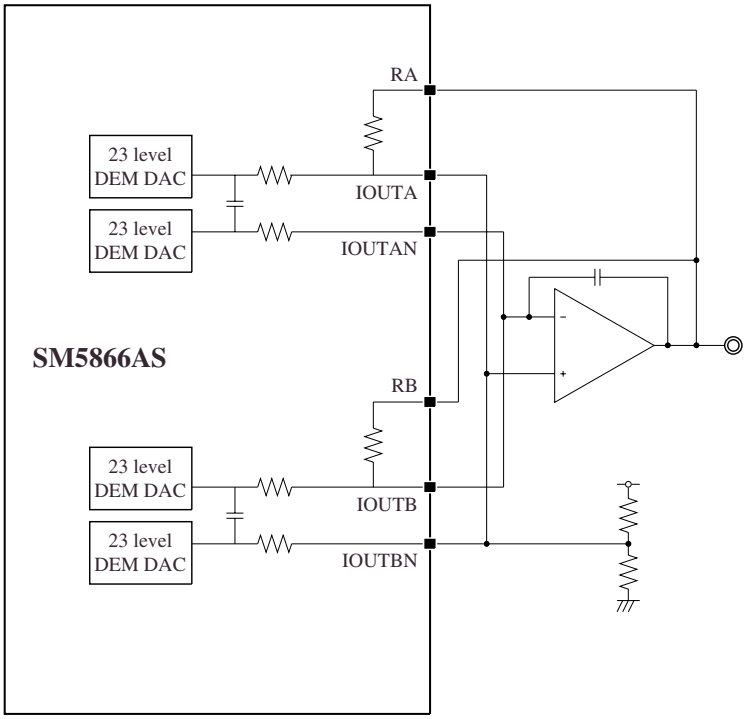



Figure 15. Connection example 2

Note:
The connection examples are connections for formats described earlier, with no specific guaranteed output analog characteristics.
NPC does not accept responsibility for any patent issues relating to usage of application circuits published in this document.

## DYNAMICS CHARACTERISTICS

### DSD mode (H-Mode) Dynamics Characteristics (Under Measurement Condition in page 8)

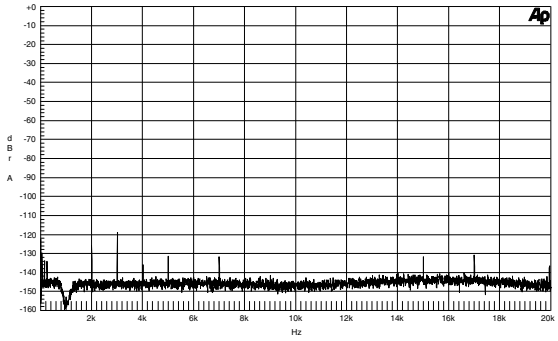



Figure 16. 0dB input FFT
(with 1kHz notch filter 32768 pts. 8 average)

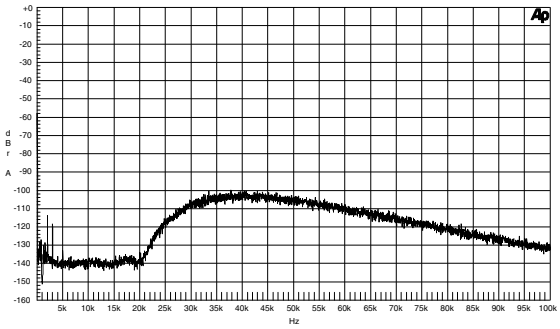



Figure 17. 0dB input FFT
(with 1kHz notch filter 32768 pts. 8 average)

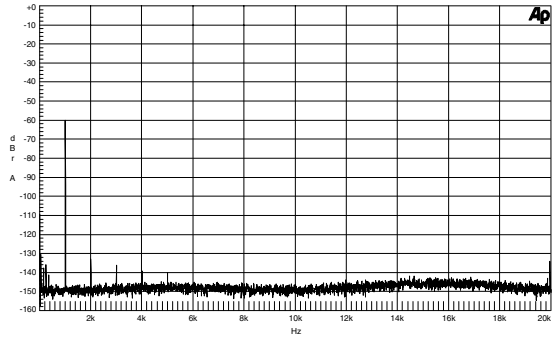



Figure 18. −60dB input FFT (32768 pts. 8 average)

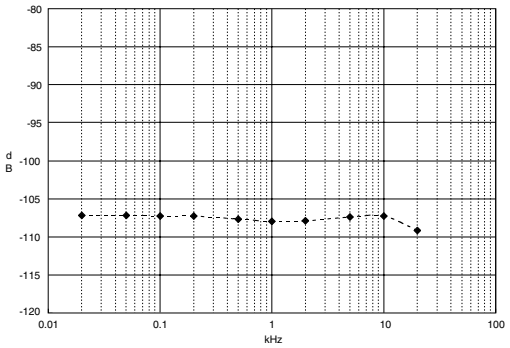



Figure 19. THD + N vs. frequency

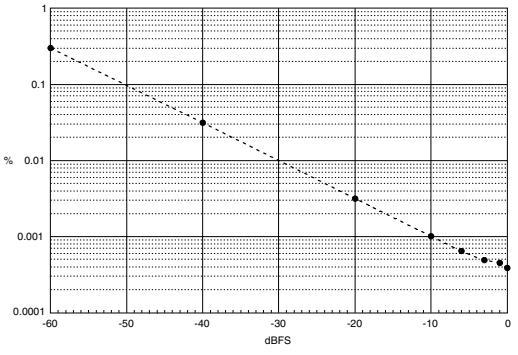



Figure 20. THD + N (%) vs. amplitude

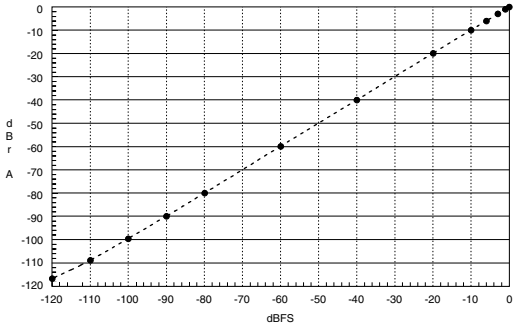



Figure 21. Linearity

Note. Input data: SUPER AUDIO CD DAC Test Disc (PHILIPS, 3122-783-00632)

## PCM mode (D-Mode) Dynamics Characteristics (Under Measurement Condition in page 9)

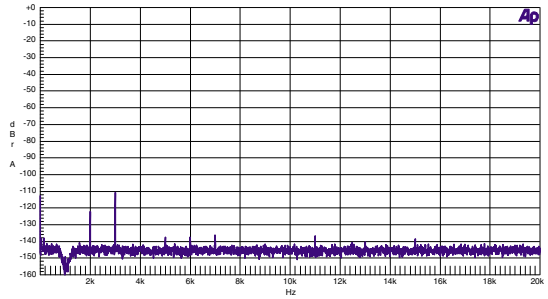



Figure 22. 0dB input FFT
(with 1kHz notch filter 32768 pts. 8 average)

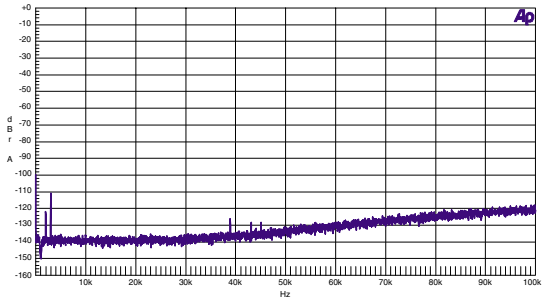



Figure 23. 0dB input FFT
(with 1kHz notch filter 32768 pts. 8 average)

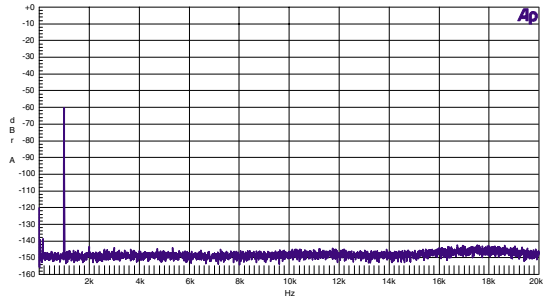



Figure 24. −60dB input FFT (32768 pts. 8 average)

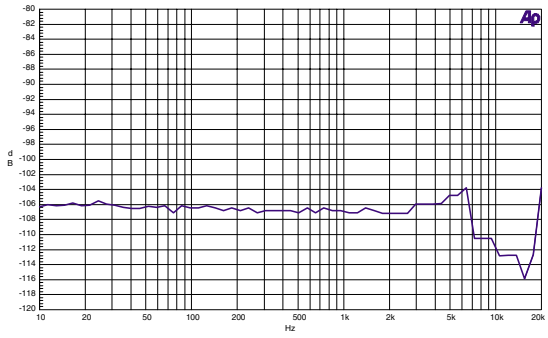



Figure 25. THD + N vs. frequency

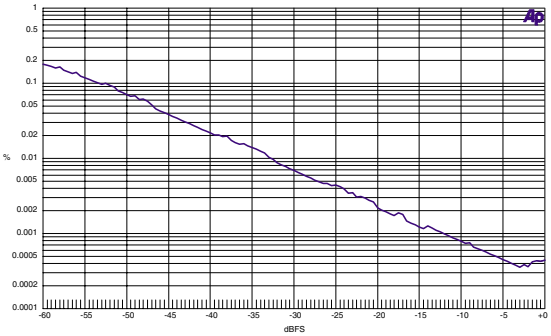



Figure 26. THD + N (%) vs. amplitude

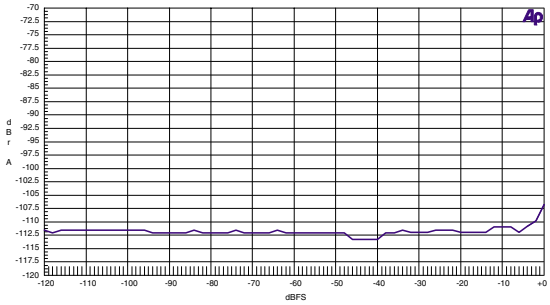



Figure 27. THD + N (dB) vs. amplitude

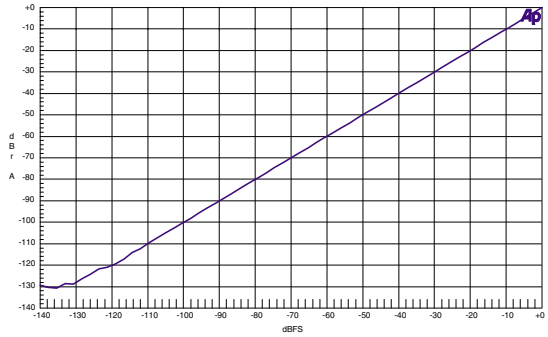



Figure 28. Linearity

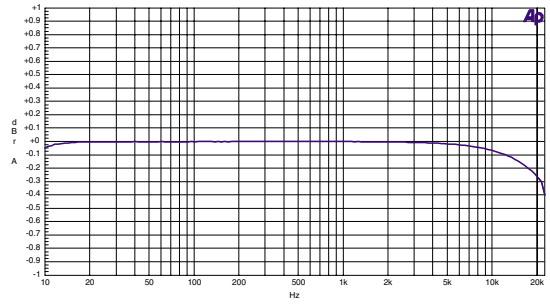



Figure 29. Frequency response

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