256Kx32 SRAM MODULE *PRELIMINARY**

FEATURES

- Access Times 20, 25, 35ns
- MIL-STD-883 Compliant Devices Available
- Packaging
  - 66 pin, PGA Type, 1.185 inch square, Hermetic Ceramic HIP (Package 401)
  - 68 lead, 40mm, Hermetic CQFP (Package 501)
- Organized as 256Kx32, User Configurable as 512Kx16
- Upgradable to 512Kx32 for future expansion
- Data I/O Compatible with 3.3V devices
- 2V Data Retention devices available (WS256K32L-XXX low power version only)
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Weight
  WS256K32N-XHX - 13 grams typical
  WS256K32-XG4X - 20 grams typical

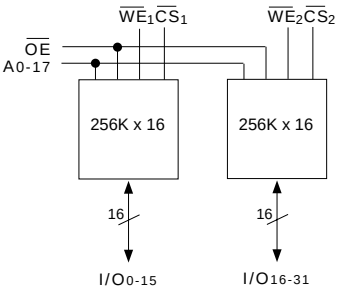
* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

FIG. 1 PIN CONFIGURATION FOR WS256K32N-XHX

TOP VIEW

1	12	23		34	45	56
I/O8	NC	I/O15		I/O24	VCC	I/O31
I/O9	NC	I/O14		I/O25	NC	I/O30
I/O10	GND	I/O13		I/O26	NC	I/O29
A13	I/O11	I/O12		A6	I/O27	I/O28
A14	A10	$\overline{OE}$		A7	A3	A0
A15	A11	NC		NC	A4	A1
A16	A12	$\overline{WE_1}$		A8	A5	A2
A17	VCC	I/O7		A9	$\overline{WE_2}$	I/O23
I/O0	$\overline{CS_1}$	I/O6		I/O16	$\overline{CS_2}$	I/O22
I/O1	NC	I/O5		I/O17	GND	I/O21
I/O2	I/O3	I/O4		I/O18	I/O19	I/O20
11	22	33		44	55	66

BLOCK DIAGRAM

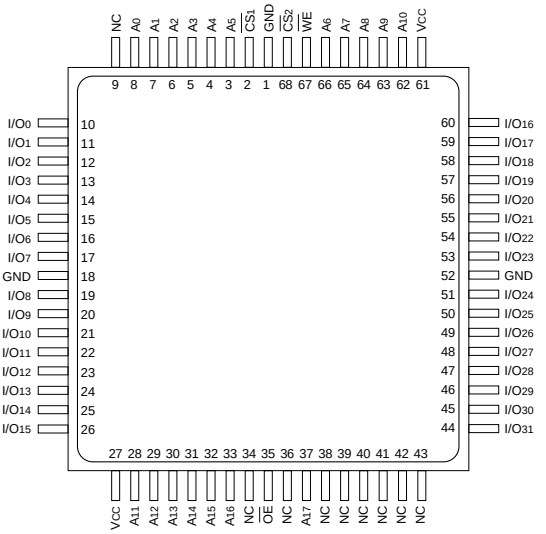


PIN DESCRIPTION

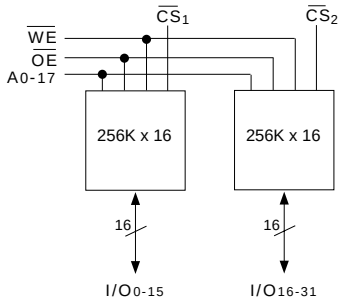
I/O0-31	Data Inputs/Outputs
A0-17	Address Inputs
$\overline{WE}_{1-2}$	Write Enables
$\overline{CS}_{1-2}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

FIG. 2 PIN CONFIGURATION FOR WS256K32-XG4X

TOP VIEW



BLOCK DIAGRAM



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
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$\overline{WE}$	Write Enable
$\overline{CS}$1-2	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp (Mil)	T_A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	28	pF
$\overline{WE}_{1\text{-}2}$ capacitance HIP (PGA)	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
CQFP G4			28	
$\overline{CS}_{1\text{-}2}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	28	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current x 32 Mode	$I_{CC \times 32}$	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		550	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		34	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, Vcc = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, Vcc = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

LOW POWER DATA RETENTION CHARACTERISTICS

(WS256K32L-XXX ONLY)

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Supply Voltage	V_{DR}	$\overline{CS}$ ≥ V_{CC} -0.2V	2.0		5.5	V
Data Retention Current	I_{CCDR3}	V_{CC} = 3V		1.0	16	mA

AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-20		-25		-35		Units
Read Cycle		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		35		ns
Address Access Time	t_{AA}		20		25		35	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns
Chip Select Access Time	t_{ACS}		20		25		35	ns
Output Enable to Output Valid	t_{OE}		12		15		20	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		12		15		20	ns
Output Disable to Output in High Z	t_{OHZ}[1]		12		15		20	ns

1. This parameter is guaranteed by design but not tested.

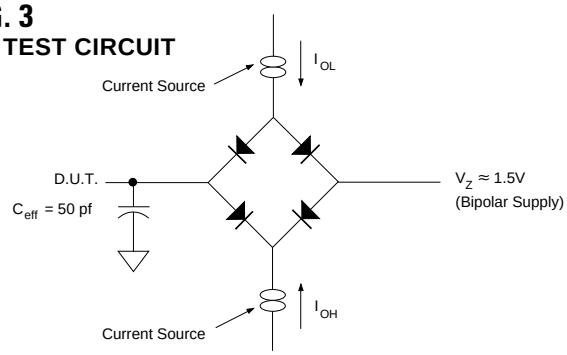
AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-20		-25		-35		Units
Write Cycle		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20		25		35		ns
Chip Select to End of Write	t_{CW}	17		20		25		ns
Address Valid to End of Write	t_{AW}	17		20		25		ns
Data Valid to End of Write	t_{DW}	12		15		20		ns
Write Pulse Width	t_{WP}	17		20		25		ns
Address Setup Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	2		2		2		ns
Output Active from End of Write	t_{OW}[1]	0		0		0		ns
Write Enable to Output in High Z	t_{WHZ}[1]		8		10		15	ns
Data Hold Time	t_{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 3
AC TEST CIRCUIT

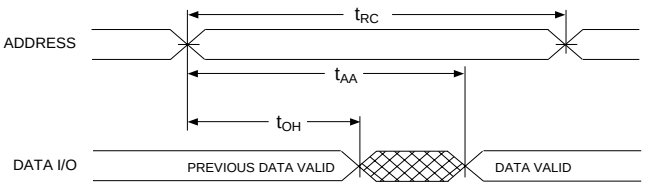


AC TEST CONDITIONS

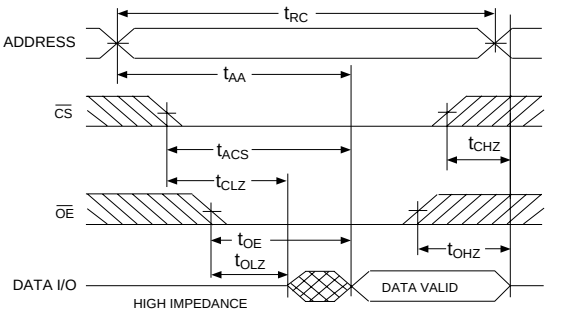
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 4
TIMING WAVEFORM - READ CYCLE

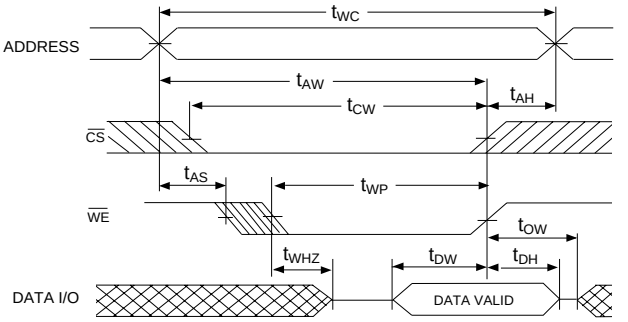


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



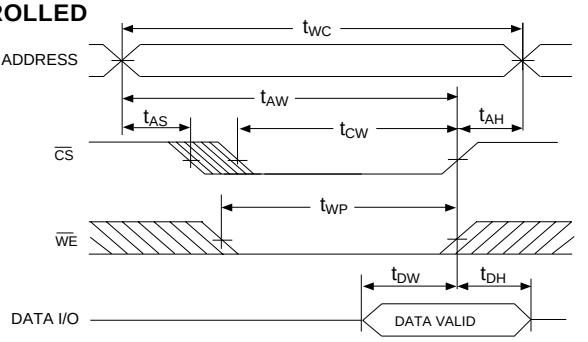
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

FIG. 5
WRITE CYCLE - $\overline{WE}$ CONTROLLED



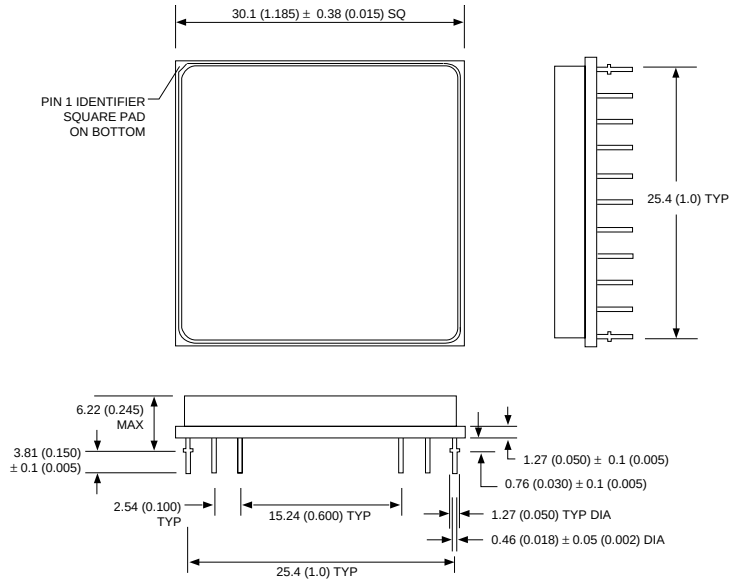
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

FIG. 6
WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

PACKAGE 401: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H)



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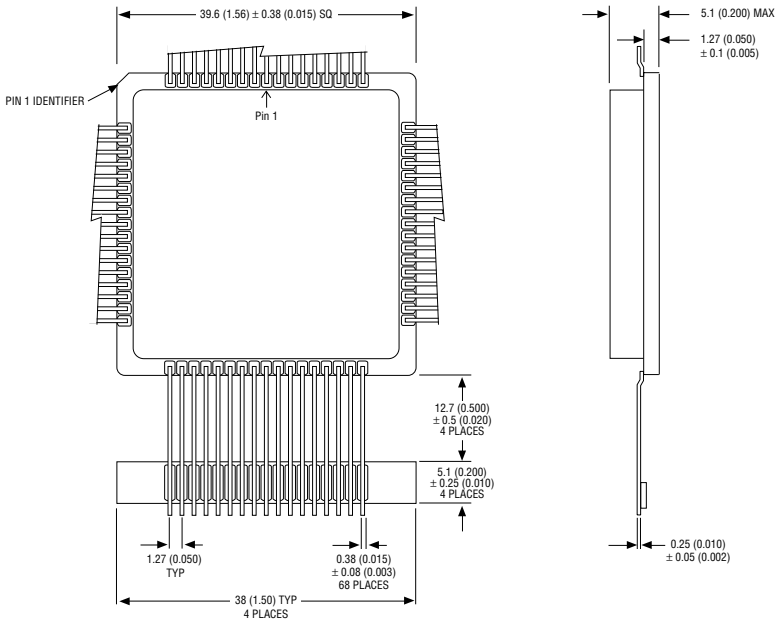
PACKAGE 501: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4)



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ORDERING INFORMATION