

SED1565 Series

Dot Matrix LCD Driver

■ DESCRIPTION

The SED1565 Series is a series of single-chip dot matrix liquid crystal display drivers that can be connected directly to a microprocessor bus. 8-bit parallel or serial display data sent from the microprocessor is stored in the internal display data RAM and the chip generates a liquid crystal drive signal independent of the microprocessor. Because the chips in the SED1565 Series contain 65×132 bits of display data RAM and there is a 1-to-1 correspondence between the liquid crystal panel pixels and the internal RAM bits, these chips enable displays with a high degree of freedom.

The SED1565 Series chips contain 65 common output circuits and 132 segment output circuits, so that a single chip can drive a 65×132 dot display (capable of displaying 8 columns \times 4 rows of a 16×16 dot kanji font). The SED1567 Series chips contain 33 common output circuits and 132 segment output circuits, so that a single chip can drive 33×132 dot display (capable of displaying 8 columns \times 2 rows of 16×16 dot kanji fonts). Moreover, the capacity of the display can be extended through the use of master/slave structures between chips.

The chips are able to minimize power consumption because no external operating clock is necessary for the display data RAM read/write operation. Furthermore, because each chip is equipped internally with a low-power liquid crystal driver power supply, resistors for liquid crystal driver power voltage adjustment and a display clock CR oscillator circuit, the SED1565 Series chips can be used to create the lowest power display system with the fewest components for high-performance portable devices.

■ FEATURES

- Direct display of RAM data through the display data RAM.
RAM bit data: "1" Non-illuminated
"0" Illuminated
(during normal display)
- RAM capacity
 $65 \times 132 = 8580$ bits
- Display driver circuits
SED1565***: 65 common output and 132 segment outputs
SED1566***: 49 common output and 132 segment outputs
SED1567***: 33 common outputs and 132 segment outputs
SED1568***: 55 common outputs and 132 segment outputs
SED1569***: 53 common outputs and 132 segment outputs
- High-speed 8-bit MPU interface (The chip can be connected directly to the both the 80 \times 86 series MPUs and the 68000 series MPUs)
/Serial interfaces are supported.
- Abundant command functions
- Display data Read/Write, display ON/OFF, Normal/Reverse display mode, page address set, display start line set, column address set, status read, display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction select, power saver, static indicator, common output status select, V₅ voltage regulation internal resistor ratio set.
- Static drive circuit equipped internally for indicators. (1 system, with variable flashing speed.)
- Low-power liquid crystal display power supply circuit equipped internally.
Booster circuit (with Boost ratios of Double/Triple/Quad, where the step-up voltage reference power supply can be input externally)
High-accuracy voltage adjustment circuit (Thermal gradient $-0.05\%/^{\circ}\text{C}$ or $-0.2\%/^{\circ}\text{C}$ or external input)
V₅ voltage regulator resistors equipped internally, V₁ to V₄ voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.
- CR oscillator circuit equipped internally (external clock can also be input)

SED1565 Series

- Extremely low power consumption
Operating power when the built-in power supply is used (an example)
SED1565D0B 81 μ A ($V_{DD} - V_{SS} = V_{DD} - V_{SS2} =$
/SED1565DBB 3.0 V, Quad voltage, $V_5 - V_{DD} =$
-11.0 V)
SED1566D0B 43 μ A ($V_{DD} - V_{SS} = V_{DD} - V_{SS2} =$
/SED1566DBB 3.0 V, Triple voltage, $V_5 - V_{DD} =$
-8.0 V)
SED1567D0B 29 μ A ($V_{DD} - V_{SS} = V_{DD} - V_{SS2} =$
/SED1567DBB 3.0 V, Triple voltage, $V_5 - V_{DD} =$
-8.0 V)
SED1568D0B 46 μ A ($V_{DD} - V_{SS} = V_{DD} - V_{SS2} =$
/SED1568DBB 3.0 V, Triple voltage, $V_5 - V_{DD} =$
/SED1569D0B -8.0 V)
/SED1569DBB
Conditions: When all displays are in white and the
normal mode is selected.

- Power supply
Operable on the low 1.8 voltage
Logic power supply $V_{DD} - V_{SS} = 1.8$ V to -5.5 V
Boost reference voltage: $V_{DD} - V_{SS2} = 1.8$ V to
-6.0 V
Liquid crystal drive power supply: $V_{DD} - V_5 = -4.5$
V to -16.0 V
- Wide range of operating temperatures: -40 to
85°C
- CMOS process
- Shipping forms include bare chip and TCP.
- These chips not designed for resistance to light or
resistance to radiation.

■ SERIES SPECIFICATIONS

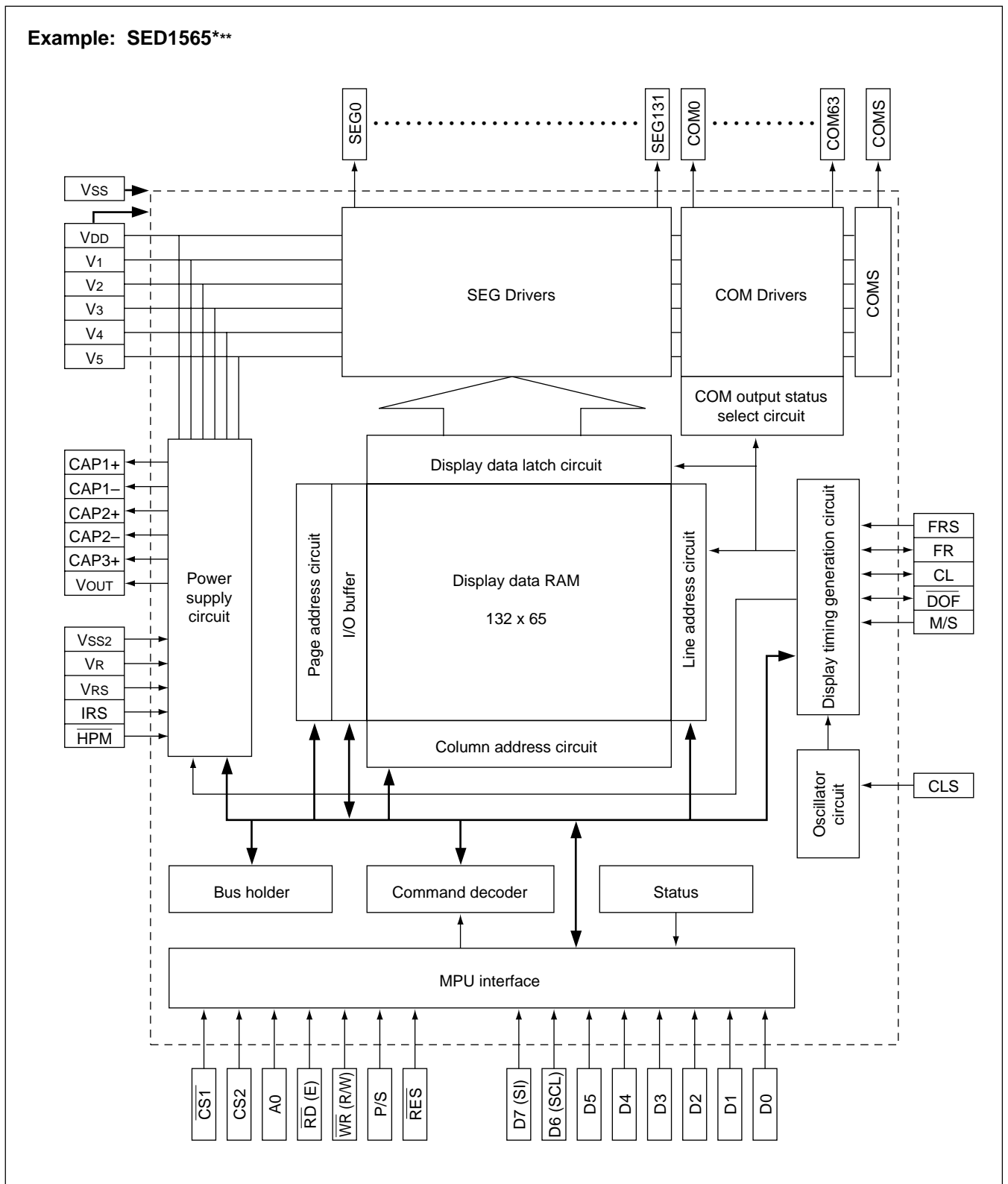
Product Name	Duty	Bias	SED Dr	COM Dr	VREG Temperature Gradient	Shipping Forms
SED1565D0B /SED1565DBB	1/65	1/9, 1/7	132	65	-0.05%/°C	Bare Chip
SED1565T0*	1/65	1/9, 1/7	132	65	-0.05%/°C	TCP
* SED1565D1B	1/65	1/9, 1/7	132	65	-0.2%/°C	Bare Chip
* SED1565T1*	1/65	1/9, 1/7	132	65	-0.2%/°C	TCP
SED1565D2B	1/65	1/9, 1/7	132	65	External Input	Bare Chip
SED1565T2*	1/65	1/9, 1/7	132	65	External Input	TCP
SED1566D0B /SED1566DBB	1/49	1/8, 1/6	132	49	-0.05%/°C	Bare Chip
SED1566T0*	1/49	1/8, 1/6	132	49	-0.05%/°C	TCP
SED1566D1B	1/49	1/8, 1/6	132	49	-0.2%/°C	Bare Chip
* SED1566T1*	1/49	1/8, 1/6	132	49	-0.2%/°C	TCP
SED1566D2B	1/49	1/8, 1/6	132	49	External Input	Bare Chip
* SED1566T2*	1/49	1/8, 1/6	132	49	External Input	TCP
SED1567D0B /SED1567DBB	1/33	1/6, 1/5	132	33	-0.05%/°C	Bare Chip
SED1567T0*	1/33	1/6, 1/5	132	33	-0.05%/°C	TCP
SED1567D1B	1/33	1/6, 1/5	132	33	-0.2%/°C	Bare Chip
* SED1567T1*	1/33	1/6, 1/5	132	33	-0.2%/°C	TCP
SED1567D2B	1/33	1/6, 1/5	132	33	External Input	Bare Chip
* SED1567T2*	1/33	1/6, 1/5	132	33	External Input	TCP
SED1568D0B /SED1568DBB	1/55	1/8, 1/6	132	55	-0.05%/°C	Bare Chip
SED1569D0B /SED1569DBB	1/53	1/8, 1/6	132	53	-0.05%/°C	Bare Chip
SED1569T0*	1/53	1/8, 1/6	132	53	-0.05%/°C	TCP

Note: The circuit for the VREG temperature gradient -0.2%/°C and the external input is under preparation.

* : Under development

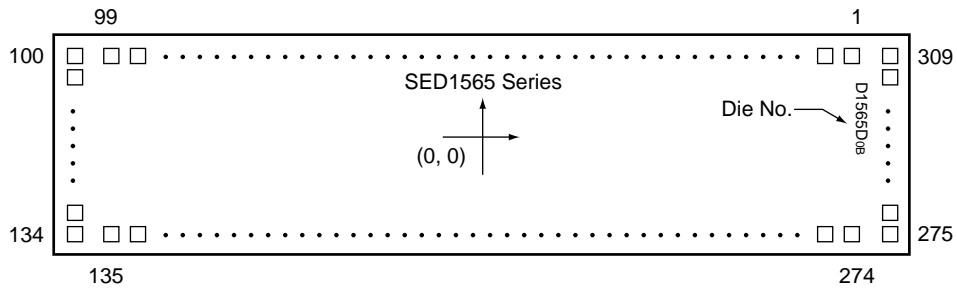
■ BLOCK DIAGRAM

Example: SED1565***



SED1565 Series

■ PAD LAYOUT



Chip Size	10.82 mm × 2.81 mm	
Bump Pitch	71 μm (Min.)	
Bump Size	PAD #1~24	85 μm × 85 μm
	PAD #25~82	64 μm × 85 μm
	PAD #83~99	85 μm × 85 μm
	PAD #100	85 μm × 73 μm
	PAD #101~133	85 μm × 47 μm
	PAD #134	85 μm × 73 μm
	PAD #135	73 μm × 85 μm
	PAD #136~273	47 μm × 85 μm
	PAD #274	73 μm × 85 μm
	PAD #275	86 μm × 73 μm
	PAD #276~308	85 μm × 47 μm
	PAD #309	85 μm × 73 μm
	Bump Height	17 μm (Typ.)

■ PIN DESCRIPTIONS

● Power Supply Pins

Pin Name	I/O	Function	# of Pins																																													
VDD	Power Supply	Shared with the MPU power supply terminal Vcc.	13																																													
VSS	Power Supply	This is a 0 V terminal connected to the system GND.	9																																													
VSS2	Power Supply	This is the reference power supply for the step-up voltage circuit for the liquid crystal drive.	4																																													
VRS	Power Supply	This is the externally-input VREG power supply for the LCD power supply voltage regulator. These are only enabled for the models with the VREG external input option.	2																																													
V1, V2, V3, V4, V5	Power Supply	This is a multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on V _{DD} , and must maintain the relative magnitudes shown below. $V_{DD} (= V_0) \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ <p>Master operation: When the power supply turns ON, the internal power supply circuits produce the V₁ to V₄ voltages shown below. The voltage settings are selected using the LCD bias set command.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th colspan="2">SED1565***</th> <th colspan="2">SED1566***</th> <th colspan="2">SED1567***</th> <th colspan="2">SED1569***</th> </tr> </thead> <tbody> <tr> <td>V1</td> <td>1/9 • V₅</td> <td>1/7 • V₅</td> <td>1/8 • V₅</td> <td>1/6 • V₅</td> <td>1/6 • V₅</td> <td>1/5 • V₅</td> <td>1/8 • V₅</td> <td>1/6 • V₅</td> </tr> <tr> <td>V2</td> <td>2/9 • V₅</td> <td>2/7 • V₅</td> <td>2/8 • V₅</td> <td>2/6 • V₅</td> <td>2/6 • V₅</td> <td>2/5 • V₅</td> <td>2/8 • V₅</td> <td>2/6 • V₅</td> </tr> <tr> <td>V3</td> <td>7/9 • V₅</td> <td>5/7 • V₅</td> <td>6/8 • V₅</td> <td>4/6 • V₅</td> <td>4/6 • V₅</td> <td>3/5 • V₅</td> <td>6/8 • V₅</td> <td>4/6 • V₅</td> </tr> <tr> <td>V4</td> <td>8/9 • V₅</td> <td>6/7 • V₅</td> <td>7/6 • V₅</td> <td>5/6 • V₅</td> <td>5/6 • V₅</td> <td>4/5 • V₅</td> <td>7/8 • V₅</td> <td>5/6 • V₅</td> </tr> </tbody> </table>		SED1565***		SED1566***		SED1567***		SED1569***		V1	1/9 • V ₅	1/7 • V ₅	1/8 • V ₅	1/6 • V ₅	1/6 • V ₅	1/5 • V ₅	1/8 • V ₅	1/6 • V ₅	V2	2/9 • V ₅	2/7 • V ₅	2/8 • V ₅	2/6 • V ₅	2/6 • V ₅	2/5 • V ₅	2/8 • V ₅	2/6 • V ₅	V3	7/9 • V ₅	5/7 • V ₅	6/8 • V ₅	4/6 • V ₅	4/6 • V ₅	3/5 • V ₅	6/8 • V ₅	4/6 • V ₅	V4	8/9 • V ₅	6/7 • V ₅	7/6 • V ₅	5/6 • V ₅	5/6 • V ₅	4/5 • V ₅	7/8 • V ₅	5/6 • V ₅	10
	SED1565***		SED1566***		SED1567***		SED1569***																																									
V1	1/9 • V ₅	1/7 • V ₅	1/8 • V ₅	1/6 • V ₅	1/6 • V ₅	1/5 • V ₅	1/8 • V ₅	1/6 • V ₅																																								
V2	2/9 • V ₅	2/7 • V ₅	2/8 • V ₅	2/6 • V ₅	2/6 • V ₅	2/5 • V ₅	2/8 • V ₅	2/6 • V ₅																																								
V3	7/9 • V ₅	5/7 • V ₅	6/8 • V ₅	4/6 • V ₅	4/6 • V ₅	3/5 • V ₅	6/8 • V ₅	4/6 • V ₅																																								
V4	8/9 • V ₅	6/7 • V ₅	7/6 • V ₅	5/6 • V ₅	5/6 • V ₅	4/5 • V ₅	7/8 • V ₅	5/6 • V ₅																																								

● LCD Power Supply Circuit Pins

Pin Name	I/O	Function	# of Pins
CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1-terminal.	2
CAP1-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.	2
CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2-terminal.	2
CAP2-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.	2
CAP3-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.	2
VOUT	O	DC/DC voltage converter. Connect a capacitor between this terminal and Vss.	2
VR	I	Output voltage regulator terminal. Provides the voltage between V _{DD} and V ₅ through a resistive voltage divider. These are only enabled when the V ₅ voltage regulator internal resistors are not used (IRS = "L"). These cannot be used when the V ₅ voltage regulator internal resistors are used (IRS = "H").	2

SED1565 Series

● System Bus Connection Terminals

Pin Name	I/O	Function	# of Pins														
D7 to D0 (SI) (SCL)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S = "L"), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance.	8														
A0	I	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.	1														
$\overline{\text{RES}}$	I	When $\overline{\text{RES}}$ is set to "L," the settings are initialized. The reset operation is performed by the $\overline{\text{RES}}$ signal level.	1														
$\overline{\text{CS1}}$ $\overline{\text{CS2}}$	I	This is the chip select signal. When $\overline{\text{CS1}}$ = "L" and $\overline{\text{CS2}}$ = "H," then the chip select becomes active, and data/command I/O is enabled.	2														
$\overline{\text{RD}}$ (E)	I	<ul style="list-style-type: none"> When connected to an 8080 MPU, this is active LOW. This pin is connected to the $\overline{\text{RD}}$ signal of the 8080 MPU, and the SED1565 series data bus is in an output status when this signal is "L". When connected to a 6800 Series MPU, this is active HIGH. This is the 68000 Series MPU enable clock input terminal. 	1														
$\overline{\text{WR}}$ ($\overline{\text{R/W}}$)	I	<ul style="list-style-type: none"> When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU $\overline{\text{WR}}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{\text{WR}}$ signal. When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When $\overline{\text{R/W}}$ = "H": Read. When $\overline{\text{R/W}}$ = "L": Write. 	1														
C86	I	This is the MPU interface switch terminal. C86 = "H": 6800 Series MPU interface. C86 = "L": 8080 MPU interface.	1														
P/S	I	This is the parallel data input/serial data input switch terminal. P/S = "H": Parallel data input. P/S = "L": Serial data input. The following applies depending on the P/S status: <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>P/S</th> <th>Data/Command</th> <th>Data</th> <th>Read/Write</th> <th>Serial Clock</th> </tr> </thead> <tbody> <tr> <td>"H"</td> <td>A0</td> <td>D0 to D7</td> <td>$\overline{\text{RD}}$, $\overline{\text{WR}}$</td> <td rowspan="2">SCL (D6)</td> </tr> <tr> <td>"L"</td> <td>A0</td> <td>SI (D7)</td> <td>Write only</td> </tr> </tbody> </table> When P/S = "L", D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open. $\overline{\text{RD}}$ (E) and $\overline{\text{WR}}$ ($\overline{\text{P/W}}$) are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported.	P/S	Data/Command	Data	Read/Write	Serial Clock	"H"	A0	D0 to D7	$\overline{\text{RD}}$, $\overline{\text{WR}}$	SCL (D6)	"L"	A0	SI (D7)	Write only	1
P/S	Data/Command	Data	Read/Write	Serial Clock													
"H"	A0	D0 to D7	$\overline{\text{RD}}$, $\overline{\text{WR}}$	SCL (D6)													
"L"	A0	SI (D7)	Write only														
CLS	I	Terminal to select whether or enable or disable the display clock internal oscillator circuit. CLS = "H": Internal oscillator circuit is enabled CLS = "L": Internal oscillator circuit is disabled (requires external input) When CLS = "L", input the display clock through the CL terminal.	1														

SED1565 Series

Pin Name	I/O	Function	# of Pins																																								
M/S	I	<p>This terminal selects the master/slave operation for the SED1565 Series chips. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals required for the liquid crystal display, synchronizing the liquid crystal display system.</p> <p>M/S = "H": Master operation M/S = "L": Slave operation</p> <p>The following is true depending on the M/S and CLS status:</p> <table border="1"> <thead> <tr> <th>M/S</th> <th>CLS</th> <th>Oscillator Circuit</th> <th>Power Supply Circuit</th> <th>CL</th> <th>FR</th> <th>FRS</th> <th>DOF</th> </tr> </thead> <tbody> <tr> <td>"H"</td> <td>"H"</td> <td>Enabled</td> <td>Enabled</td> <td>Output</td> <td>Output</td> <td>Output</td> <td>Output</td> </tr> <tr> <td>"H"</td> <td>"L"</td> <td>Disabled</td> <td>Enabled</td> <td>Input</td> <td>Output</td> <td>Output</td> <td>Output</td> </tr> <tr> <td>"L"</td> <td>"H"</td> <td>Disabled</td> <td>Disabled</td> <td>Input</td> <td>Input</td> <td>Output</td> <td>Input</td> </tr> <tr> <td>"L"</td> <td>"L"</td> <td>Disabled</td> <td>Disabled</td> <td>Input</td> <td>Input</td> <td>Output</td> <td>Input</td> </tr> </tbody> </table>	M/S	CLS	Oscillator Circuit	Power Supply Circuit	CL	FR	FRS	DOF	"H"	"H"	Enabled	Enabled	Output	Output	Output	Output	"H"	"L"	Disabled	Enabled	Input	Output	Output	Output	"L"	"H"	Disabled	Disabled	Input	Input	Output	Input	"L"	"L"	Disabled	Disabled	Input	Input	Output	Input	1
M/S	CLS	Oscillator Circuit	Power Supply Circuit	CL	FR	FRS	DOF																																				
"H"	"H"	Enabled	Enabled	Output	Output	Output	Output																																				
"H"	"L"	Disabled	Enabled	Input	Output	Output	Output																																				
"L"	"H"	Disabled	Disabled	Input	Input	Output	Input																																				
"L"	"L"	Disabled	Disabled	Input	Input	Output	Input																																				
CL	I/O	<p>This is the display clock input terminal</p> <p>The following is true depending on the M/S and CLS status.</p> <table border="1"> <thead> <tr> <th>M/S</th> <th>CLS</th> <th>CL</th> </tr> </thead> <tbody> <tr> <td>"H"</td> <td>"H"</td> <td>Output</td> </tr> <tr> <td>"H"</td> <td>"L"</td> <td>Input</td> </tr> <tr> <td>"L"</td> <td>"H"</td> <td>Input</td> </tr> <tr> <td>"L"</td> <td>"L"</td> <td>Input</td> </tr> </tbody> </table> <p>When the SED1565 Series chips are used in master/slave mode, the various CL terminals must be connected.</p>	M/S	CLS	CL	"H"	"H"	Output	"H"	"L"	Input	"L"	"H"	Input	"L"	"L"	Input	1																									
M/S	CLS	CL																																									
"H"	"H"	Output																																									
"H"	"L"	Input																																									
"L"	"H"	Input																																									
"L"	"L"	Input																																									
FR	I/O	<p>This is the liquid crystal alternating current signal I/O terminal.</p> <p>M/S = "H": Output M/S = "L": Input</p> <p>When the SED1565 Series chip is used in master/slave mode, the various FR terminals must be connected.</p>	1																																								
DOF	I/O	<p>This is the liquid crystal display blanking control terminal.</p> <p>M/S = "H": Output M/S = "L": Input</p> <p>When the SED1565 Series chip is used in master/slave mode, the various $\overline{\text{DOF}}$ terminals must be connected.</p>	1																																								
FRS	O	<p>This is the output terminal for the static drive.</p> <p>This terminal is only enabled when the static indicator display is ON when in master operation mode, and is used in conjunction with the FR terminal.</p>	1																																								
IRS	I	<p>This terminal selects the resistors for the V5 voltage level adjustment.</p> <p>IRS = "H": Use the internal resistors IRS = "L": Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal.</p> <p>This pin is enabled only when the master operation mode is selected. It is fixed to either "H" or "L" when the slave operation mode is selected.</p>	1																																								
HPM	I	<p>This is the power control terminal for the power supply circuit for liquid crystal drive.</p> <p>HPM = "H": Normal mode HPM = "L": High power mode</p> <p>This pin is enabled only when the master operation mode is selected. It is fixed to either "H" or "L" when the slave operation mode is selected.</p>	1																																								

SED1565 Series

● Liquid Crystal Drive Pins

Pin Name	I/O	Function	# of Pins																																										
SEG0 to SEG131	O	<p>These are the liquid crystal segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal, a single level is selected from VDD, V2, V3, and V5.</p> <table border="1"> <thead> <tr> <th>RAM DATA</th> <th>FR</th> <th colspan="2">Output Voltage</th> </tr> <tr> <td></td> <td></td> <th>Normal Display</th> <th>Reverse Display</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>VDD</td> <td>V2</td> </tr> <tr> <td>H</td> <td>L</td> <td>V5</td> <td>V3</td> </tr> <tr> <td>L</td> <td>H</td> <td>V2</td> <td>VDD</td> </tr> <tr> <td>L</td> <td>L</td> <td>V3</td> <td>V5</td> </tr> <tr> <td>Power save</td> <td>—</td> <td colspan="2">VDD</td> </tr> </tbody> </table>	RAM DATA	FR	Output Voltage				Normal Display	Reverse Display	H	H	VDD	V2	H	L	V5	V3	L	H	V2	VDD	L	L	V3	V5	Power save	—	VDD		132														
RAM DATA	FR	Output Voltage																																											
		Normal Display	Reverse Display																																										
H	H	VDD	V2																																										
H	L	V5	V3																																										
L	H	V2	VDD																																										
L	L	V3	V5																																										
Power save	—	VDD																																											
COM0 to COM31	O	<p>These are the liquid crystal common drive outputs.</p> <table border="1"> <thead> <tr> <th>Part No.</th> <th>COM</th> <th>Part No.</th> <th></th> </tr> </thead> <tbody> <tr> <td>SED1565***</td> <td>COM 0 to COM 63</td> <td>SED1565***</td> <td>64</td> </tr> <tr> <td>SED1566***</td> <td>COM 0 to COM 47</td> <td>SED1566***</td> <td>48</td> </tr> <tr> <td>SED1567***</td> <td>COM 0 to COM 31</td> <td>SED1567***</td> <td>32</td> </tr> <tr> <td>SED1568***</td> <td>COM 0 to COM 53</td> <td>SED1568***</td> <td>54</td> </tr> <tr> <td>SED1569***</td> <td>COM 0 to COM 51</td> <td>SED1569***</td> <td>52</td> </tr> </tbody> </table> <p>Through a combination of the contents of the scan data and with the FR signal, a single level is selected from VDD, V1, V4, and V5.</p> <table border="1"> <thead> <tr> <th>Scan Data</th> <th>FR</th> <th>Output Voltage</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>V5</td> </tr> <tr> <td>H</td> <td>L</td> <td>VDD</td> </tr> <tr> <td>L</td> <td>H</td> <td>V1</td> </tr> <tr> <td>L</td> <td>L</td> <td>V4</td> </tr> <tr> <td>Power Save</td> <td>—</td> <td>VDD</td> </tr> </tbody> </table>	Part No.	COM	Part No.		SED1565***	COM 0 to COM 63	SED1565***	64	SED1566***	COM 0 to COM 47	SED1566***	48	SED1567***	COM 0 to COM 31	SED1567***	32	SED1568***	COM 0 to COM 53	SED1568***	54	SED1569***	COM 0 to COM 51	SED1569***	52	Scan Data	FR	Output Voltage	H	H	V5	H	L	VDD	L	H	V1	L	L	V4	Power Save	—	VDD	64
Part No.	COM	Part No.																																											
SED1565***	COM 0 to COM 63	SED1565***	64																																										
SED1566***	COM 0 to COM 47	SED1566***	48																																										
SED1567***	COM 0 to COM 31	SED1567***	32																																										
SED1568***	COM 0 to COM 53	SED1568***	54																																										
SED1569***	COM 0 to COM 51	SED1569***	52																																										
Scan Data	FR	Output Voltage																																											
H	H	V5																																											
H	L	VDD																																											
L	H	V1																																											
L	L	V4																																											
Power Save	—	VDD																																											
COMS	O	<p>These are the COM output terminals for the indicator. Both terminals output the same signal. Leave these open if they are not used. When in master/slave mode, the same signal is output by both master and slave.</p>	2																																										

● Test Terminals

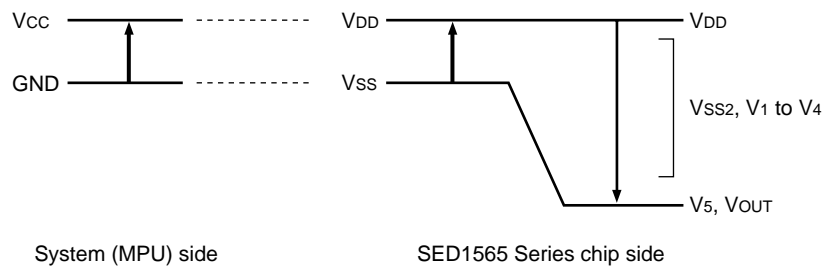
Pin Name	I/O	Function	No. of Pins
TEST0 to 9	I/O	These are terminals for IC chip testing. They are set to OPEN.	14

Total: 288 pins for the SED1565***.
 272 pins for the SED1566***.
 256 pins for the SED1567***.
 276 pins for the SED1569***.

■ ABSOLUTE MAXIMUM RATINGS

Unless otherwise noted, $V_{SS} = 0\text{ V}$

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		V_{DD}	-0.3 to +7.0	V
Power supply voltage (2) (V_{DD} standard)	With Triple step-up	V_{SS2}	-7.0 to +0.3	V
	With Quad step-up		-6.0 to +0.3 -4.5 to +0.3	
Power supply voltage (3) (V_{DD} standard)		V_5, V_{OUT}	-18.0 to +0.3	V
Power supply voltage (4) (V_{DD} standard)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	-0.3 to $V_{DD} + 0.3$	V
Output voltage		V_O	-0.3 to $V_{DD} + 0.3$	V
Operating temperature		T_{OPR}	-40 to +85	°C
Storage temperature	TCP	T_{STR}	-55 to +100	°C
	Bare chip		-55 to +125	



Notes and Cautions

1. The V_{SS2} , V_1 to V_5 and V_{OUT} are relative to the $V_{DD} = 0\text{ V}$ reference.
2. Insure that the voltage levels of V_1 , V_2 , V_3 , and V_4 are always such that $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

SED1565 Series

DC CHARACTERISTICS

Unless otherwise specified, VSS = 0 V, VDD = 3.0 V ± 10%, Ta = -40 to 85°C

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage (1)	Recommended Voltage	VDD			2.7	—	3.3	V	VDD*1
	Possible Operating Voltage				1.8	—	5.5	V	VDD*1
Operating Voltage (2)	Recommended Voltage	VSS2	(Relative to VDD)		-3.3	—	-2.7	V	VSS2
	Possible Operating Voltage	VSS2	(Relative to VDD)		-6.0	—	-1.8	V	VSS2
Operating Voltage (3)	Possible Operating Voltage	V5	(Relative to VDD)		-16.0	—	-4.5	V	V5 *2
	Possible Operating Voltage	V1, V2	(Relative to VDD)		0.4 × V5	—	VDD	V	V1, V2
	Possible Operating Voltage	V3, V4	(Relative to VDD)		V5	—	0.6 × V5	V	V3, V4
High-level Input Voltage		VIHC			0.8 × VDD	—	VDD	V	*3
Low-level Input Voltage		VILC			VSS	—	0.2 × VDD	V	*3
High-level Output Voltage		VOHC	IOH = -0.5 mA		0.8 × VDD	—	VDD	V	*4
Low-level Output Voltage		VOLC	IOL = 0.5 mA		VSS	—	0.2 × VDD	V	*4
Input leakage current		ILI	VIN = VDD or VSS		-1.0	—	1.0	µA	*5
Output leakage current		ILO			-3.0	—	3.0	µA	*6
Liquid Crystal Driver ON Resistance		RON	Ta = 25°C (Relative To VDD)	V5 = -14.0 V	—	2.0	3.5	KΩ	SEgN
				V5 = -8.0 V	—	3.2	5.4	KΩ	COMn *7
Static Consumption Current		ISSQ			—	0.01	5	µA	VSS, VSS2
Output Leakage Current		I5Q	V5 = -18.0 V (Relative To VDD)		—	0.01	15	µA	V5
Input Terminal Capacitance		CIN	Ta = 25°C f = 1 MHz		—	5.0	8.0	pF	
Oscillator Frequency	Internal Oscillator	fOSC	Ta = 25°C		18	22	26	kHz	*8
		fCL	SED1565***/1567**		18	22	26	kHz	CL
	External Input	fOSC	Ta = 25°C		27	33	39	kHz	*8
		fCL	SED1566***/1569**		14	17	20	kHz	CL
Internal Power	Input voltage		VSS2	With Triple (Relative To VDD)	-6.0	—	-1.8	V	VSS2
			VSS2	With Quad (Relative To VDD)	-4.5	—	-1.8	V	VSS2
	Supply Step-up output voltage Circuit		VOUT	(Relative to VDD)	-18.0	—	—	V	VOUT
	Voltage regulator Circuit Operating Voltage		VOUT	(Relative to VDD)	-18.0	—	-6.0	V	VOUT
	Voltage Follower Circuit Operating Voltage		V5	(Relative to VDD)	-16.0	—	-4.5	V	V5 *9
Base Voltage		VREG0 VREG1	Ta = 25°C (Relative to VDD)	-0.05%/°C	-2.16	-2.10	-2.04	V	*10
				-0.2%/°C	-5.15	-4.9	-4.65	V	*10

SED1565 Series

- Dynamic Consumption Current (1), During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used.

Display Pattern OFF

Ta = 25°C

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
SED1565***	IDD (1)	VDD = 5.0 V, V5 - VDD = -11.0 V	—	18	30	μA	*11
		VDD = 3.0 V, V5 - VDD = -11.0 V	—	16	27		
SED1566***		VDD = 3.0 V, V5 - VDD = -11.0 V	—	13	22		
		VDD = 5.0 V, V5 - VDD = -8.0 V	—	11	19		
SED1567***		VDD = 3.0 V, V5 - VDD = -8.0 V	—	9	15		
		VDD = 5.0 V, V5 - VDD = -8.0 V	—	8	13		
SED1568***/SED1569***		VDD = 3.0 V, V5 - VDD = -8.0 V	—	7	12		
		VDD = 5.0 V, V5 - VDD = -8.0 V	—	12	20		
		VDD = 3.0 V, V5 - VDD = -8.0 V	—	10	17		

Display Pattern Checker

Ta = 25°C

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
SED1565***	IDD (1)	VDD = 5.0 V, V5 - VDD = -11.0 V	—	23	38	μA	*11
		VDD = 3.0 V, V5 - VDD = -11.0 V	—	21	35		
SED1566***		VDD = 3.0 V, V5 - VDD = -11.0 V	—	17	29		
		VDD = 5.0 V, V5 - VDD = -8.0 V	—	14	24		
SED1567***		VDD = 3.0 V, V5 - VDD = -8.0 V	—	12	20		
		VDD = 5.0 V, V5 - VDD = -8.0 V	—	11	18		
SED1568***/SED1569***		VDD = 3.0 V, V5 - VDD = -8.0 V	—	10	17		
		VDD = 5.0 V, V5 - VDD = -8.0 V	—	15	25		
		VDD = 3.0 V, V5 - VDD = -8.0 V	—	13	22		

- Dynamic Consumption Current (2), During Display, with the Internal Power Supply ON

Display Pattern OFF

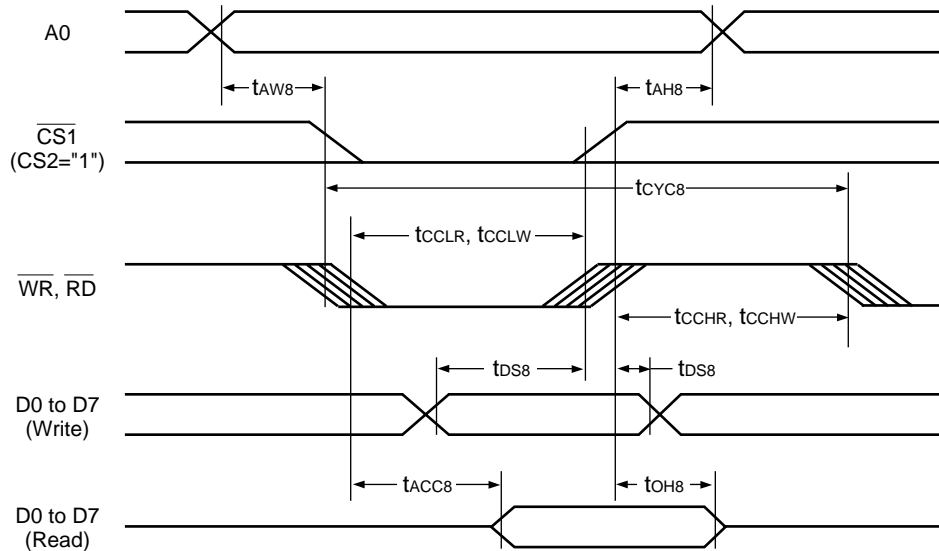
Ta = 25°C

Item	Symbol	Condition	Rating			Units	Notes	
			Min.	Typ.	Max.			
SED1565***	IDD (2)	VDD = 5.0 V, Triple step-up voltage. V5 - VDD = -11.0 V	Normal Mode	—	67	112	μA	*12
			High-Power Mode	—	114	190		
		VDD = 3.0 V, Quad step-up voltage. V5 - VDD = -11.0 V	Normal Mode	—	81	135		
			High-Power Mode	—	138	230		
SED1566***		VDD = 5.0 V, Double step-up voltage. V5 - VDD = -8.0 V	Normal Mode	—	35	59		
			High-Power Mode	—	64	107		
		VDD = 3.0 V, Triple step-up voltage. V5 - VDD = -8.0 V	Normal Mode	—	43	72		
			High-Power Mode	—	84	140		
SED1567***	VDD = 3.0 V, Quad step-up voltage. V5 - VDD = -11.0 V	Normal Mode	—	72	121			
		High-Power Mode	—	128	214			
	VDD = 5.0 V, Double step-up voltage. V5 - VDD = -8.0 V	Normal Mode	—	26	44			
		High-Power Mode	—	60	100			
SED1568***/ SED1569***	VDD = 3.0 V, Triple step-up voltage. V5 - VDD = -8.0 V	Normal Mode	—	29	49			
		High-Power Mode	—	73	122			
	VDD = 5.0 V, Double step-up voltage. V5 - VDD = -8.0 V	Normal Mode	—	37	62			
		High-Power Mode	—	67	112			
		VDD = 3.0 V, Triple step-up voltage. V5 - VDD = -8.0 V	Normal Mode	—	46	77		
			High-Power Mode	—	87	145		

SED1565 Series

■ TIMING CHARACTERISTICS

● System Bus Read/Write Characteristics 1 (for the 8080 Series MPU)



(V_{DD} = 4.5 V to 5.5 V, T_a = -40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t _{AH8}	—	0	—	ns
Address setup time	A0	t _{AW8}	—	0	—	ns
System cycle time	A0	t _{CYC8}	—	166	—	ns
Control L pulse width (\overline{WR})	\overline{WR}	t _{CCLW}	—	30	—	ns
Control L pulse width (\overline{RD})	\overline{RD}	t _{CCLR}	—	70	—	ns
Control H pulse width (\overline{WR})	\overline{WR}	t _{CCHW}	—	30	—	ns
Control H pulse width (\overline{RD})	\overline{RD}	t _{CCHR}	—	30	—	ns
Data setup time	D0 to D7	t _{DS8}	—	30	—	ns
Address hold time		t _{DH8}	—	10	—	ns
\overline{RD} access time	D0 to D7	t _{ACC8}	CL = 100 pF	—	70	ns
Output disable time		t _{OH8}	—	5	50	ns

(V_{DD} = 2.7 V to 4.5 V, T_a = -40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t _{AH8}	—	0	—	ns
Address setup time	A0	t _{AW8}	—	0	—	ns
System cycle time	A0	t _{CYC8}	—	300	—	ns
Control L pulse width (\overline{WR})	\overline{WR}	t _{CCLW}	—	60	—	ns
Control L pulse width (\overline{RD})	\overline{RD}	t _{CCLR}	—	120	—	ns
Control H pulse width (\overline{WR})	\overline{WR}	t _{CCHW}	—	60	—	ns
Control H pulse width (\overline{RD})	\overline{RD}	t _{CCHR}	—	60	—	ns
Data setup time	D0 to D7	t _{DS8}	—	40	—	ns
Address hold time		t _{DH8}	—	15	—	ns
\overline{RD} access time	D0 to D7	t _{ACC8}	CL = 100 pF	—	140	ns
Output disable time		t _{OH8}	—	10	100	ns

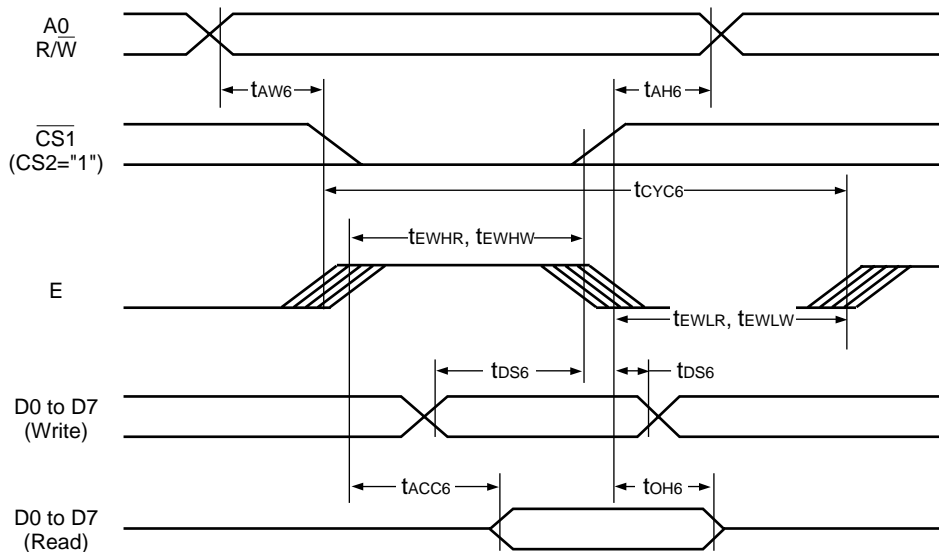
SED1565 Series

(VDD = 1.8 V to 2.7 V, Ta = -40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t _{AH8}	—	0	—	ns
Address setup time	A0	t _{AW8}	—	0	—	ns
System cycle time	A0	t _{CYC8}	—	1000	—	ns
Control L pulse width (\overline{WR})	\overline{WR}	t _{CCLW}	—	120	—	ns
Control L pulse width (\overline{RD})	\overline{RD}	t _{CCLR}	—	240	—	ns
Control H pulse width (\overline{WR})	\overline{WR}	t _{CCHW}	—	120	—	ns
Control H pulse width (\overline{RD})	\overline{RD}	t _{CCHR}	—	120	—	ns
Data setup time	D0 to D7	t _{DS8}	—	80	—	ns
Address hold time		t _{DH8}	—	30	—	ns
\overline{RD} access time		t _{ACC8}	CL = 100 pF	—	280	ns
Output disable time		t _{OH8}	—	10	200	ns

- *1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, (t_r + t_f) ≤ (t_{CYC8} - t_{CCLW} - t_{CCHW}) for (t_r + t_f) ≤ (t_{CYC8} - t_{CCLR} - t_{CCHR}) are specified.
- *2 All timing is specified using 20% and 80% of VDD as the reference.
- *3 t_{CCLW} and t_{CCLR} are specified as the overlap between CS1 being "L" (CS2 = "H") and \overline{WR} and \overline{RD} being at the "L" level.

● System Bus Read/Write Characteristics 2 (6800 Series MPU)



SED1565 Series

(V_{DD} = 4.5 V to 5.5 V, T_a = -40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t _{AH6}	—	0	—	ns
Address setup time		t _{AW6}	—	0	—	ns
System cycle time	A0	t _{CYC6}	—	166	—	ns
Data setup time	D0 to D7	t _{DS6}	—	30	—	ns
Data hold time		t _{DH6}	—	10	—	ns
Access time		t _{ACC6}	CL = 100 pF	—	70	ns
Output disable time		t _{OH6}		10	50	ns
Enable H pulse time	Read Write	E	—	t _{CCLW}	—	ns
				t _{CCLR}	70	—
Enable L pulse time	Read Write	E	—	t _{CCHW}	—	ns
				t _{CCHR}	30	—

(V_{DD} = 2.7 V to 4.5 V, T_a = -40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t _{AH6}	—	0	—	ns
Address setup time		t _{AW6}	—	0	—	ns
System cycle time	A0	t _{CYC6}	—	300	—	ns
Data setup time	D0 to D7	t _{DS6}	—	40	—	ns
Data hold time		t _{DH6}	—	15	—	ns
Access time		t _{ACC6}	CL = 100 pF	—	140	ns
Output disable time		t _{OH6}		10	100	ns
Enable H pulse time	Read Write	E	—	t _{CCLW}	—	ns
				t _{CCLR}	120	—
Enable L pulse time	Read Write	E	—	t _{CCHW}	—	ns
				t _{CCHR}	60	—

(V_{DD} = 1.8 V to 2.7 V, T_a = -40 to 85°C)

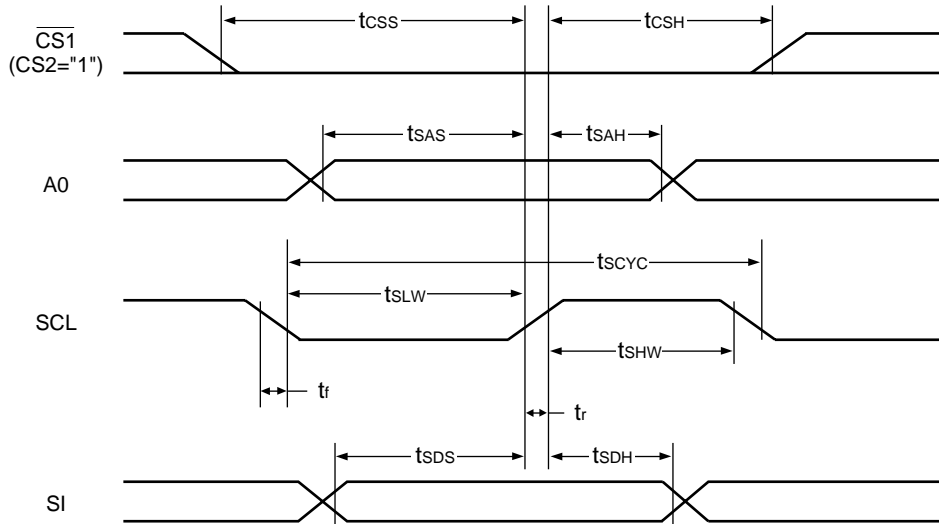
Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t _{AH6}	—	0	—	ns
Address setup time		t _{AW6}	—	0	—	ns
System cycle time	A0	t _{CYC6}	—	1000	—	ns
Data setup time	D0 to D7	t _{DS6}	—	80	—	ns
Data hold time		t _{DH6}	—	30	—	ns
Access time		t _{ACC6}	CL = 100 pF	—	280	ns
Output disable time		t _{OH6}		10	200	ns
Enable H pulse time	Read Write	E	—	t _{CCLW}	—	ns
				t _{CCLR}	240	—
Enable L pulse time	Read Write	E	—	t _{CCHW}	—	ns
				t _{CCHR}	120	—

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, (t_r + t_f) ≤ (t_{CYC6} - t_{EWLW} - t_{EWHW}) for (t_r + t_f) ≤ (t_{CYC6} - t_{EWLR} - t_{EWHR}) are specified.

*2 All timing is specified using 20% and 80% of V_{DD} as the reference.

*3 t_{EWLW} and t_{EWLR} are specified as the overlap between CS1 being "L" (CS2 = "H") and E.

● Serial Interface



(VDD = 4.5 V to 5.5 V, Ta = -40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial Clock Period	SCL	tSCYC	—	200	—	ns
SCL "H" pulse width		tSHW		75	—	ns
SCL "L" pulse width		tSLW		75	—	ns
Address setup time	A0	tSAS	—	50	—	ns
Address hold time		tSAH		100	—	ns
Data setup time	SI	tSDS	—	50	—	ns
Data hold time		tSDH		50	—	ns
CS-SCL time	CS	tCSS	—	100	—	ns
		tCSH		100	—	ns

(VDD = 2.7 V to 4.5 V, Ta = -40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial Clock Period	SCL	tSCYC	—	250	—	ns
SCL "H" pulse width		tSHW		100	—	ns
SCL "L" pulse width		tSLW		100	—	ns
Address setup time	A0	tSAS	—	150	—	ns
Address hold time		tSAH		150	—	ns
Data setup time	SI	tSDS	—	100	—	ns
Data hold time		tSDH		100	—	ns
CS-SCL time	CS	tCSS	—	150	—	ns
		tCSH		150	—	ns

SED1565 Series

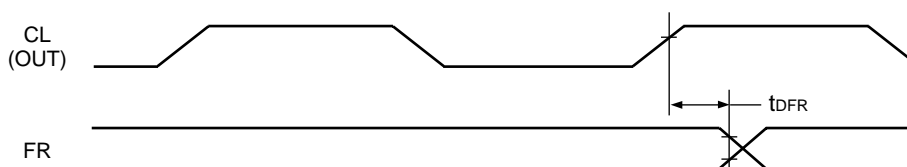
(V_{DD} = 1.8 V to 2.7 V, T_a = -40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial Clock Period	SCL	t _{SCYC}	—	400	—	ns
SCL "H" pulse width		t _{SHW}		150	—	ns
SCL "L" pulse width		t _{SLW}		150	—	ns
Address setup time	A0	t _{SAS}	—	250	—	ns
Address hold time		t _{SAH}		250	—	ns
Data setup time	SI	t _{SDS}	—	150	—	ns
Data hold time		t _{SDH}		150	—	ns
CS-SCL time	CS	t _{CSS}	—	250	—	ns
		t _{CSH}		250	—	ns

*1 The input signal rise and fall time (t_r, t_f) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of V_{DD} as the standard.

● Display Control Output Timing



(V_{DD} = 4.5 V to 5.5 V, T_a = -40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time	FR	t _{DFR}	CL = 50 pF	—	10	40	ns

(V_{DD} = 2.7 V to 4.5 V, T_a = -40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time	FR	t _{DFR}	CL = 50 pF	—	20	80	ns

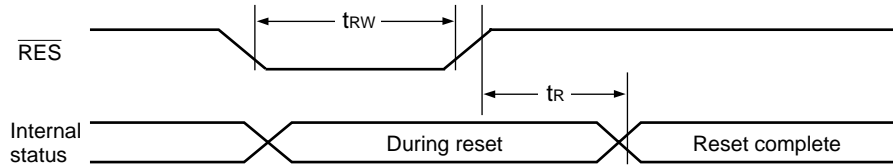
(V_{DD} = 1.8 V to 2.7 V, T_a = -40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time	FR	t _{DFR}	CL = 50 pF	—	50	200	ns

*1 Valid only when the master mode is selected.

*2 All timing is based on 20% and 80% of V_{DD}.

● Reset Timing



($V_{DD} = 4.5\text{ V to }5.5\text{ V}$, $T_a = -40\text{ to }85^\circ\text{C}$)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time		t_R	—	—	—	0.5	μs
Reset "L" pulse width	RES	t_{RW}		0.5	—	—	μs

($V_{DD} = 2.7\text{ V to }4.5\text{ V}$, $T_a = -40\text{ to }85^\circ\text{C}$)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time		t_R	—	—	—	1	μs
Reset "L" pulse width	RES	t_{RW}		1	—	—	μs

($V_{DD} = 1.8\text{ V to }2.7\text{ V}$, $T_a = -40\text{ to }85^\circ\text{C}$)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time		t_R	—	—	—	1.5	μs
Reset "L" pulse width	RES	t_{RW}		1.5	—	—	μs

*1 All timing is specified with 20% and 80% of V_{DD} as the standard.

NOTICE:

No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. This material or portions thereof may contain technology or the subject relating to strategic products under the control of the Foreign Exchange and Foreign Trade Law of Japan and may require an export license from the Ministry of International Trade and Industry or other approval from another government agency.

© Seiko Epson Corporation 2000 All right reserved.

All other product names mentioned herein are trademarks and/or registered trademarks of their respective companies.

SEIKO EPSON CORPORATION

ELECTRONIC DEVICES MARKETING DIVISION

IC Marketing & Engineering Group

ED International Marketing Department I (Europe, U.S.A)

421-8 Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: 042-587-5812 FAX: 042-587-5564

ED International Marketing Department II (ASIA)

421-8 Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: 042-587-5814 FAX: 042-587-5110

■ Electronic devices information on the Epson WWW server.

<http://www.epson.co.jp/device/>

